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DESIGN AND ANALYSIS OF InP AND GaAs DOUBLE GATE MOSFET TRANSISTORS FOR LOW POWER APPLICATIONS

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Abstract

This paper deals with a novel Double Gate MOSFET (DG MOSFET) which is constructed by the unification of III group materials (Indium, Gallium) and V group materials (Phosphide, Arsenide) is analyzed. Due to its short channel effect immunization, leakage current reduction and higher scaling potential, DG MOSFET as one of the most comforting devices for low power applications. In this work, we investigated the effect of DG MOSFET based on Indium Phosphide (InP) and Gallium Arsenide (GaAs) on optimal performance and drain current characteristics by replacing traditional DG MOSFET based on silicon. The transistor's channel length is set to 20 nm. Both devices have been modeled using the NanoHub simulator and characteristics has been examined using Matlab. The descriptive analysis of characteristics has been performed through the corresponding plot structures - energy band structure, I_D vs V_{GS} characteristics, I_D vs V_{GS} characteristics, transconductance. From the results provided, it has been found that the DG MOSFET device based on InP offers ON current 10^{-3}A is better than the DG MOSFET device based on Silicon and Gallium Arsenide (GaAs).

Keywords:

DG MOSFET, GaAs, InP, ON Current, OFF Current

1. INTRODUCTION

For the past few decades, the dimensions of the Metal Oxide Semiconductor Field Effect Transistor (MOSFET) device is reduced below 100nm. Now- a-days, the devices are scaled down below 20nm in order to enhance the speed, significant number of components contained per chip and to lower the cost. Correspondingly, various short channel effects were explored [1] [2]. The current ratio of ON-OFF state determines the output of the device. Improvising the ON-state current and avoidance of short channel effects (SCEs) is the demanding factor in typical MOSFET and one of the nanoscale devices available to accomplish all these characteristics is Double Gate (DG) MOSFET based on silicon. The Short Channel Effects(SCEs) typically comprise drain induced barrier lowering (DIBL), gate leakage current, threshold voltage roll-off, subthreshold swing, leakage current, punch through and so on.

DG MOSFET has an electrostatically improved device design consisting of two gates, while the conventional MOSFETs have a one gate. Such gates offer effective control of the channel from both ends. As for the gate bias, it can be graded as Symmetrically Driven Double Gate (SDDG) and Independent Driven Double Gate (IDDG). In SDDG, the same bias is imposed at both the gates and in IDDG, the different bias is imposed at both the gates [3]-[5].

The silicon-based DG MOS transistor goes outside its physical and optimal limits and does not persuade the ITRS roadmap criteria in accordance with the moore's law. Therefore requires a different device design and appropriate materials channels and gate dielectrics [6] [7]. Such device designs can reduce static power (off-current) and power utilization, together with enhanced switching speed and drain current.

In the sector of InP and GaAs based DG MOS transistors, a minimal number of research studies have contributed. III-V composite semiconductors with greater electron mobility, a supportive device design for tremendous speed and low power implementations instead of DG MOS transistors based silicon [8] [9].

In this work, InP and GaAs are considered to be the surface materials of DG MOSFET among III-V composite semiconductors. In the case of larger electron mobility, higher speed saturation, higher thermal conductivity at a room temperature, making InP-based DG MOS transistors with the aid of several technologies is of particular interest. GaAs-based devices have 5 times higher mobility of electron than Si-based devices with better breakdown. The features of GaAs MOSFET provide improved drain current, minimized gate leakage current and increased flexibility in digital integrated circuit design [10] [11].

The electrical parameters such as electrostatic potential, electric field distribution on the channel, I_D vs. V_{GS} characteristics, I_D vs. V_{GS} characteristics and transconductance are analyzed. Finally, all the device parameters acquired are contrasted with traditional DG MOSFET based silicon. All such results play a key role in explaining the transition and modifiability of experimental devices on a nano scale.

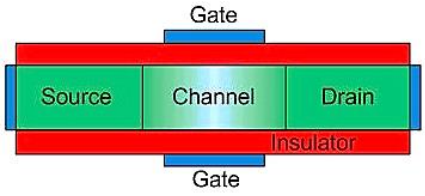

Fig.1. Schematic cross section of DG MOSFET

2. METHODOLOGY

The schematic cross section of DG MOSFET is exposed in Fig.1. In our research, the gate is formed of poly silicon material and Silicon-di-oxide is used as the insulator. The regions of substrate, Source and drain consist of Indium Phosphide (InP) and Gallium Arsenide (GaAs).

The room temperature properties of the surface materials InP and GaAs (300 K) has the electron mobility (Cm^2/Vs) of 5400 and 8500, respectively. Similarly for InP and GaAs, electron affinity (eV) as 4.38 and 4.07, electron saturation velocity ($\times 10^7$cm/s) as 2.2 and 1.2, hole saturation velocity ($\times 10^6$cm/s) as 8 and 2.1, thermal conductivity (W/cm×k) as 0.7 and 0.5, dielectric constant as 12.4 and 12.9, energy gap (eV) as 1.344 and 1.424, electron effective mass (Kg) as 0.073 and 0.067, minority carrier lifetime

(ns) as 200 and 1.66. These parameters has been comprised in the nanohub simulator.

3. NANOHUB SIMULATION

Nanohub simulator seems to be a scripting language of Multigate Field Effect Transistor (MUGFET), a simulation platform built for FET models at the US-Purdue University. Through choosing either PROPHET or PADRE simulators, these simulations can be implemented. These simulators were engineered at Bell Laboratories. PADRE is an application-oriented simulator of 2D or 3D device models such as MOS transistors, while PROPHET simulator is beneficial in solving Partial Differential Equations (PDEs) and supports the Poisson equations and drift-diffusion equations with effective results. PADRE makes some valuable engineering characteristic plots and intense physics analysis. There are also many equivalents to numerical methods and physics of semiconductor devices [12]. In this paper, PADRE simulator is selected to acquire various characteristics such as like electrostatic potential, total electric field, characteristics of drain current (I_D) with respect to both VDS and VGS and transconductance.

The device parameters of nanohub simulation used by DG MOSFET are channel width (W_{CH}) as 5nm, Oxide thickness (t_{ox}) as 1nm, Gate length (L_G) as 20nm, Source and drain extension length as 40nm, Source and drain doping concentration as $10^{20}/cm^3$, and channel doping concentration as $10^{15}/cm^3$.

4. RESULT AND DISCUSSIONS

In this section, DG MOSFET in the nanometer region provided numerical results of the electrostatic potential, total electric field distribution, I_{DS}-V_{GS} characteristics, I_{DS}-V_{DS} characteristics and transconductance of Indium Phosphide (InP) and Gallium Arsenide (GaAs).

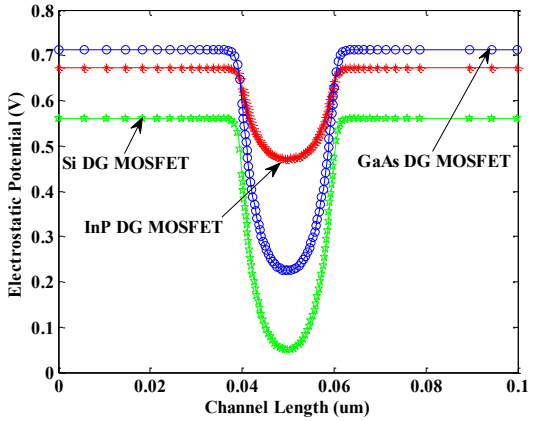

Fig.2. Electrostatic potential profile of Si, GaAs and InP based DG MOSFET

The Fig.2 shows the Electrostatic potential profile channel length (L) of DG MOSFET based on Si, GaAs and InP is 20nm. The Fig.2 clearly shows that the InP-based DG MOSFET offers greater potential in the channel area than DG MOSFET based on silicon and GaAs. In addition the potential is relatively large at the source side and drain side than at the middle of the channel. Therefore, the DG MOSFET model based on InP delivers better electrostatic potential for enhancing electrical characteristics.

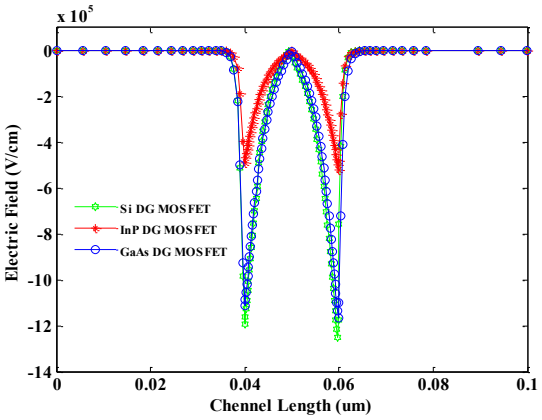

Fig.3. Total Electric field profile of Si, GaAs and InP based DG MOSFET

The Fig.3 shows the total electric field profile channel length (L) of DG MOSFET based on Si, GaAs and InP is 20nm. The drain bias applied is 0.3V and the gate bias is 0.5V. The channel length is very small (L=20nm) in the proposed device design. Therefore, it is a remarkable part of an electrical field in both the vertical (y-direction) and lateral (x-direction) axes. The influence of the electric field on the channel area tends to increase the carrier transport efficiency. Hence, the InP-based DG MOSFETs achieve the best electrical field pattern compared to the DG MOSFETs based on silicon and GaAs at the channel region, which actually improves drain current.

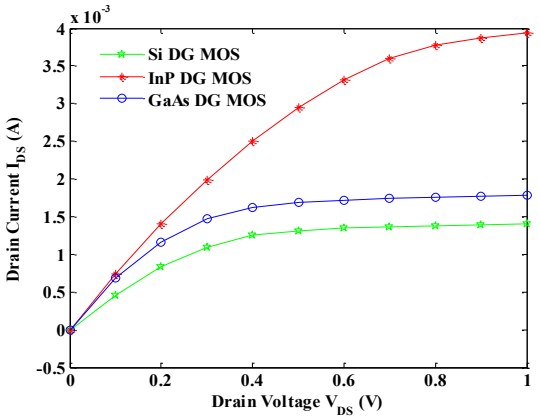

Fig.4. IDS-VDS characteristics of Si, GaAs and InP based DG MOSFET

The Fig.4 depicts the Si, GaAs and InP-based DG MOSFET I_{DS}-V_{DS} characteristics. The velocity saturation and pinch-off are related to the MOS device's drain bias. Therefore, with shortest DG MOSFET gate lengths (L=20nm) in the sub-micrometer scale, the saturation of the velocity would exist near the drain portion of the channel at smaller V_{DS} than the pinch-off.

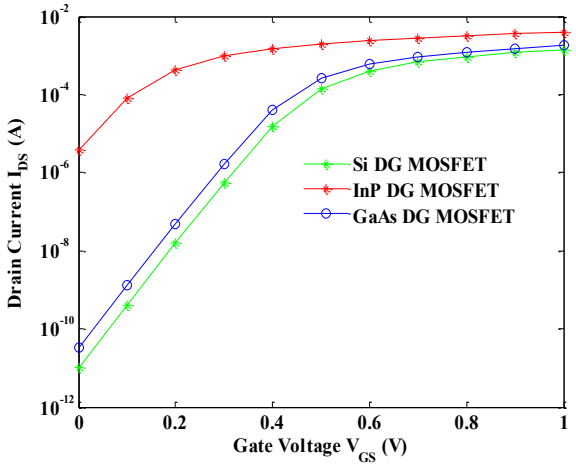

Fig.5. IDS-VGS characteristics of Si, GaAs and InP based DG MOSFET

The Fig.5 shows the I_{DS}-V_{GS} characteristics of the DG MOSFET based on Si, GaAs and InP. The gate voltage generates a field in the x-direction that causes charge and current flows across the y-direction channel. The Fig.5 shows that the gradual increase in gate voltage (V_{GS}) results in an increase in drain current (I_{DS}). Whenever the gate voltage falls below 0.6V, the drain current achieves saturation. It has also been noted that the DG MOSFET model based on InP offers stronger ON current (10^{-3}A) than Si based DG MOSFET (10^{-5}A) and GaAs based DG MOSFET (~10^{-5}A).

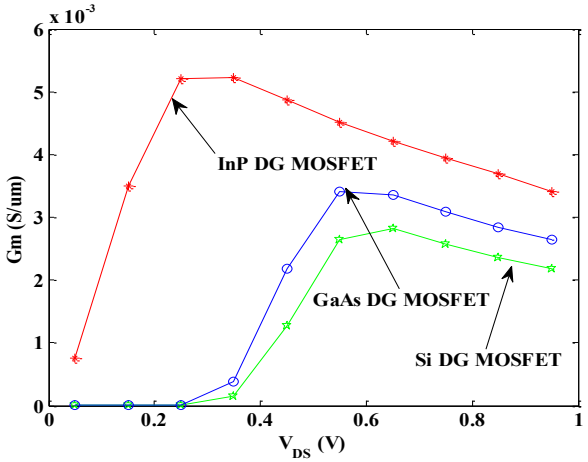

Fig.6. Transconductance of Si, GaAs and InP based DG MOSFET

The Fig.6 depicts the transconductance curve of the DG MOSFET based on Si, GaAs and InP. Transconductance is the ratio of the change in drain current (I_D) over a specified short interval to the change in gate voltage (V_{GS}). Better channel conductance and transconductance values for greater electron mobility, better gate insulator capacitances (i.e. thin gate insulator layers) and massive gate width to longitudinal ratios. Therefore, DG MOSFETs based on InP achieve a better transconductance curve than DG MOSFETs based on silicon and GaAs.

5. CONCLUSION

In this paper, the enhanced drain current characteristics of DG MOSFET were investigated by analyzing III and V group elements DG MOSFET based on Gallium Arsenide and Indium Phosphide to silicon based DG MOSFET. The whole device design is developed and modeled using nanohub online simulator. The electrical parameters of the device such as electrostatic potential, electric field distribution on the channel, I_D vs. V_{GS} characteristics, I_D vs. V_{GS} characteristics and transconductance have been studied. The electrostatic potential (0.49eV) and electric field (-4×10^5V/cm^3) for InP-based DG MOSFET are relatively higher. It has also been found from the results presented that the InP-based DG MOSFET device design offers a remarkable improvement in the ON state current (10^{-3}A). As a result, the leakage current is in the range of 10^{-11}A to 10^{-10}A and ON state current is improving (10^{-4}A) for the DG MOSFET structure based on GaAs. Both DG MOSFET based on InP and DG MOSFET based on GaAs tend to be preferred devices for applications with low power. Among these, DG MOSFET based on InP offers a better performance characteristic than DG MOSFET based on GaAs.

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