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PROCESS FOR IMPLEMENTATION OF TRANSMISSION LINE ON STANDARD SILICON SUBSTRATE AND ITS CHARACTERIZATION AT KA-BAND

K. Singh and A.V. Nirmal
System Engineering Group, U R Rao Satellite Centre, India

Abstract
Planar transmission line on silicon substrate imposes certain challenges at higher frequencies and measurement of the same employing wafer probing techniques needs accurate characterization. Wafer measurement provides information related with the device performance which in turn helps to minimize parasitic related with package and assembly. Wafer probing at higher frequencies imposes certain challenges more so ever on silicon substrate. Silicon substrate due to semiconductor in nature is a lossy medium for radio frequencies and standard wafer is not suitable for the realization of RF circuits. Present article demonstrate realization of planar transmission line on high resistivity silicon substrate by employing thick oxide layer. Both simulated and measured results are presented in this article and the CPW line fabricated with the proposed process results in ~1dB loss with better than 12dB return loss at Ka-band. Measurement techniques for the line characterization are detailed in this article along with transmission line characterization at Ka-band.

Keywords:
Wafer Probing, Testing, Measurement, Radio-Frequency

1. INTRODUCTION

Standard silicon substrates for RF applications is not preferred due to associated high dielectric losses and so are having limited usage at lower end of frequencies. High quality passive components on standard silicon impose challenges resulting in the difficulty of RF-CMOS realization [1]. Various approaches for employing silicon technology for RF domain are proposed such as micromachining, thick oxide layer, ion-implantation, and high resistivity wafer [2], [3]. To circumvent various aspects of each approach, authors propose combination of technologies which can result in high performance passive components at higher frequencies. In the proposed article, coplanar waveguide (CPW) transmission line is realized on the oxide layer over the high resistivity silicon wafer which is fully compatible with the standard CMOS processing [4]. At higher frequencies, radiation and dispersion are more prominent compared to other losses on standard substrate whereas in silicon added dielectric losses leads to overall higher losses. Coplanar waveguide is preferred transmission media at higher frequencies due to low parasitic and ease of probing. As in coplanar waveguide (CPW) the signal lines and ground planes are all placed on one side so a circuit consisting of passive components and active devices can be implemented by CPW with ease of implementation [5].

The connectorised based characterization involves extra losses which are detrimental at higher frequencies. On-wafer characterization is presently employed for measurement of MMIC and MEMS devices whereas measurement of RF microstrip components involves transition so as to probe the circuit [6]. Wafer probing techniques are directly employed for the line characterization [7]. Various substrate and subsequent parameters are listed in Table.1, where in the major difference inherently in silicon substrate is constant non-uniform resistivity across wafer apart from high dielectric permittivity.

Table.1. Substrate comparison

Parameters	PCB	Alumina	Silicon
Thickness	Uneven	Even	Even
Line width control	Not good	Good	Good
Surface	Rough	Smooth	Polished
Dielectric filling	Non-uniform	Uniform	Uniform
Dielectric purity	High	Low	Low
Thermal conductivity	Good	Poor	Good
Brittleness	Low	High	High
Dielectric constant	Low	High	High
Resistivity	High and uniform	High and uniform	Comparatively low and non-uniform

Measurement at Ka-band imposes challenge due to various parasitic and associated losses which results in the deviation of the circuit performance from the simulated performance. This article details the line characterization apart from standard probing and characterization techniques, measurement challenges, various wafer probing techniques, testing and measurement at Ka-band frequencies.

2. FABRICATION AND MODELING ASPECTS

The fabrication process initiated with the cleaning of the wafer followed by dielectric deposition on the top side. The choice of the wafer either p-type or n-type is immaterial as the electrical characteristics are independent for the same in RF circuits. The dielectric material choice is taken oxide and the thickness of dielectric material is kept high, so PECVD process is employed for the dielectric deposition (Fig.1). Further aluminum metallization using sputtering is carried out [1]. Silicon substrate acts as the dielectric layer if its wafer conductivity is very low and can support dielectric quasi-TEM mode. High frequency and high conductivity of silicon substrate will make it to act as a metal layer and it supports skin effect mode. Moderate conductivity and working frequency will lead to slow wave mode. Mostly slow-wave mode propagates in the silicon substrate due to finite resistivity. The criteria for the same are having small frequency compared to dielectric relaxation frequency and depth of quasi-

static field penetration is small compared with the skin-depth of the substrate.

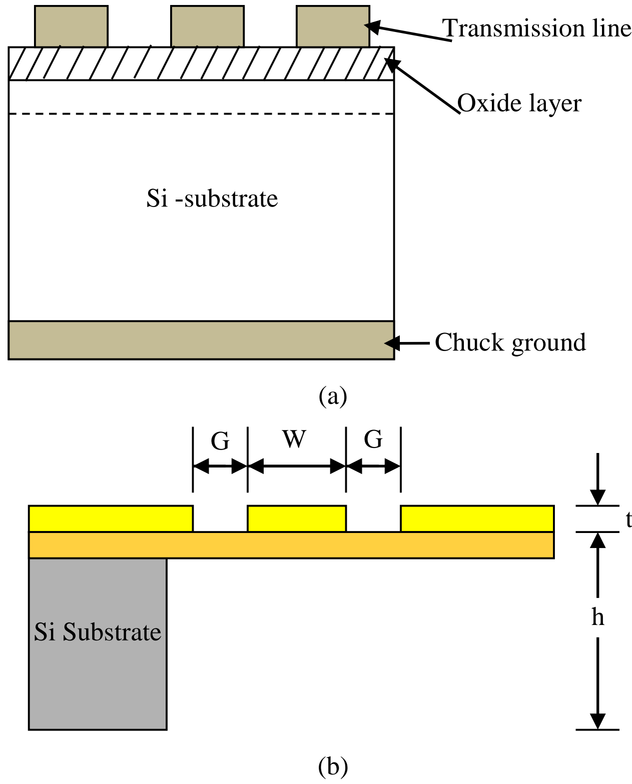

Fig.1. Cross section view of the CPW line

Silicon is a semiconductor and having finite resistivity so the losses associated with silicon are due to ohmic and dielectric polarization. At Ka-band, the polarization losses dominate due to dielectric behavior and are much higher compared to the ohmic losses. The losses are enhanced with the frequency due to increase of substrate resistivity. Further, ohmic losses are also significant higher due to the finite metallization thickness employed in standard foundries. The resistivity of the substrate plays prominent role as current flowing along the wafer surface depends on the intermediate dielectric layer. Low resistivity silicon substrate allows maximum electric field concentrated in dielectric layer whereas semi-insulating substrate allows penetration of electric filed into substrate resulting in quasi-TEM mode. In the present article, thicker oxide layer and high resistivity substrate is employed so as to avoid spurious and other mode of propagation. The equivalent model can be represented in Fig.2(a). C_{ox} depends on the oxide thickness whereas R_{si} depends on the substrate resistivity (Eq.(1)) and the wafer resistivity is modeled as variable capacitor. C_{pad} and R_{pad} are associated with the probing pad. The series losses are dominated by the inductance and associated resistances which are shown as R and L in the Fig.2(b).

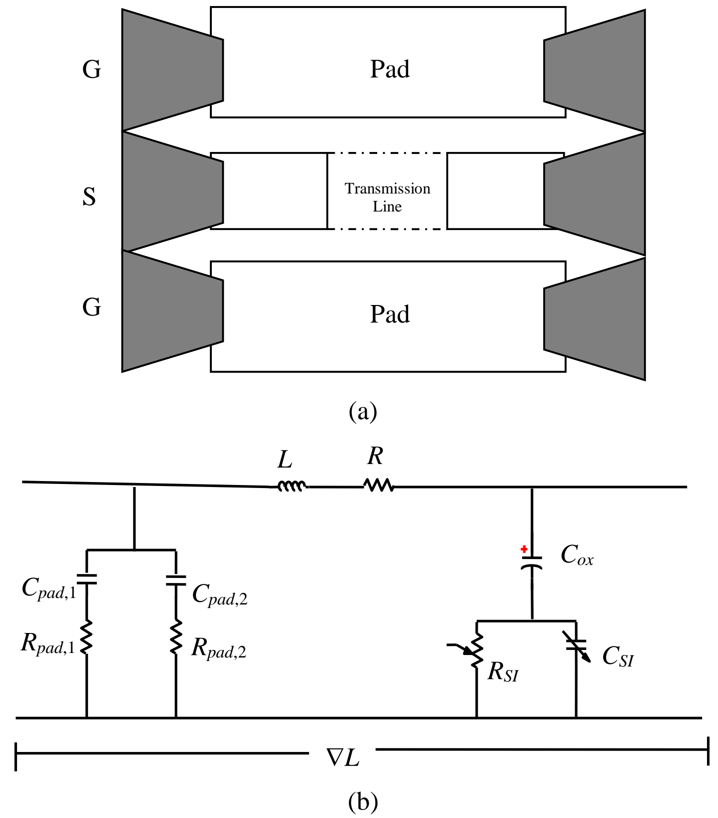

Fig.2. Structure and equivalent circuit

$$C = \frac{\omega \cdot \ell \cdot \varepsilon_0 \varepsilon_{eff}}{t_{eff}}$$

$$\varepsilon_{eff} = \frac{1+\varepsilon}{2} + \frac{\varepsilon - 1}{2}\left(1 + \frac{10t}{\omega}\right)^{-0.5}$$

$$\frac{1}{R} = \frac{t_{eff}}{\sigma_{eff}\,\omega \cdot \ell} \tag{1}$$

Wide transmission lines, primarily employed in the pad, lead to higher losses and to be avoided in circuit implementation. The transmission line losses are dependent on the intermediate layer (oxide) thickness, substrate resistivity and frequency. The role of passivation layer is studied by Verma et al. [8] and increasing the dielectric layer thickness increases the characteristic impedance but decreases the effective permittivity. The effect of W/t is negligible after certain value of ε and Z_0, whereas permittivity is constant with frequency variation.

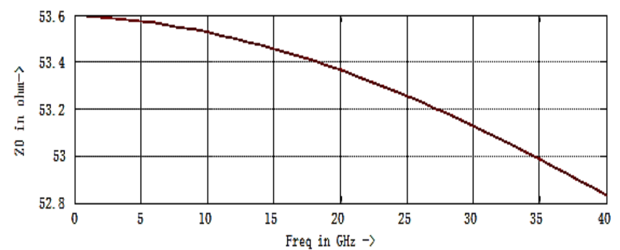

Fig.3. Characteristic impedance variation with frequency for constant W/h

Passive elements are characterized by quality factor and associated parasitic by the pads degrades the value. Enhancement of quality factor can be carried out by enhancing the values of R_{si} and C_{si} (Fig.2(b)) which are associated with silicon substrate.

3. WAFER PROBING AND CALIBRATION

Key parameters for probe measurements are repeatability, RF performance and calibration procedures. Wafer probing is preferred compared to the test fixture approach as apart from the higher losses test fixtures are limited to frequency ranges. Measurements using VNA through cables and connectors introduce phase shift and mismatch losses. The Table.2 summarizes the various parameters.

Table.2. Generic comparison between wafer probing and test fixtures

Parameter	Wafer probing	Test fixtures
Flexibility	Poor	Good
Cost	High	Low
RF reflection	Low	High
Ground loops	Low	High
Frequency Range	Wide	Narrow (customized)

The RF probes should have superior field confinement reducing unwanted coupling and transmission lines and for low contact resistance measurements. The main blocks of wafer level measurement are: equipment, wafer, calibration standard, cable, and probe station. The main parameters for the probe measurement are: contact pressure, repeatability, RF performance, calibration procedures [9]. Electrostatic chucks employing proper grounding mechanism to be ensured. Probing can be for DC and RF (Fig.3) behavior where DC probing involves single pad and RF probing is primarily using G/S/G or G/S. Bias tees are employed where both DC and RF are implemented simultaneously.

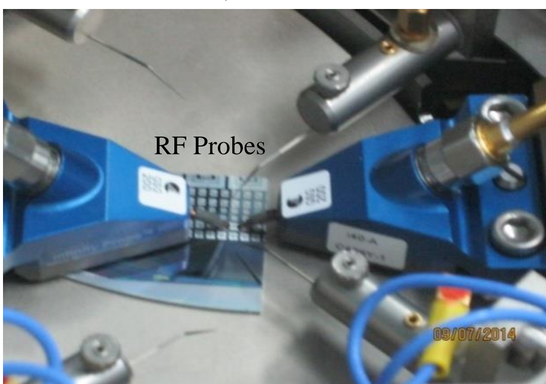

Fig.3. Wafer probing using G/S/G probes

Wafer probing is carried using the probes and generally having G/S/G configuration so as to minimize losses and crosstalk associated with characterization. Other probing techniques such as G/S and S/G are also employed on Si circuits resulting in compactness of the circuit with the excitation of the multiple modes. The ground plane on both sides of signal lines in G/S/G configuration grounds the radiated fields and having lesser ground inductance compared to S-G probe.

Impedance standard substrate (ISS) is having planar structures in CPW mode and structures are made on the alumina substrate. Various calibration techniques such as SOLT, TRL, LRL, TRM or LRM are employed and errors associated with VNA, cable, probes and reflections to be removed before testing. SOLT (Short, Open, Load and Through), LRM (Line, Reflect, Match) and LRL (Line, Reflect, Line) calibrations are preferred techniques for wafer probe measurement. Calibration using TRL is preferred over SOLT due to parasitic consideration. The TRL calibration technique does not rely on perfectly known standards but relies on the characteristic impedance of a short transmission line. TRM technique is not frequency limited as compared to TRL but TRM technique is not preferred on Si wafer due to large variations in the load value. The role of calibration substrate is important for initiating the calibration and matching with recommended pitch range.

Probe station is having DC and RF positioners, probe head, RF probes, chuck, platen, probe holders and tips. Probes material are either Ni, W or BeCu where BeCu is having low contact resistance whereas W probes can penetrate through oxide layer for making electrical contact. Major probe parameters are

- RF operating range
- Probe pitch
- Insertion Loss
- Return Loss
- Contact Resistance
- Connector type
- Crosstalk

4. LINE CHARACTERIZATION

The transmission line structure is simulated in the standard software for the desired frequency range. Various parameters such as parasitic, device mounting, reference plane de-embedding effects the circuit performance. RF probing using the probe station is carried out as shown in Fig.4 where signal line is probed using GSG probe.

Fig.4. RF probing of CPW line

The Fig.5 shows the simulated results along with the measured value. The simulation carried out using MOM techniques considered ideal substrate while in actual condition the finite

resistivity plays important role in RF measurements. The calibration is carried out using the TRL methodology. Due to thicker oxide thickness, the effect of resistivity variation across wafer is minimized and the same is corroborated with the multiple die characterization. The wafer probe measurement shows that the losses associated with this approach is ~1dB (max) with the return loss better than 13dB at Ka band for the fabricated lines. Further in some cases the results are close to the simulated one which can be inferred to the resistivity variation across wafer associated with the high resistivity wafer. The imbalance between the ground return path between ground pads and substrate are also important considerations for reducing the losses apart from other associated losses.

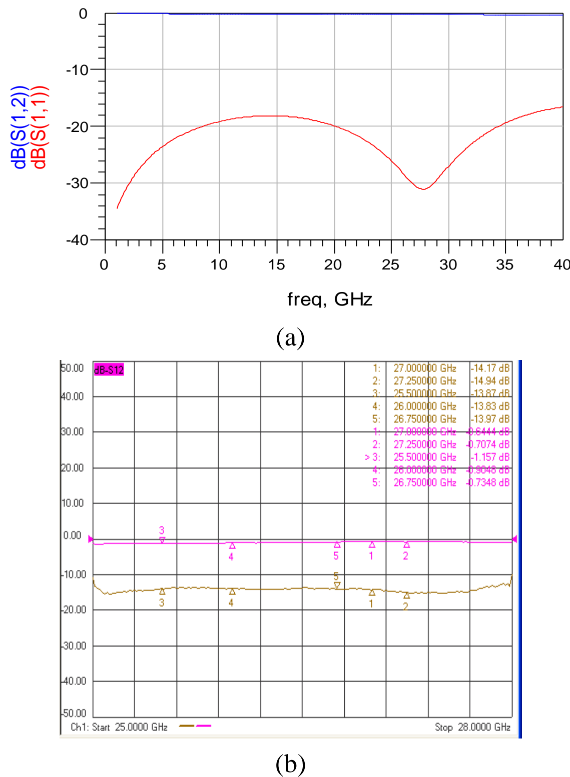

Fig.5. Characterization (a) simulated (b) measured results

The measured results show that proposed technique effectively reducing silicon substrate losses. Small deviations in the simulated and measured results are attributed to the finite resistivity. Much thicker layer of oxide can nullify the silicon resistivity effect but it can lead to fabrication and reliability issues [10]. This process can easily be incorporated for the realization of RF-CMOS circuitry on the standard silicon substrate [11].

5. CONCLUSION

This paper details the transmission line characterization at Ka-band using direct wafer probing. Various parameters such as selection of planar lines, calibration and probing techniques, modeling aspects are discussed. Testing of the wafer is carried out to verify the proposed approach of implementing thicker oxide over silicon substrate. The approach of realization of RF circuits over thick oxide over high resistivity silicon yields in low losses at Ka-band. Lower end of RF frequency standard techniques such as ion implantation, micromachining can be adopted but at high frequencies accurate modeling of the same is complex. Measurement is band limited to accurately characterize the transmission line. Further fabrication processes are complicated and results in multiple steps. Present approach is fully CMOS compatible and can yield high quality passive components using standard foundries while facilitating designer to take into account packaging effects.

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