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ANALYSIS OF DATA SKIPPING USING LOW TRANSITION SWITCH REGISTERS

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Abstract

The emerging scenario in the fields of VLSI testing has its own demand for fault diagnosis in VLSI circuits. If the area and size of the circuit increases the problem of test generation time becoming very tough. Efficient techniques for test generations are essential in order to reduce the test generation time and size. In Existing methods, Low transition Switch Register (LTSR) applies the corresponding repeated patterns of the generated test data. The complication in the LTSR technique exponentially increases power with respect to the circuit size. In case of circuit which has more stuck-at-fault, the LTSR method fails to provide suitable fault coverage and low power consumption. The proposed test data skipping scheme using Reconfigurable Johnson counter reduces the test data volume from the multiple test pattern and reduces switching transitions by skipping the test sequence mostly between the consecutive test sequences. The RJC based Test data skipping scheme has additional circuit which consists of various counters, Bit skipping circuit and logic gates. Memory unit consists of the whole test sequence then these test sequences are fed to RJC and Switching Transition counter. The consecutive test sequence are eliminated or skipped by comparing those counters and the state analysis of FSM. The proposed test data skipping scheme circuit is developed to achieve minimum test patterns and reduced scan power by skipping long scan chain switching activities. This present work with the above mentioned issues for LTSR and existing in VLSI circuits is to examine all detectable faults with proposed circuit. The Efficiency of such system is tested by Xilinx and ISE tools to generate test patterns to achieve high fault coverage with low power consumption over the conventional systems.

Keywords:

LTSR, Test Data Skipping Algorithm, Reconfigurable Johnson counter, ATPG

1. INTRODUCTION

With the advancement in semiconductor manufacturing technology, a Very-Large-Scale-Integration (VLSI) device can now contain tens to hundreds of millions of transistors which has led to many challenges during manufacturing test. In digital VLSI circuit design, power dissipation and testing speed has become a critical design concern in recent years driven by the emergence of portable devices in mobile applications. This is applicable not only to design power but also for testing power [1]-[3].

In testing process, if test vector sets are not optimized for power, even low power circuits dissipate more than twice the power under test, than at normal operating condition. This is because the large and complex chips require a huge amount of test data and dissipate a substantial amount of power during test. The reason is that the consecutive input test vectors are statistically independent which results in increased switching activity in the circuit during testing. There are many test parameters that should be improved in order to reduce the test cost. These parameters include the test power, test length (test application time), test fault coverage, and test hardware area overhead [10]-[12].

Minimization of test power, test length (test application time), test fault coverage, and test hardware area overhead in testing of VLSI circuits is challenging problem for the researchers. Thus the above factors motivated to-do research in this area. Most of these techniques to enhance the design of the conventional LFSR method (or other forms of TPGs such as cellular automata) in such a way as to reduce the transitions in the primary inputs of the Circuit Under Test (CUT) for test-per-clock BIST (Built in Self-Test) or inside the scan-chain for scan-based BIST.

Numerous related research works are already existed in literature which based on test generation circuit of the system. Some of them are reviewed here.

A BIST technique based on multiplier-accumulator pair for data path architecture to overcome the issues of power is proposed in [3]. Another low power test pattern generation model [4] is developed based on cellular automation for combinational circuits.

In [5] a distributed BIST control scheme to simplify the testing activity for complex ICs is proposed. Two different types of LFSR based on the performance of speed are developed in [6], for a circuit which has inputs with high transition densities.

The circuit-reliant and fault coverage efficiency are the major drawbacks of the above said BIST schemes. The State Skip scheme of Linear Feedback Shift Registers (LFSRs) is presented in [7]. In this skip method, the Linear Feedback Shift Registers detects the consecutive or repeated test sequence. So that the useless parts of the test sequences are skipped by State Skip LFSRs mode.

In [8], the author proposed a new scheme for Built-In Test (BIT) that utilizes Multiple-polynomial Linear Feedback Shift Registers (MP-LFSR's). The MP-LFSR that produces random patterns to envelop easy to test faults is loaded with seeds to make deterministic vectors for difficult to test faults. The seeds are developed by solving systems of linear equations connecting the seed variables for the positions where the test cubes have specified values.

In [9], the authors explained a design of an LFSR (linear feedback shift register) that can effortlessly contain a change-of-seeds feature. This novel LFSR is activated by two separate clocks, one operates the normal LFSR and another one operates the change of seeds option. The change of seeds is speedy since it is skilled by a pair of clock pulses rather than by long scan operations. Over a long phase, there are many schemes based on LFSR has been proposed as the best test pattern generator for the circuit under test. On the go, many modified LFSR schemes have been developed for low power VLSI testing.

Though there are many contributions in the low power testing. The excessive switching activity in the CUT causes many problems like reliability failure, manufacturing yield loss, high power consumption and hardware overhead as discussed above. Thus the survey leads to consider low power and high speed VLSI testing an important issue in research. In the existing methods, conventional TPGs, running a test vector for short period of time causes loss of fault coverage. Also when the test vector runs for a

longer period of time increases the test cost and total power consumed during testing. Hence the thesis concentrates to reduce the test data volume which extensively improves the performance of the testing device, with the minimum test area and minimum test power consumption.

This work presents a proposed ATPG architecture which uses a regenerative Johnson counter and combinational circuit to reduce the test sequences; significantly reducing the power consumption and memory utilization leads to test data compression.

2. TEST DATA SKIP (TDS) SCHEME

The Fig.1 shows the general architecture of the proposed test data skip scheme and it shows the functional or logical blocks of the proposed algorithm with memory and CUT. The proposed structure has four main components namely reconfigurable Johnson counter RJC, Switching Transition Counter (STC), Finite state machine (FSM) and Bit selecting/skipping circuit (BSC). Firstly the whole test vectors are stored in memory which is feed to RJC and STC each time of testing. These test sequences are generated randomly using RJC architecture. Then the present test sequence is compared with the next consecutive test sequence using switching transition counter (STC). FSM generates different state value based on the correlation among the different test sequences. By using the FSM state output, Test sequences are skipped or selected with the help of BSC. Finally those test sequences are sent to CUT.

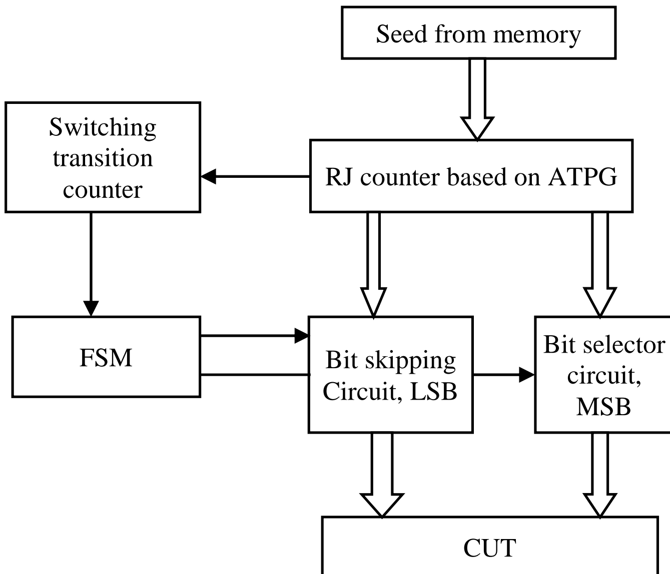

Fig.1. General Architecture of TDS Scheme

2.1 RJC-ATPG

The reconfigurable Johnson counter (Fig.2) uses D-FFs xor-ed with the feedback loop produces a new sequence of test vector. The RJC consists of D-flip flops and Multiplexer combined to generate automatic test patterns by selecting the mode of operation. The modified structure of RJC has five inputs namely *clk*, enable (*en*), selection line, *D* and q_{n-1} then single output as qn. Whenever the selection line which is equal to logic "0" then the proposed RJC counter starts to generate new test patterns using count operation to avoid the consecutive test sequences. If the selection line is set to logic "1" then the present test sequence (seeds) fed from memory.

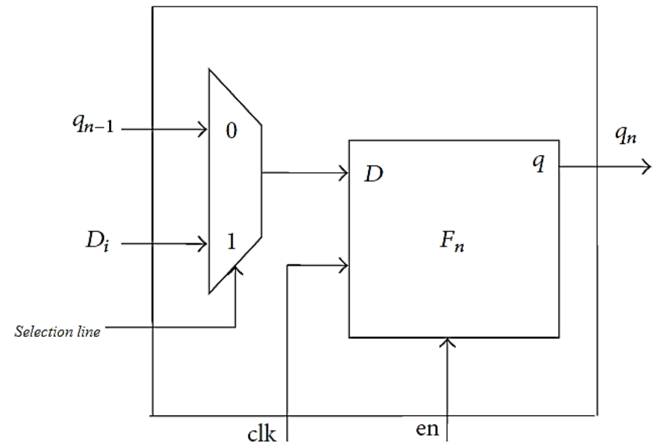

Fig.2. Proposed RJC based D flip flop

2.2 SWITCHING TRANSITION COUNTER

This section shows the switching transition counter which has XOR logic, Multiplexer and an OR gate. The current test sequence from the memory is compared with the next consecutive test sequences using XOR logic circuit. If the correlation between the test sequences is less then new test pattern inserted randomly. By inserting the random test sequences reduces the test data volume and skipping the unnecessary test sequences in the memory. After analyzing the test sequence which produces the FSM state value.

2.3 FINITE STATE MACHINE

The FST illustrates the State Transition Graph (STG) of an FSM. In that FSM, every node (*A*, *B* and *C*) corresponds to a states (s_0,s_1) and every arc corresponds to a transition (0,1). The label on the arc indicates the input that enables the transition and the output produced when the transition takes place. FSM access the input from the STC counter then provides the output to the BSC Circuit. The Table.1 shows the function performed in each state of FSM is as follows:

Table.1. Function performed at each FSM state

FSM State	Select Line S0 S1	Test patterns applied to Cut MSB LSB
A	1 1	Next value Next value
B	0 0	Present value Random bit
C	1 0	Present value Next value

2.4 BIT SELECTOR CIRCUIT

In the beginning of each test sequence is evenly separated into two parts which is named as LSB and MSB. Partial part of the LSB has Bit selection or skipping circuit to avoid the consecutive

test patterns. These BSC circuit skips the test sequence based on the FSM states. The remaining (MSB) half of the test pattern must be stable during test vector skipping using bit selector MSB circuit.

Bit skipping circuit in LSB has Random bit generation using XOR logic operation to reduce the test data volume. It is clear that the skipping scheme is done by BSC Structure. Finally the random bit insertion improves the high fault coverage by avoiding unnecessary test patterns.

3. DECOMPRESSION ARCHITECTURE

This section shows the proposed decompression architecture having chain environment with RJC and STC Counter, BSC counter useful segment counter and decoder logic. Whenever a new seed entered various counters are used to compare and skip the sequence then the final seed id fed to useful segments counter. Then a new set of seeds are chosen for the more processing. To find out the excellence of the useful segment, Mode Select unit is used here. For this evaluation, all the values of Segment Counter, RJC Counter and STC Counter are decoded. The decoded output is given to the Mode Select unit to drive the proposed test data Skip logic.

For the decompression architecture, the Test data length evaluated using the control of speedup factor *k*, test sequence group *S* and window size *L*. These parameters are used to achieve the test data length (TDL) improvement. The TDL enhancement is designed by the subsequent rule:

$$\text{TDL Improvement (\%)} = \left(1 - \frac{TDL_{prop}}{TDL_{existing}}\right) \times 100$$

4. RESULTS AND DISCUSSION

The Modeling and implementation of the proposed TDS scheme is done in VHDL and simulation is carried out in Model Sim 6.5. Parameters like power, area are analyzed in Xilinx 14.2 ISE. In this paper, samples of 256 test patterns are analyzed for correlation, randomness and number of transitions between consecutive patterns. The validation of the analyzed patterns is done by applying to benchmark circuits of different complexity. Power analysis is done with the maximum, minimum and typical input test vectors for stuck-at faults and transition faults of combinational and sequential circuits. Results for each method are tabulated and compared with the previous methods. The obtained results proved that the reduced Dynamic power dissipation is by TDS scheme.

The Fig.3 shows that simulated output of the RJC, for *clk*=1 and control signal *sel* = 1, the output *J* are initialized to zero whereas for control signals are zero, the output confirms that 8 bit reconfigurable Johnson counter works as RJC-ATPG mode function. For control signal of logic 1, the output of reconfigurable Johnson counter is circular shifted for 8 *clk* cycles.

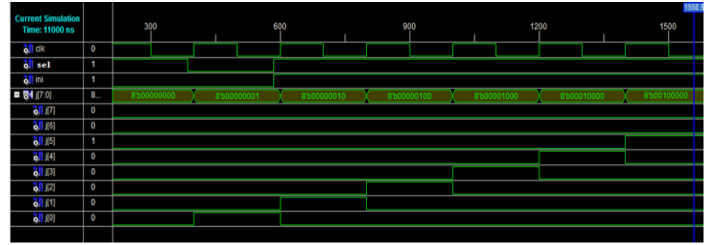

Fig.3. Output of Reconfigurable Johnson counter

The Table.2 shows the Comparison between the Existing Algorithms (LTSR) and proposed TDS algorithm for peak and average power analysis for ISCAS benchmarks in testing. From the analysis proves that TDS scheme reduces the power compared to LTSR.

Table.2. Power Reduction of Benchmark

Benchmark Circuit	LT-LFSR		Proposed TDS scheme	
	Average Power (μW)	Peak Power (μW)	Average Power (μW)	Peak Power (μW)
S5378	600	4200	582	2100
S9234	730	4520	680	2260
S13207	745	4735	602	2367.5
S15850	783	5904	594	2952
S38584	2466	19880	2102	9940

Table.3. Area overhead (%) of Benchmark

Circuit	LTSR (%)	TDS Scheme (%)
S5378	0.45	0.42
S9234	0.57	0.5
S13207	0.68	0.6
S15850	0.75	0.73
S38584	0.91	0.89

The Table.3 shows the area overhead results for TDS scheme compared to conventional LTSR method with low test data volume. The experimental results clearly show that the proposed method can be implemented for large designs with low area hardware.

The Table.4 illustrates the improvements in Test Data length reduction achieved by the proposed TDS method (using tetramax testing tool) for various values of *L*, *S*, and *k*. Columns labeled "TDL" present the reduction percentage for each case. It can be seen that the reduction achieved by the proposed method is very high (60%-96%).

Table.4. Test Data Length Improvements

Circuit	*L* = 50		
	Existing	Proposed	TDL
S5378	9000	1200	88%
S9234	9100	1082	88%
S13207	11100	1309	87%

S15850	9500	1129	88%
S38584	9450	3805	60%
Circuit	***L* = 200**		
	Existing	**Proposed**	**TDL**
S5378	30300	1790	92%
S9234	32400	1784	94%
S13207	31800	1756	93%
S15850	32400	1740	95%
S38584	25200	6639	74%
Circuit	***L* = 500**		
	Existing	**Proposed**	**TDL**
S5378	69000	2906	95%
S9234	76000	3055	96%
S13207	56000	2701	94%
S15850	79500	2791	96%
S38584	46000	9054	80%

The Table.5 reported the Fault coverage comparison (%) of different Benchmark circuits. The testing was conducted for selected versions of ISCAS'89 benchmark circuits with low power standard cell libraries. To estimate the fault diagnosing ability of the proposed scheme, various fault models were injected in the experiment. Test patterns were generated using proposed method and testing performance has more fault coverage than previous methods.

Table.5. Fault coverage comparison (%) of Benchmark

Circuit	LTSR (%)	TDS (%)
S27	89.61	96.32
S298	81.35	93.66
S15850	80.93	91.21
S38584	81.08	96.45

The Table.4 shows the specifications of ISCAS benchmarks and the number of test patterns required to hit a target fault coverage for existing LT-LFSR and proposed skipping algorithm. The Table.5 compares our results for the number of patterns and fault coverage.

5. CONCLUSION

This paper presents a new method to reduce the average and peak power of combinational and sequential circuits during the test mode. The switching activity in the CUT and scan chains and, eventually, their power consumption are reduced by increasing the correlation between patterns and also within each pattern. The proposed method achieves with almost no increase in test length to hit a target fault coverage. TDS algorithm significantly reduces the instantaneous power violation compared to the LFSR and, thus, avoids putting stress on the circuit during test.

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