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FRAMEWORK FOR PARAMETER EXTRACTION OF NONLINEAR MODEL FOR MESFETS AND IMPLEMENTATION IN CAD TOOLS

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Abstract

Extraction and implementation of nonlinear model in computer aided design (CAD) tools requires multiple steps. In this paper we present framework for nonlinear parameters extraction and implementation of model in CAD tools. Methodology selection at each step is based on the requirement according to the LN G7A in house fabricated MESFETs device and its application. To validate the model, simulated s-parameters from model are compared with measured data and percentage of error is below 10.3% from 500MHz to 20GHz. Measured and simulated drain to source current (Ids) is compared to validate the dc characteristics of the device. To evaluate the convergence of model in CAD tools, 5 to 5.5 GHz medium power amplifier is simulated which show that the model has not convergence issue during circuit simulation in Advanced Design System (ADS).

Keywords:

Nonlinear Device Modeling, Nonlinear Parameter Extraction, Nonlinear Model, MESFETs, pHEMTs

1. INTRODUCTION

To design nonlinear circuits using CAD tools like ADS /Microwave Office/Qucs/QucsStudio (last two are open source), we require to implement nonlinear model of device in to the CAD tools. Implementation of model in CAD tools requires various model parameters related to device under consideration. Parameter extraction for nonlinear model is complex process. It starts with de-embedding of test structure from the device, extraction of intrinsic and extrinsic parameter for small signal device model, extraction of parameter from DC I-V (current-voltage) measurements. These steps need s-parameter measurement at various condition and DC I-V measurements. Nonlinear Model implementation is multiple steps process to extract the parametric values of model. Error at a pervious stage impact the accuracy of latter stage process by introducing an error. Number of methodology are available to complete the extraction process at each step by different author focusing at single step or part of step.

Convergence of model in design tools while simulating a design is also dependent on model parameters. For practical design of circuits, fast convergence of model in simulator is one of essential requirement. Accurate parameter extraction and slight tuning/optimization of parameter are required to make model to converge in CAD tools [1] [2].

Implementation of nonlinear model in design tools requires lot of effort and multiple skills like programming, measurements and design expertise, without using proprietary model parameter extraction tools (IC-CAP, AmCAD, etc.) which are very costly [3].

Aim of this work is to integrate all steps required for model parameter extraction by choosing best suited method/equation to device under practical consideration and ease to implement it in CAD tools. Model parameter extraction program are developed in MATLAB which are also usable with open source alternative of MATLAB with slight modification. By using this methodology user have more control over model parameter extraction process as compared to above mentioned proprietary tools. Curtice cubic model is selected as nonlinear model for this work which is present in ADS as one of standard model. Curtice cubic model is also supported by the open source CAD tools Qucs, QucsStudio and other CAD tools. Validation of implemented model in ADS is done by comparing simulated data from model and measured data from device. Implemented model is used for design of nonlinear medium power amplifier (MPA) to evaluate convergence of model during circuit simulation in ADS. This presented framework is also useful for pHEMTs devices. A 5-5.5GHz amplifier has designed using the implemented model, find application in various communication module having requirement for radiation hardening and have to operate in higher temperature environment.

2. DEVICE DESCRIPTION

In this paper we use LN G7A MESFET device with 0.7µm gate length with gate is shifted 1µm towards source. Gate width of the device is 2×150µm. This device is fabricated in house at GAETEC. G7A process is based on ion implanted depletion mode technology for MESFETs with recessed gates. The process uses 8 mask during fabrication and contact lithography. The process starts with 3 semi-insulating GaAs wafer having 625µm thickness and finally wafer is thinned down to 200±20µm thickness. The wafer is metallised with gold on the backside. The MESFETs are isolated from external environments like moisture using passivation with nitride 1.

3. MODEL PARAMETER EXTRACTION FRAMEWORK

3.1 DE-EMBEDDING PROCEDURE

The layout of the test structure is converted in to the equivalent circuit, short and open RF measurement data is used to calculate the value of the impedances and admittances (Z_1, Z_2, Z_3 and Y_1, Y_2, Y_3). This procedure includes first subtracting out the on wafer open *Y*-parameters shunting the input and output ports, next subtracting out the *Z*-Parameters taken from the on wafer shorts, and finally subtracting the coupling capacitance between the input and output lines [4]. *S*-parameters for Short RF measurement is converted in to Z parameters and Z_1, Z_2 and Z_3 is calculated as:

$$Z_1 = Z_{11} - Z_{12};\ Z_2 = Z_{22} - Z_{12};\ Z_3 = Z_{12} \quad (1)$$

A function is developed in Matlab for this purpose.

3.2 EXTRACTION OF THE PARASITIC RESISTANCE AND INDUCTANCE

Extraction of the parasitic resistance and inductance is done using condition $V_{ds} = 0$, V_{gs} is forward biased. In this condition the C_{pg} and C_{pd}, parasitic capacitance is negligible and consequently the extrinsic Z parameters are determined by adding the parasitic resistance R_s, R_g, R_d and inductances L_g, L_s, L_d to the intrinsic Z parameters [5] [11]. The study then obtains the Eq.(2) - Eq.(4).

$$Z_{11} = R_s + R_g + \frac{R_c}{3} + \frac{nkT}{qI_g} + jw\left(L_s + L_g\right) \tag{2}$$

$$Z_{12} = Z_{21} = R_s + \frac{R_c}{2} + jwL_s \tag{3}$$

$$Z_{22} = R_s + R_d + R_c + jw\left(L_s + L_g\right) \tag{4}$$

If we know the value of the channel resistance R_c we can easily get the value of the R_s using the real part of Z_{12} or Z_{21}, consequently we will get valve of R_d from Z_{22} and R_g from Z_{11}. Channel resistance (R_c) is calculated by [6] or [10]. Method given by Brady et al. [6] uses s parameter for extraction as compared to method given by Fukui [10] which require extra measurement set-up. For this framework Method given by Brady et al. [6] is selected to simplify the process of extraction of parasitic resistance. A function is developed for determining the value of the R_g in Matlab.

3.3 EXTRACTION OF THE CPG AND CPD

In Dambrine method [5], two identical capacitors were used to describe the depletion-layer extension under the gate. White et al. [14] proposed an improved pinched-off cold-FETs method. They used three identical capacitors to represent the depletion-layer extension under the pinched-off cold-FETs bias condition. However, the method cannot precisely explain the physical depletion-layer distribution because the physical geometry of the gate is not identical to those of the source and drain in real FET. LNG7A device has gate 1µm towards source so consideration of charge distribution under gate is important because it create a condition which makes the charge distribution under gate more far away from assumption of equal distribution under gate assumed in Dambrine method [5]. Unreasonable configuration for the intrinsic capacitors would lead to non-physical results of parameter extraction for FET equivalent circuits. Different capacitors are desirable to represent the intrinsic depletion layer of a pinched-off cold-FET [7]. we have gone through the method [5] and [8] for determining the values of C_{pg} and C_{pd} and methodology given by Ooi et al. [8] which consider the above discussion and take alpha (α) a weighing factor to relate the three different capacitors which has been used for this work.

$$C_{pg} = \mathrm{Im}\left(Y_{22}\right) + \frac{2\,\mathrm{Im}\left(Y_{12}\right)}{w} \tag{5}$$

$$C_{pd} = \mathrm{Im}\left(Y_{22}\right) + \left(1+\alpha\right)\frac{2\,\mathrm{Im}\left(Y_{12}\right)}{w} \tag{6}$$

3.4 EXTRACTION OF INTRINSIC PARAMETER

Intrinsic parameters extraction given by Dambrine et al. [5] is providing good fit up to 5 GHz. In this work intrinsic parameters are extracted by using method presented by Manfred Berroth et al. [12], which provides broad-band fit of measured s-parameters with simulated *s*-parameters generated from model [9] [13]. Following equation is used for this purpose:

$$C_{gd} = \frac{\mathrm{Im}(Y_{12})}{\omega} \tag{7}$$

$$C_{gs} = \frac{\mathrm{Im}\left(Y_{11}\right) - \omega C_{gd}}{\omega}\left(1 + \frac{\left(\mathrm{Re}\left(Y_{11}\right)\right)^2}{\left(\mathrm{Im}\left(Y_{11}\right) - \omega C_{gd}\right)^2}\right) \tag{8}$$

$$R_i = \frac{\mathrm{Re}\left(Y_{11}\right)}{\left(\mathrm{Im}\left(Y_{11}\right) - \omega C_{gd}\right)^2 + \left(\mathrm{Re}\left(Y_{11}\right)\right)^2} \tag{9}$$

$$g_m = \sqrt{\left(\mathrm{Re}\left(Y_{21}\right)\right)^2 + \left(\mathrm{Im}\left(Y_{21}\right)\right) + \left(\omega C_{gd}\right)^2\left(1 + \omega^2 C_{gs} R_i^2\right)} \tag{10}$$

$$\tau = \frac{1}{\omega}\arcsin\left(\frac{-\omega C_{gd} - \mathrm{Im}\left(Y_{21}\right) - \omega C_{gs} R_i\,\mathrm{Re}\left(Y_{21}\right)}{g_m}\right) \tag{11}$$

$$C_{ds} = \frac{\mathrm{Im}\left(Y_{22}\right) - \omega C_{gd}}{\omega} \tag{12}$$

$$g_{ds} = \mathrm{Re}\left(Y_{22}\right) \tag{13}$$

3.5 EXTRACTION OF NONLINEAR PARAMETER FROM DC I-V CHARACTERISTICS OF DEVICE

To implement the nonlinear model in ADS, Curtice-Cubic GaAsFET Model is selected as basis model.

$$I_{ds} = I_{dso} \times \tanh(\gamma \times V_{ds}) \tag{14}$$

$$I_{dso} = [A_0 + A_1 \times V_1 + A_2 \times V_{12} + A_3 \times V_{13}] + (V_{ds} - V_{dsdc})/R_{ds0} \tag{15}$$

where, I_{ds} is DC drain to source current, Gamma is current saturation, A_0 to A_3 are cubic polynomial coefficient for I_{ds}, V_{ds} is drain to source voltage, V_{dsdc} is V_{ds} at which R_{ds0} is measured, R_{ds0} is DC drain to source resistance at $V_{gs} = 0$ [12]. This is slightly modified Curtice-Cubic model, used to extract the model coefficient by fitting the measured dc I-V data of device under consideration using curve fitting tools. Extracted parameters are used to implement the device model for simulation of the device behaviour in ADS design CAD tools.

3.6 IMPLEMENTATION OF NONLINEAR MODEL IN ADS DESIGN CAD TOOLS

Curtice-Cubic model is available as standard model in ADS. Small signal model parameters and nonlinear parameters extracted from the DC I-V characteristics of device under consideration is used to implement this model in ADS as shown in Fig.1.

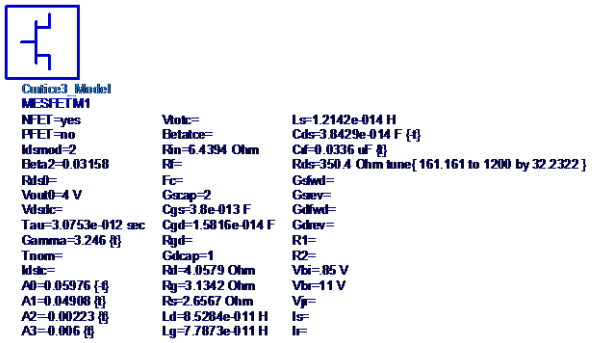
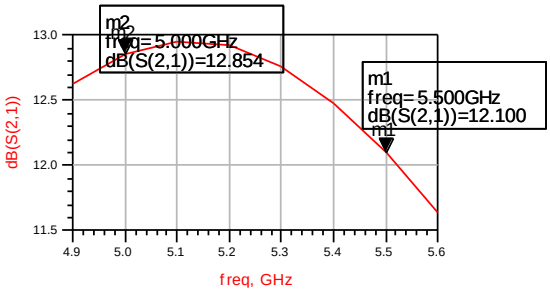


Fig.1. Curtice-Cubic model implementation in ADS with extracted parameters for device LN G7A 2×150µm

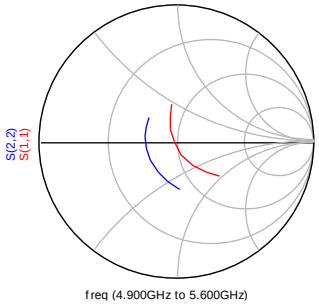
3.7 ASSESSMENT OF MODEL CONVERGENCE FOR NONLINEAR CIRCUIT DESIGN

Model convergence during simulation of circuits in CAD tool is one of important requirement. To assess convergence of model, 5-5.5GHz medium power amplifier is designed using load pull simulation of implemented model. No convergence issue is occurred during simulation of amplifier and simulation result is presented in Fig.2(a), Fig.2(b), Fig.3(a), Fig3(b), and Fig.4(a), Fig.4(b). Simulated output power at 1 dB compression point for amplifier is 16.5dBm and gain is 11.77dB as shown in Fig.5. This amplifier finds the application in ad-hoc wireless sensor network and communication having requirement to operate the system in high temperature environment.

The Fig.2 to Fig.5 show that the model has no convergence issue during nonlinear circuit design process in CAD tools using implemented model, otherwise the simulation process halt without meaningful simulation result.

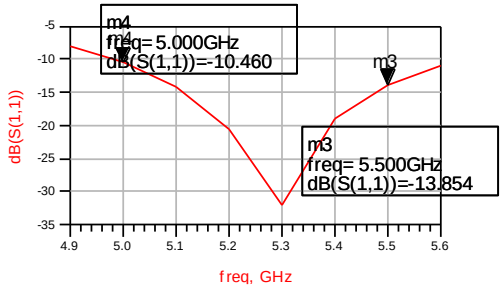


(a)

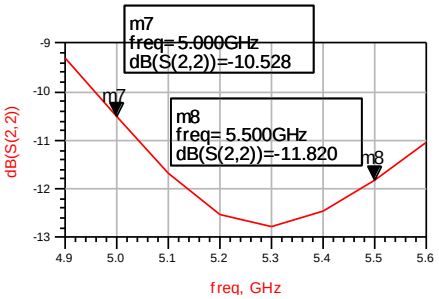


(b)

Fig.2(a). Simulated gain (S_{21}) (b) shows the simulated S_{11} and S_{22} match for designed circuit after matching the simulated load after load pull of implemented model impedance with 50Ω load and input impedance match

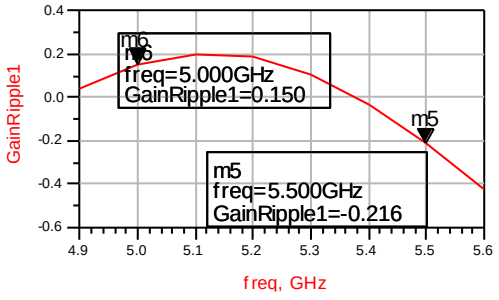


(a)

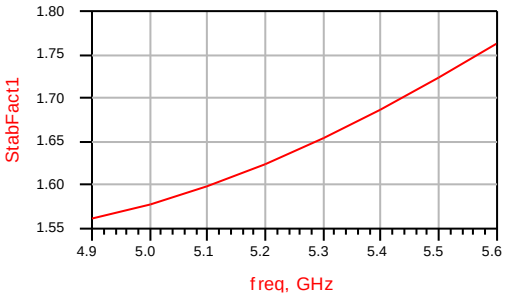


(b)

Fig.3. (a). shows the Simulated Input return loss(S11), (b). shows the Output return loss (S22) of the 5-5.5GHz amplifier simulated using implemented model



(a)



(b)

Fig.4. (a). Simulated Gain ripple and (b). Stability factor for amplifier with respect to frequency

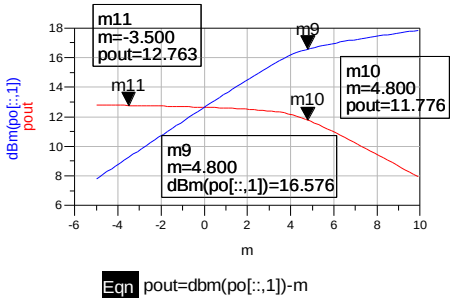
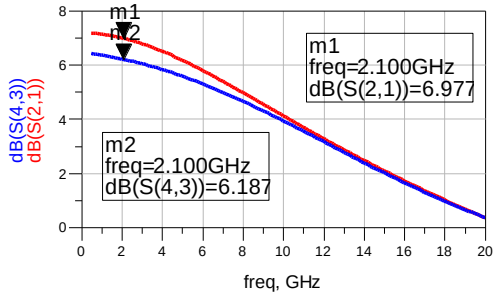


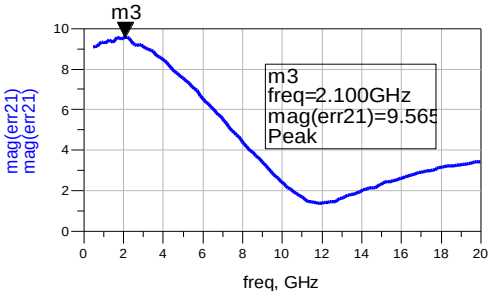
Fig.5. p_{out} is gain in dB and p_o is output power in dBm simulated for power amplifier using implemented nonlinear model

4. COMPARISON, VALIDATION AND DISCUSSION

To validate the implemented model, the small signal s-parameters at $I_{dss}/5$ (I_{ds} is drain to source current at V_{gs}=0), S_{21} (blue line) measured data is compared with the simulated S_{43} (red line) in Fig.6(a), the percentage of error between simulated and measured data is plotted in Fig.6(b) with respect to frequency. Similarly input return loss, measured data S_{11} (blue line) and output return loss, S_{22} (blue line) are compared with the simulated input return loss S_{33} (red line) and S_{44} (red line) respectively in Fig.7(a) and Fig.8(a). In Fig.7(b) and Fig.8(b) the percentage of error between simulated and measured data is plotted w.r.t frequency. The percentage of error between the simulated data and measured data is below 10.3% for frequency from 500MHz to 20GHz. In Fig.9 I_{ds} measured current is compared *with* I_{dss} model (Curtice-cubic) current. Error are within the range and model is useful to simulate the design as demonstrated by design of 5-5.5GHz Medium Power Amplifier (MPA).



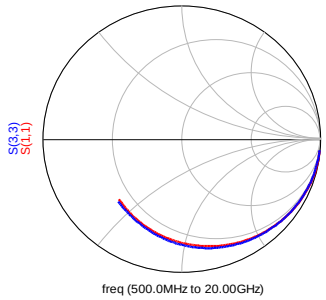
(a)



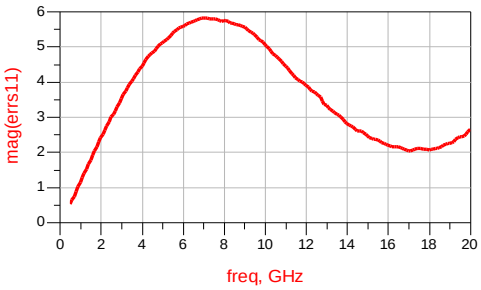
(b)

Fig.6. (a). Comparison of measured gain S_{21}(red line) with simulated gain S_{43} (blue line), (b). percentage of error between simulated and measured gain with respect to frequency

For fabrication process of device, 10% of process variation is normal due to various fabrication factor affecting the process parameters for different run (batch) of wafer. The Fig.6 to Fig.9 show that measured and simulated result are close or below to 10%. Model accuracy is close to process variation so model is useful for simulation of circuits in CAD tools.

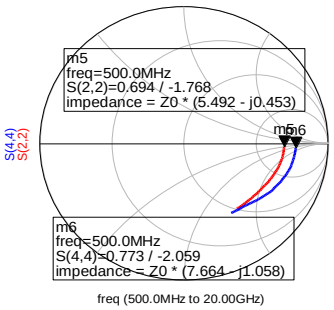


(a)

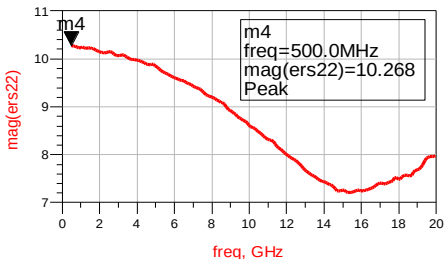


(b)

Fig.7. (a). Comparison of measured input return loss S_{11} (red line) with simulated gain S_{33} (blue line), (b). percentage of error between simulated and measured input return loss with respect to frequency



(a)



(b)

Fig.8. (a). Comparison of measured output return loss S_{22} (red line) with simulated gain S_{44} (blue line), (b). percentage of error between simulated and measured output return loss with respect to frequency

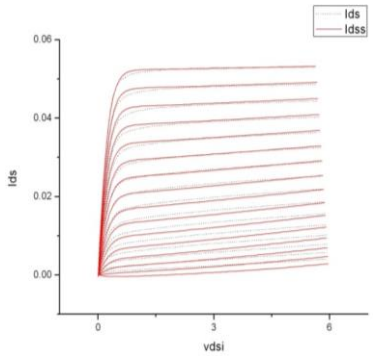


Fig.9. Comparison of measured (black doted) drain to source current (I_{ds}) data with simulated (red continuous) current

5. CONCLUSIONS

Nonlinear model is implemented in ADS CAD tools. The framework for implementation of nonlinear model starting from the de-embedding of test structure, extraction of intrinsic and extrinsic parameters of device and extraction of nonlinear parameters from DC I-V currents is presented. During selection of the methodology at each step the suitability of method for device and nonlinear application of device are considered. The percentage of error for implemented model is within the process variation of fabrication. This model will be useful for simulation of various nonlinear circuit prior to fabrication. This model is used to simulate the 5-5.5GHz MPA that show that no convergence issue has halted the process of circuit simulation. This amplifier find application in ad-hoc wireless sensor network and communication having requirement to operate the system in high temperature environment due to use of wide band gap material (GaAs) used for MESFETs device under consideration. GaAs has also radiation hardening, so circuit using this device is useful for space communication systems.

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