ISSN: 2395-1680 (ONLINE)
DOI: 10.21917/ijme.2019.0142

ANALYSIS OF SURFACE POTENTIAL MODEL DEVELOPED FOR BALLISTIC PLANAR CNTFET OPERATED WITH CNT DIAMETER VARIATION

S. Balaji Ramakrishna[1] and A.R. Aswatha[2]
[1]*Department of Electrical and Electronics Engineering, Dayananda Sagar College of Engineering, India*
[2]*Department of Electronics and Telecommunication Engineering, Dayananda Sagar College of Engineering, India*

Abstract
Carbon nanotube based devices are foreseen as the vital candidates for fabricating high-performance logic blocks that can be operated in the sub 22nm regime. Unlike their silicon-based counterparts, these CNTFET devices can be operated without getting affected by short channel issues of downscaled technology. In this work, an analytic model based on surface potential of the ballistic planar CNTFET device is developed and a simulation study is carried out to examine the current-voltage characteristics of the device. The developed MATLAB model also investigates the stability of the device performance under the variation of CNT diameter and oxide thickness used for the device. The model generates optimal I-V characteristics of the device that possess a negligible off-state current even under an increase in temperature. The obtained current values are compared with the simulation results of the nanoHUB Fettoy simulator for the validation of the developed model. The characteristics demonstrate the compatibility of the device to design high-performance circuits.

Keywords:
CNTFET, Device Model, Surface Potential, On-State Current, Analytic Model

1. INTRODUCTION

The research of nano-electronics is moving towards the fabrication of high-performance circuits suitable for high-speed data computation and memory design. To create the necessary technology it is needed to quantify the performance nano-devices such as CNTFET with existing CMOS technology in the nano regime in the order of 22nm and less than that in regards to power dissipation, speed, and transistor integration. The performance of CNTFETS can be further improved by arriving at new physical concepts that are modeled to obtain optimal device characteristics.

The devices with shorter channels and better performance characteristics are the focus of nano-electronic research in recent past and such device fabrication benefits to meet the challenging needs of today's technology as per Moore's prediction of IC technology evolution. The scaling of devices less than 22nm was a foremost challenge in the CMOS regime due to the effects of tunneling of carriers through the gate oxide and also through the body slipping from source and drain regions. Even though the challenges of short channel effects were addressed to an extent by adopting appropriate doping techniques, it is always harder to obtain optimal device current ratios in conventional MOS devices under continued downscaling. It is because of the above limitations the semiconductor industry is looking to explore novel nano-devices such as CNTFET in order to address the existing challenges.

The CNTFETs are found to be a favorable alternative to conventional MOS devices due to their metallic and semiconducting properties and their ability to function with high currents through ballistic transport of carriers. The metallic behavior of CNTFETS is extensively engaged in making interconnects while semiconducting behavior is employed for devices [1]. This paper proposes an accurate model based on the surface potential of ballistic CNTFET with the single-walled tube to investigate the device performance based on drain currents under variation of chiral ratios and insulating gate oxide thickness [12]. Since the Structure of CNTFET is similar to that of the MOSFET device and it is able to build PCNFET and NCNFET like conventional devices suitable for building logic structures, the topic of modeling of CNTFETS is gaining attention in recent past.

The need of the day is to explore the vital parameters of device physics of CNTFET such as device quantum capacitance and carrier transport mechanism. The two main methods to study the CNT device are (i) Non-equilibrium Green's function (NGEF) approach and the Ballistic transport mechanism approach [1]. The NGEF approach is quite iterative and has limitations w.r.t to model the device to study its suitability for circuit simulation whereas the ballistic transport mechanism supports the modeling of the device and the IV and CV characteristics can be explored. In this work, it has been focused on the surface potential of the CNT to examine the charge developed and in turn the flow of current in the CNT. In CNTFETs, The current flow can be precisely controlled by reducing the barrier width between source and drain regions and it can be maintained constant throughout the CNT [2]. The device can be made to work with ballistic transport of carriers if the channel length is less than the mean free path of the carriers [3]. The described mean free path for CNT is typically 200 nm and its band structure makes it possible to have the carrier transport inside the CNT as near ballistic [4]. Due to these factors, the reduced channel length is not a disturbing criterion in CNTFET devices, however, the chirality of the tube selected and power supply plays a vital role in the charge transport mechanism. Also, the chiral ratio selected will influence the threshold voltage which is a major advantage to regulate the power of operation of the device. The threshold voltage of CNTFET is not dependent on channel length like in the case of MOS devices [5]; this makes the device supportive for downscaling. The diameter of CNT will influence the off-state current, bandgap and oxide capacitance of the device. Owing to the above motives it is important to select proper CNT diameter and oxide thickness to study the ballistic mechanism. The on-state current in this ballistic device depends on the number of CNTs used and its distribution [6].

The proposed surface potential model is developed for planar MOSFET like CNTFET with semiconducting CNTs of diameter ranging from 1nm to 4nm and length up to 500nm. The oxide thickness is also varied between 1nm to 4nm to investigate the

effect on the model. IV and CV characteristics are studied and compared with the results obtained in [9].

The model demonstrates the characteristics depicting the robustness of ballistic transport even under diameter variation and oxide thickness variation. This surface potential analysis is not applicable for devices with armchair tubes as the approximation is based on ballistic transport of charge carriers. In section 2, the background literature of CNTFETs is presented. The proposed model and results are elucidated in further sections.

2. CARBON NANOTUBE DEVICES

The carbon nanotube structure can be geometrically visualized as the cylindrical graphene layers with carbon atoms at the edges of a tubular structure. The bonding of carbon atoms is responsible for the semiconducting or metallic properties of the CNT. In Fig.1 the graphene sheet is assumed to be finite in the direction of *Ch* vector and infinite in an orthogonal direction to that of i.e. CNT can be visualized as rolling of the sheet in the direction of the vector *T* with unit cell *OAB′B*.

The unit cells of the graphene layer are defined by the lines a_1 and a_2 as depicted in Fig.1.

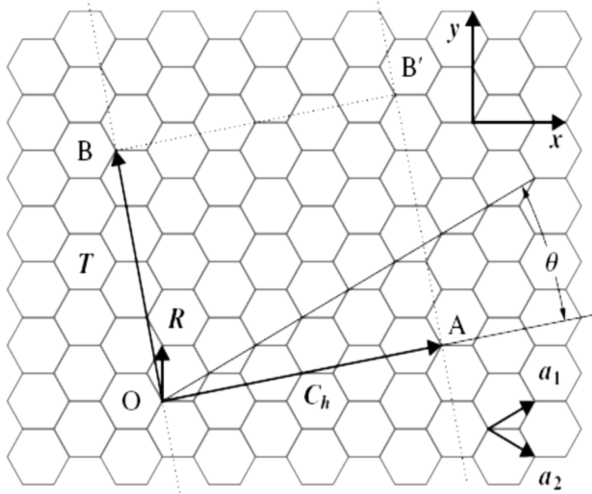

Fig.1. Graphene ribbon

Let the chiral indices of the CNT are *n* and *m* to attain the diameter. The relation to obtaining CNT diameter is illustrated in Eq.(1).

$$d = \frac{a_{cc}\sqrt{3\left(n^2+m^2+nm\right)}}{\pi} \tag{1}$$

where, a_{cc} is 1.44Å is the distance between the nearest adjacent carbon atoms in graphene sheet and numerals *m* and *n* are selected such that always $0 \leq m \leq n$. The angle θ is made between the vectors *Ch* and projected vector a_1. This angle is very important in measuring the electronic properties of the selected single-walled carbon nanotube for the given chirality. The angle is defined in Eq.(2).

$$\cos\theta = \frac{2n+m}{2\sqrt{\left(n^2+m^2+nm\right)}} \tag{2}$$

$$d = \frac{a_{cc}}{\pi\sqrt{\left(n^2+m^2+nm\right)}} \tag{3}$$

In [8], the diameter of the tube is obtained by the relation in Eq.(3) with a_{cc} is 2.49Å by considering the effect of elastic scattering on the channel length and for non-ballistic transport. Depending on the requirement of device modeling the single-walled carbon nanotube SWCNT is synthesized for metallic or semiconducting properties. The two prominent types of CNTs employed are armchair nanotubes and zig-zag nanotubes whose chiral values are (*n*,*n*) and (*n*,0) respectively i.e. for the armchair tubes both the indices are of same value whereas for zigzag tubes index n is varied by fixing the index $m = 0$. Based on this method for the depicted graphene layer in Fig.1, the nanotube is synthesized by joining translational vector (*T*) OB and chiral vectors (*Ch*) OA in order to form a rectangle *OAB′B* which defines the unit cell for the nanotube. In the hexagonal lattice of the tube, the electrical property is attained with the relation of indices ($n-m=3i$), where, if *i* is an integer the tube shall have metallic properties and the tube will be semiconducting for the non-integer value of *i*. Hence by the above relation, all zigzag tubes yield the semiconducting properties suitable for developing the devices.

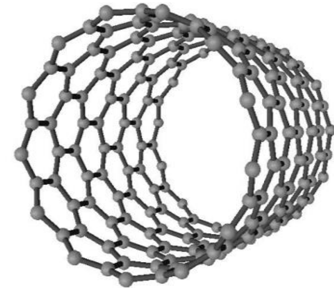

Fig.2. A Semiconducting zigzag nanotube is drawn using [15] for chiral indices (*m*=0, *n*=13)

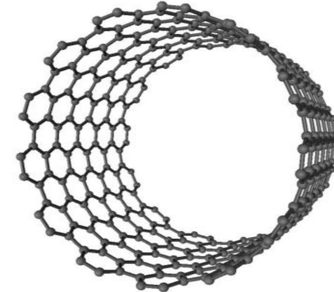

Fig.3. An armchair nanotube is drawn using [15] for chiral indices (*m*=13, *n*=13)

The Fig.2 and Fig.3 represent the semiconducting and metallic SWCNTs respectively whose difference can be observed at the edge of the tube w.r.t. bonding of carbon atoms. These tubes are used as a channel of charge carriers in a CNT device. Multiwalled Carbon nanotubes MWCNTS are normally preferred to be used as interconnect in circuits for improved performance [5]. There are mainly two types of CNTFET devices employed which are becoming the substitutes of MOS device (i) Planar MOSFET like CNTFET and (ii) Schottky Barrier CNTFET (SBCNTFET) [7] [13] illustrated in Fig.4 and Fig.5. In planar CNTFETs, the source and drain regions are heavily doped and the current in the channel can be controlled with control over gate potential similar to that of a conventional MOSFET operation.

These devices offer higher on-state current for even a low gate potential. The Fig.4 represents the band structure of planar CNTFET. The structure is one dimensional and helps for ballistic transport of carriers in the CNT. The current is independent of the length and diameter of SWCNT considered [1].

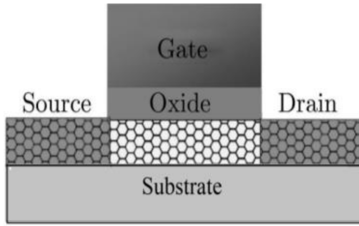

Fig.4. Planar CNTFET suitable for ballistic transport

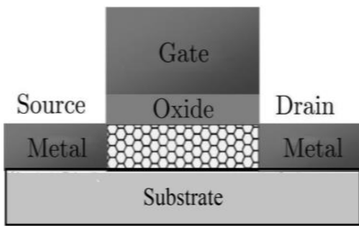

Fig.5. SB-CNTFET

In SBCNTFET depicted in Fig.5, the source and drain regions are shaped by metals and a Schottky barrier exists between the diffusion regions and the CNT. The channel current which is dependent on the width of this barrier. The Fig.6 represents the band structure of SBCNTFET. The barrier height is maintained by controlling the gate bias and during the unbiased state, the Schottky barrier height is needed as half of the bandgap.

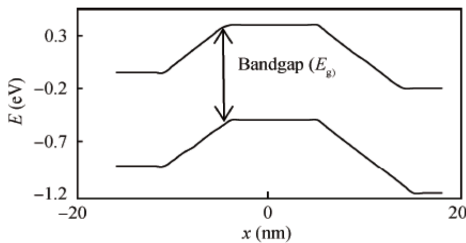

Fig.6. Planar CNTFET suitable for ballistic transport [1]

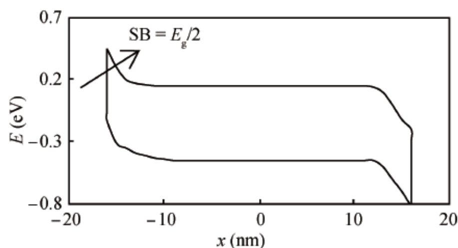

Fig.7. SB CNTFET bandgap [1]

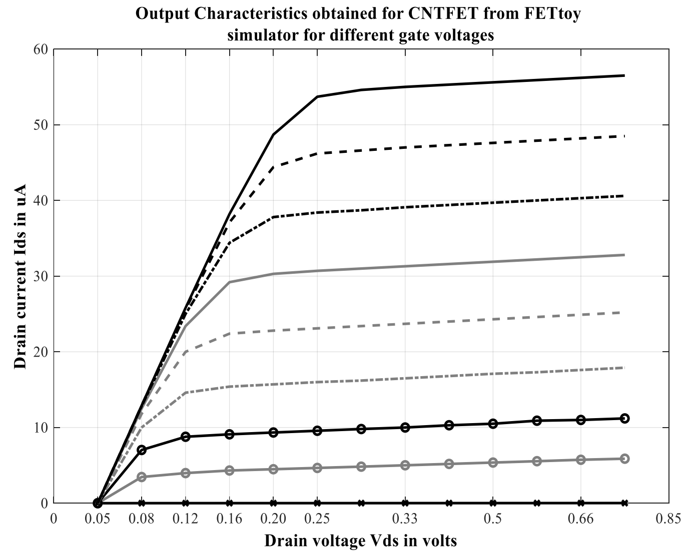

Fig.8. Output characteristics of planar CNTFET simulated with [9] for different gate voltages

Due to the semiconducting property of the device, the planar CNTFETs offer a wide range of advantages like a MOS device and also good in the elimination of the parasitics.

The device offers excellent I-V characteristics even for the lowest power supply such as 1volt as depicted in Fig.8. It is simulated using [9] with CNT diameter 1nm and oxide thickness 4nm and a pitch of 20nm. The device current saturates around 60μA for a low voltage of less than 1V. Hence it will enhance the current driving capability of the design under consideration. They can be used to build multifaceted CNTFET based circuits, thus can be suitable for low voltage, low power, and high-speed applications. Also, the device offers a denser capacitance effect to yield electrically robust performance compared to conventional MOS devices.

3. PROPERTIES OF BALLISTIC PLANAR CNTFET

The ballistic CNTFET devices possess identical structures to that of the MOS device except that a CNT acting as channel material. The evolution of the CNTFET structure suitable for the nano regime is offering extremely efficient behavior. The analytical model developed in this work is focused towards the surface potential of the CNT, The normalized surface potential is assumed as the difference of surface potentials of drain end and source end. The applied gate voltage is used to regulate the energy band of the carbon nanotube device and thereby controlling the drain current. The current is also dependent on the chirality of the tube and the same is validated through the model developed. The various capacitances of the model considered are depicted next.

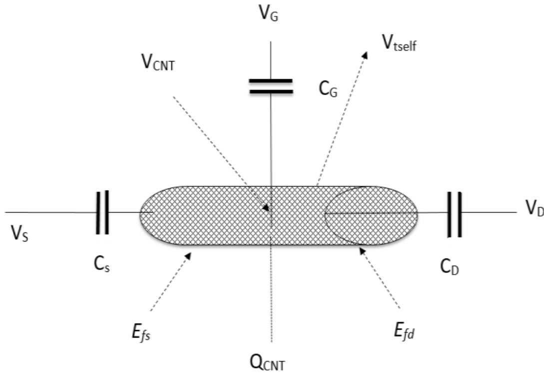

Fig.9. Capacitance Model for ballistic CNTFET

The charge present in the nanotube is determined by the local carrier density and Fermi levels of source and drain represented as E_{fs} and E_{fd} respectively. The amount of self-consistent potential at the top of the barrier V_{tself} is also an important empirical in calculating the drain current. By maintaining the surface potential at zero volts, the drain current is obtained using the relation 3 of [1] [14].

$$I_d = \frac{4qkT}{n}\left\{\ln\left(1+e^{E_{fs}-V_{tself}}\right)-\ln\left(1+e^{E_{fd}-V_{tself}}\right)\right\} \tag{4}$$

where, k is Boltzmann's constant, h is Planck's constant and T is the temperature maintained at the surface of the tube. The drain current is determined for different values of V_G and V_D. For the ballistic planar CNTFET, the charge and current will remain constant in the channel across the length. In the proposed model we vary the diameter to validate the device performance, as the diameter of the tube directly impacts the threshold voltage and carrier concentration.

The potential developed across the CNT is given by:

$$V_{CNT} = V_G - \frac{Q_{CNT}}{C} \tag{5}$$

where, C is the equivalent capacitance given by $C=C_{ox}+C_D+C_s+C_{sub}$ [1]. In this work the electrostatic model is considered through only three capacitances C_D, C_S and C_G and Q_{CNT} is given by

$$Q_{CNT} = \frac{e}{2} n_{CNT} \exp\left(\frac{V_{CNT}}{kT}\right)\left[1+\exp\left(\frac{-V_{ds}}{kT}\right)\right] \tag{5}$$

In Eq.(5) is the charge of electron and k is Boltzmann constant and T is operating temperature, also we can confirm that the charge developed in the nanotube will increase tremendously with the voltage across it and can be controlled with the drain voltage. The surface potential model is analyzed using the above equations and IV characteristics of the device is obtained.

4. ANALYTICAL MODELLING

In this work, A MATLAB model is characterized and analyzed based on the surface potential method to attain the CNTFET device characteristics. The on-state current is measured with respect to variation in gate voltage and CNT diameter. It is compared with the nanoHUB FETtoy model [16]. The Fig.10 represents the flow of the proposed model. We have selected different chiral vectors for the single-walled CNT and programmed the device equations. Table 1 describes the voltages attained in the model for V_{Gs} and V_{CNT}.

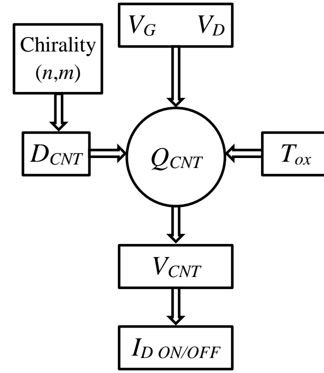

Fig.10. Flowchart of the proposed model

The surface potential will not be linear parameter w.r.t to the gate bias voltage. From, Table.1 it is apparent that voltage across the tube gets saturated after $V_{GS} > 0.6$. In the proposed model the drain current is calculated according to the selected chirality which is dependent on the conduction band minima. The current in the CNTFET increases with an increase in diameter. We attain this by controlling the Fermi levels of Eq.(3). The varied V_{CNT} is obtained with different chirality values such that d=1nm to d=4nm is employed. The oxide thickness is also varied up to 4nm and observed the effect on the surface potential. The model delivers an operating current of 150uA for the maximum gate bias. The plot of gate oxide thickness T_{ox} vs. drain current I_D is depicted in Fig.11.

Table.1. V_{GS} vs. V_{CNT} for different drain potentials

V_{GS} (Volt)	V_{CNT} (Volt)		
	V_D=0	V_D=0.8	V_D=1
0	0	0	0
0.2	0.201	0.211	0.230
0.4	0.351	0.351	0.345
0.6	0.501	0.520	0.570
0.8	0.611	0.656	0.671
1	0.624	0.658	0.680

From Fig.11, it can be established that there is a reduction of drain current when the gate oxide thickness is increased unto the typical value of 4nm. It can be examined that the model provides a high value of current around 130µA for the gate to source potential of 1V. Lesser the oxide thickness allows an increase in electron charge density thereby increased current; however lesser oxide thickness cannot insulate the gate current. With this, we can infer that the proposed model has appropriate behavior for variation in oxide thickness.

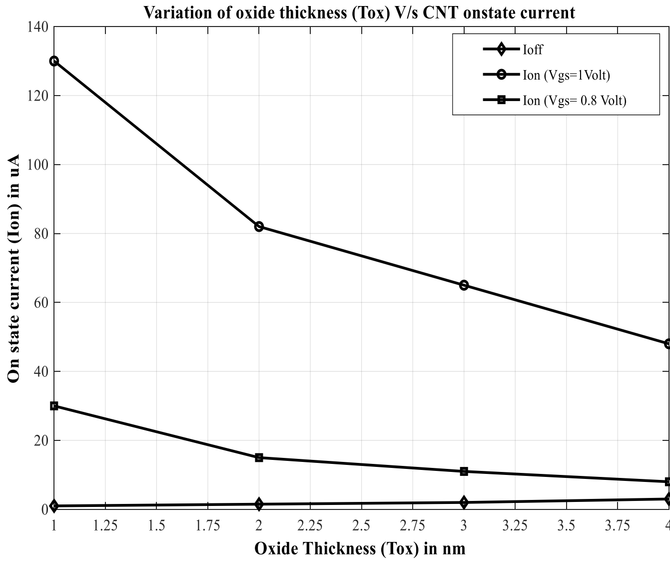

Fig.11. On current metrics for the variation of oxide thickness

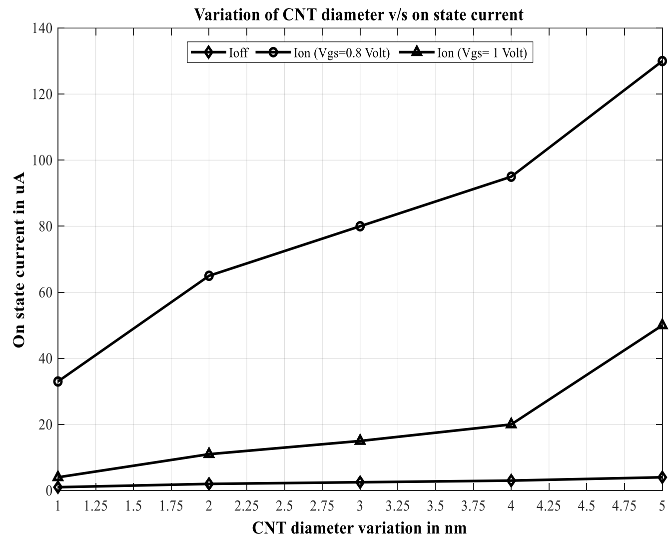

Fig.12. On current dynamics for the variation of CNT diameter

From Fig.12 we can inspect that, with an increase in the diameter the bandgap tends to decrease and it increases the current in the carbon nanotube. The device model can drive higher drain currents for even a smaller gate bias compared to that of the FetToy model depicted in Fig.8 for benchmarking.

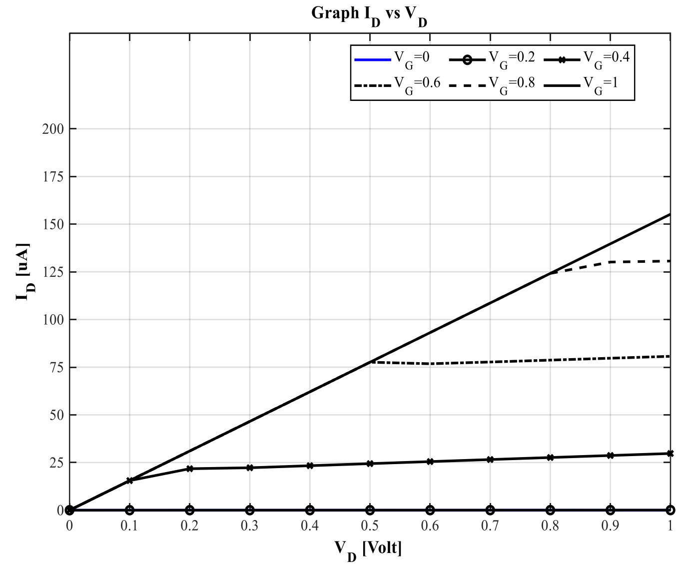

Fig.13. Output drain current magnitude of the proposed model for different gate voltages

The Fig.13 depicts the output characteristics of the proposed model of CNTFET. The maximum drain current of 150μA is obtained for the drain voltage of 1V. This infers that the model has high current driving capability and linearity similar to that of a conventional MOSFET.

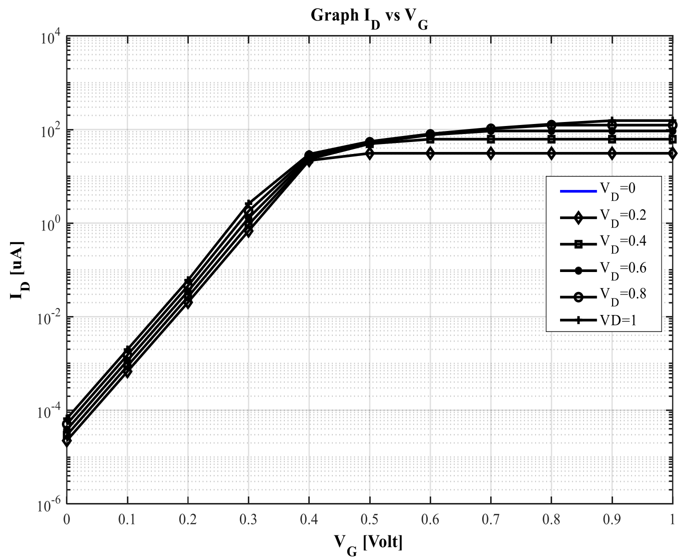

Fig.14. Saturation of drain current for CNT diameter=1nm for different drain potentials

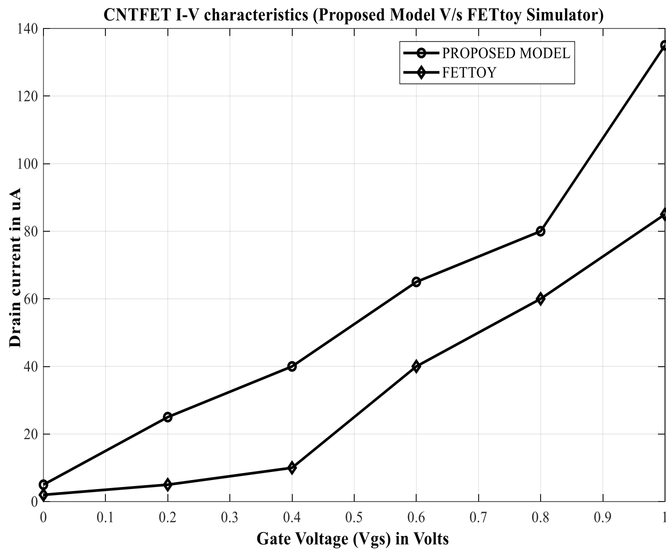

Fig.15. Benchmarking of drain current variation of proposed model vs. Fettoy simulator

The Fig.15 compares the proximity of the current magnitude for the standards of [16] and the proposed surface potential model. It demonstrates that the model delivers a high on-state current for a low power supply of 1V and hence the surface potential model is successfully validated for the same device parameters specified in section 2.

5. CONCLUSION

This work presents the surface potential model developed for ballistic CNTFET and authenticates the transport mechanism of carriers with respect to the variation of CNT diameter and oxide thickness. The proposed MATLAB model demonstrates the on-state behavior of CNTFET by exploring the impact of its diameter variation, pitch and oxide thickness under the nano regime. It is evident from the results that the model delivers a high on-state current and pertinent ID-VG and ID-VD Characteristics. The results are benchmarked with the nanoHUB FETtoy simulator so as to make a close agreement for the properness of the model in presenting the advantage of CNTFET device against short channels MOSFETS less than 22nm. The proposed surface potential model provides the relevance of ballistic planar CNTFET operation suitable for future nanodevice based circuits.

REFERENCES

[1] Amandeep Singh, Mamta Khosla and Balwinder Raj, “Compact Model for Ballistic Single Wall CNTFET under Quantum Capacitance Limit”, *Journal of Semiconductors*, Vol. 37, No. 10, pp. 1-12, 2016.

[2] Rahmat Sanudin, “A Simulation Study of Ballistic Carbon Nanotube Field-Effect Transistor”, *Proceedings of IEEE National Symposium on Microelectronics*, pp. 1-7, 2005.

[3] Mostafa Fedawy, Wael Fikry, Adel Alhenawy and Hazem Hassan, “I-V Characteristics Model for ballistic Single Wall Carbon Nanotube Field Effect Transistors(SW-CNTFET)”, *Proceedings of IEEE International Conference on Electronics Design, Systems and Applications*, pp. 115-119, 2012.

[4] Amandeep Singh, Dinesh Kumar Saini, Dinesh Agarwal, Sajal Aggarwal, Mamta Khosla and Balwinder Raj, “Modeling and Simulation of Carbon Nanotube Field-Effect Transistor and its Circuit Application”, *Journal of Semiconductors*, Vol. 37, No. 7, pp. 1-12, 2016.

[5] S. Balaji Ramakrishna and A.R. Aswatha, “CNTFET Modelling and Performance Analysis of Device Characteristics”, *International Journal for Scientific Research and Development*, Vol. 2, No. 11, pp. 21-29, 2015.

[6] Zubair Ahmed, Lining Zhang , Khawar Sarfraz and Mansun Chan, “Modeling CNTFET Performance Variation Due to Spatial Distribution of Carbon Nanotubes”, *IEEE Transactions on Electron Devices*, Vol. 63, No. 9, pp. 3776-3781, 2016.

[7] Mariya Lyubomirova Spasova, Dimitar Nikolov Nikolov, George Vasilev Angelov, Rossen Ivanov Radonov and Marin Hristov Hristov, “Analysis of the Impact of CNTFET Model Parameters on its Transfer and Output Characteristics”, *Proceedings of 25th International Scientific Conference Electronics*, pp. 12-16, 2016.

[8] Safayat Al Imam, Nasheen Kalam and Sharmin Abdhullah, “Temperature Dependence of Carbon Nanotube Field Effect Transistor under Non-Ballistic Conduction Considering Different Dielectric Materials”, *Nanoscience and Nanotechnology*, Vol. 4, No. 3, pp. 52-58, 2014.

[9] Anisur Rahman, Jing Guo, S. Datta and M. Lundstrom, “Theory of Ballistic Nanotransistors”, *IEEE Transactions on Electron Devices*, Vol. 50, No. 9, pp. 1853-1864, 2003.

[10] Sheikh Ziauddin Ahmed, Mashiyat Sumaiya Shawkat, M.D. Iramul Hoque Chowdhury, Sharif Mohammad Mominuzzaman, “Current-Voltage Characteristics of Ballistic Schottky Barrier GNRFET and CNTFET: Effect of Relative Dielectric Constant”, *Proceedings of 10th IEEE International Conference on Nano/Micro Engineered and Molecular Systems*, pp. 233-245, 2015.

[11] Soheli Farhana, A.H.M. Zahirul Alam and Sheroz Khan, “Optimum Performance of Carbon Nanotube Field Effect Transistor”, *Proceedings of World Congress on Engineering and Computer Science*, pp. 22-24, 2014.

[12] Bipul C. Paul, Shinobu Fujita, Masaki Okajima, and Thomas Lee, “A Compact Model of Ballistic CNFET for Circuit Simulation”, *Proceedings of International Conference on Nanotechnology*, pp. 846-849, 2006.

[13] R. Sahoo and R.R. Mishra, “Simulations of Carbon Nanotube Field-Effect Transistors”, *International Journal of Electronic Engineering Research*, Vol. 1, No. 2, pp. 117-125, 2009.

[14] T. Ravi and V. Kannan, “Modeling and Performance Analysis of Ballistic Carbon Nanotube Field-Effect Transistor (CNTFET)”, *Proceedings of IEEE International Conference on Recent Advances in Space Technology Services and Climate Change*, pp. 746-753, 2010.

[15] Chanaka Suranjith Rupasinghe and Mufthas Rasikim, “Ninithi”, Available at: https://nanohub.org/resources/8987/about, Accessed on 2010.