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ERROR COMPENSATION TECHNIQUE FOR 90NM CMOS FIXED-WIDTH AND AREA EFFICIENT BOOTH ENCODING MULTIPLIER

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Abstract

An area efficient, fixed width multiplier using booth encoding is done in this work. The work is further extended to accommodate the error correction feature. As in many signal processing products fast and efficient processing elements are required, the demand increases day by day. This work is one such finding to meet the standard of today's contemporary technology. The proposed methodology suits well for the discrete cosine transform application. A new multiplier architecture using booth encoding is done. The architecture includes a tree based carry save reduction unit with parallel prefix adder and the compensation circuit. The work is carried out in 180nm technology using predictive technology models. The circuits are implemented using SPICE models and the results are obtained. For equal probability the inputs of different blocks are kept '1' or '0' in equal numbers. The frequency of operation is 100MHz. The proposed design will be compared with the existing methods. The robustness will be checked using skewed distribution. The project will be further extended to design for high speed and advanced technology of 90nm in future.

Keywords:

Multiplier, Carry Save Reduction, Booth Multiplier, Error Compensation

1. INTRODUCTION

In many DSP applications, fixed-width multipliers for operating elements must cut out half the output width of the multiplier in internal multiplication which will certainly lead to truncation errors. In fixed-width multiplier literature error compensation methods are developed [1]. But their average mistakes are far greater.

We propose in this article technology modified works for the fixed-width-modified booth multiplier with high precision error compensation circuit. In addition to being symmetrical to the error distribution, the circuit also centralizes the error distribution in zero.

The mean square errors can therefore be reduced significantly simultaneously, so that the resulting fixed-width multiplier [2]-[4] is adapted for various applications whose output data can be generated through one or more multiplier-accumulation operations.

Eventually, the suggested error compensation feature creates a basic compensation loop. The modified Booth encryption, in order to achieve high performance, has been widely used in parallel multipliers, which reduces the number of part products to a factor of two.

2. LITERATURE SURVEY

In [5], the author fixed-width two's complement booth multiplier is proposed. The proposed method provides a smaller area and a lower truncation error compared with existing works.

In [6], the author presented the fixed-width booth multiplier with adaptive low error and in [7], the author proposed a statistical error compensated Booth multiplier and its DCT application.

In [8], the author presented that two designs of low-error fixed-width sign magnitude parallel multipliers and two's-complement parallel multipliers for digital signal processing applications are presented Given two n- bit inputs, the fixed-width multipliers generate *n*-bit (instead of 2*n*-bit) products with low product error, but use only about half the area and less delay when compared with a standard parallel multiplier. In them, cost-effective carry-generating circuits are designed, respectively, to make the products generated more accurately and quickly.

Applying the same approach, a low-error reduced-width multiplier with output bit-width between n and 2n has also been designed. The design of low-error fixed-width sign-magnitude and two's complement multipliers have been presented. By using this type of multiplier, the chip area can be significantly reduced and a little performance promotion is also introduced. In addition, the design strategy has also been applied to designing a reduced-width multiplier, which has lower product error than that of a fixed-width multiplier and still maintains low area complexity.

They are useful in fixed-width data path architectures for multimedia and DSP applications where a uniform or reduced word width is usually required. A similar work is proposed in [9] for a low error reduced width Booth Multiplier for DSP application. A high accuracy and low error carry free fixed width multipliers with low cost compensation circuit is proposed in [10] and [11].

In [12], the author develops a general methodology for designing a lower-error two's-complement fixed-width multiplier that receives two-bit numbers and produces an -bit product. Error-compensation bias to reduce the truncation error and then construct a lower error fixed-width multiplier is proposed, which is area-efficient for VLSI realization. Finally, the work reports the application of proposed fixed-width multiplier to a digital FIR filter for speech processing application. The work is implemented for DCT application in [13] and multilevel approach in [14].

3. THEORETICAL BACKGROUND

Fixed-width multipliers are important components in arithmetical logic units, offer high accuracy, high speed and competitiveness and are suitable for applications involving multipliers in numerous situations. Their high speed and high precision results from a reduction in the number of coding-related partial products. There is therefore less partial products in the truncated part, which leads to greater accuracy. Four methods are used to improve the performances that includes post truncation (P-T), direct truncation (D-T), math probability and computer simulation.

The P-T system measures all partial items using a rounding process with optimum precision, but with a high overhead region and energy consumption and a slow rate of velocity. The D-T approach was developed to solve these limitations by removing the lesser half of incomplete products directly, so that only the greater half is to be measured.

This reduces the area and power consumption, but precision is low. The compensation loop used the linear regression analysis numerical compensation values in the development of the compensation system to reduce the overhead region. Using mathematical methods, such as expected and conditional probability, a more difficult multilevel conditional probability model with a compensation circuit is possible.

Expected probability method achieves higher speed, reduced range and energy costs, but less precision. The conditional probability method, in contrast, provides greater precision, but increases the overall area. The PACS method in this work uses the expected and dependent probability to generate multiple potential solutions based on the row information variable.

The accelerator is used commonly for high speed multipliers. The distortion compressor. The addition of the partial products mostly contributes to the overall delay, area and electricity consumption, with a constant increase in the demand for high speed and low power compressors. Appropriate blocks must be selected for adders.

4. PROPOSED METHODOLOGY

The modified booth multiplier (Fig.1), followed by a parallel Prefix Adder, is implemented via tree based carry save-adder (CSA). The implementation of the proposed PACS is facilitated by three steps.

- *Selection of specifications*: According to the precise application, Word-and column-length information is selected to calculate variables and compensation bias.
- *Compensation circuit design* is summed using CSA tree for finding the compensation bias. The CSA tree is formed of a full or a half adder (HA).
- *MP circuit design*: The CSA tree and the parallel prefix adder sum up all partials in MP and carrying value from compensation to MP. The CSA tree includes 4-2 additional components, FAs or HAs. The 4-2 high-speed adder consists of two FAs, with 4-2 adder prior to FA and HA being higher.

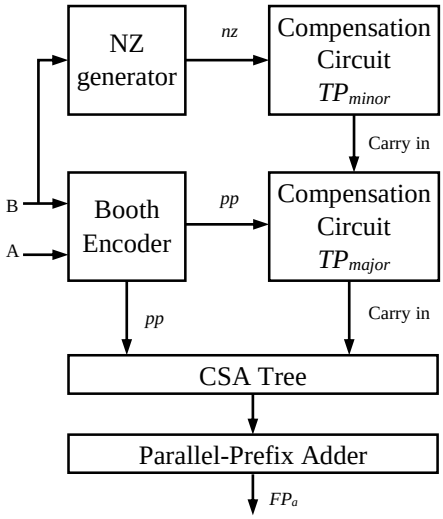


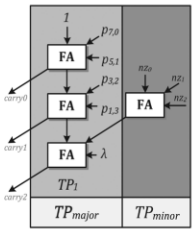
Fig.1. Entire Architecture of Proposed Booth Multiplier

The Fig.2 shows the three offsets in the 8*8 booth multiplier proposed, with w=1, 2, 3. The carriage numbers differ depending on the number of steps; the architecture of MP therefore varies also. Its use of probability and simulation is the most important feature of the proposal PACS.

Firstly, several solutions for the pre-design are generated by the expected probability methods and conditions. Second, SNR simulation selects the pre-design solution with the highest accuracy. The PACS proposed includes an error compensation formula, unlike most simulated designs.

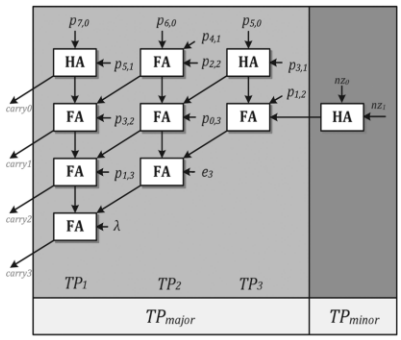
Comparison results demonstrate the P-T method has the highest accuracy but the largest area, delay, and power. The D-T method has the lowest accuracy, and the smallest area overhead, delay, and power.

The P-T method shows the highest precision, but the greatest area, delay and power. Comparison results The D-T system has the lowest precision, overhead, delay and output of the smallest area.



(a)

(b)



(c)

Fig.2. Proposed 8-bit compensation circuits for *w*=1,2,3 (a) *w*=1, (b) *w*=2 (c) *w*=3

5. RESULTS AND DISCUSSION

The different blocks of the block diagram is implemented and tested using Predictive technology models.

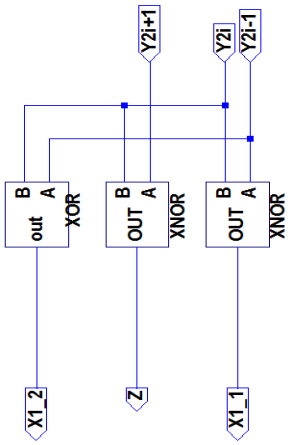


Fig.3. NZ Generator

The proposed method is based on probability and booth encoding. NZ generator is the conditional expected values of partial products. The NZ generator (Fig.3 and Fig.4) performs the exclusive OR exclusive NOR operation between the past, present and the next data. The use of conditional probability makes it possible to estimate the expected value of results.

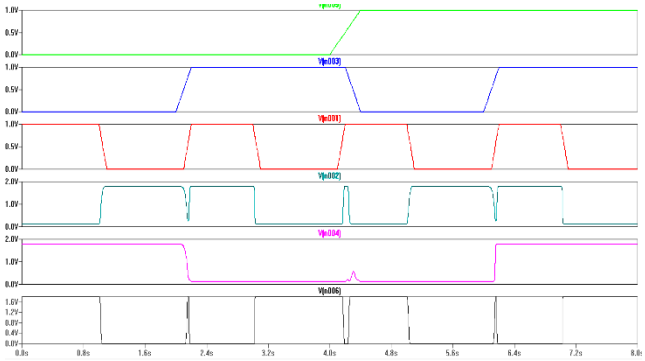


Fig.4. NZ Generator Output Waveform

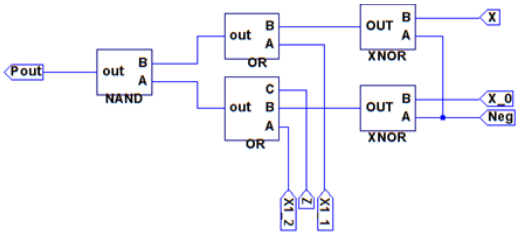


Fig.5. Booth encoder

The Booth encoder (Fig.5 and Fig.6) is designed based on the algorithm which performs the operation in 2s compliment data. The circuit is implemented using Gates XNOR, OR and NAND.

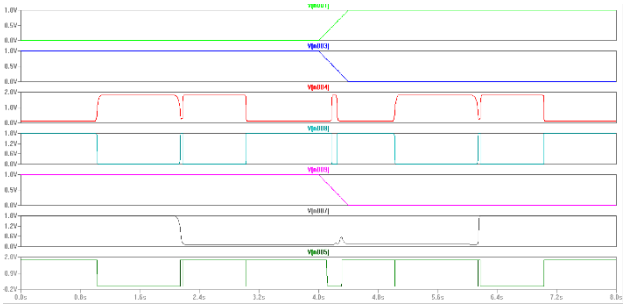


Fig.6. Booth Encoder Output Waveform

The compensation circuit is implemented for error correction happening in probability assumptions. The circuits contains two parts called the Main part (MP) and Truncation part (TP). The TP further called minor and major parts. The expected values provide different solutions but the optimized one is chosen to have better SNR. The value or w determines the SNR value. The expected value of TP (minor) and TP (major) can be calculated according to expected and conditional probability,

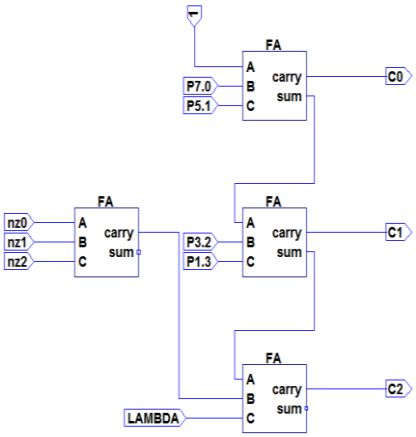


Fig.7. Proposed 8-bit compensation circuits for *w*=1

The compensation circuits (Fig.7-Fig.9) are implemented using a carry-save-adder (CSA) tree to obtain compensation bias. The CSA (Fig.10) tree is implemented using full adder (FA). The w determines the accuracy of the application. It represents the column information. For *w*=2 we have two columns, 7 full adders are required. The first full adder corresponds to the minor circuit. For *w*=3 we have three columns, 9 full adders are required .The first full adder corresponds to the minor circuit. The partial products from the booth encoder and the carry from the

compensation circuit is adder in the carry save adder. The carry save adder is implemented using half adder and full adder. The word length of the carry save adder is dependent on the booth multiplier result length and the value of '*w*'. All of the partial products in MP and carry value from compensation circuit to MP are summed using the CSA tree and parallel-prefix adder (Fig.11). The output from all the CSA blocks are combined in the parallel prefix adder.

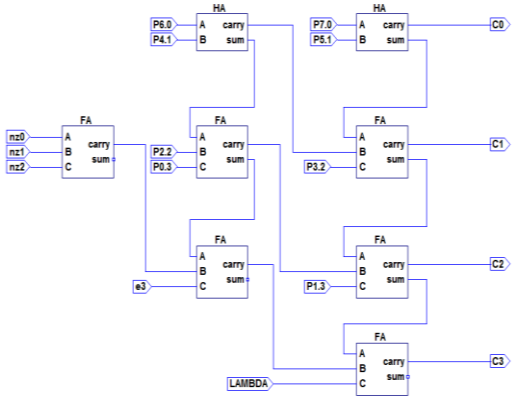


Fig.8. Proposed 8-bit compensation circuits for w=2

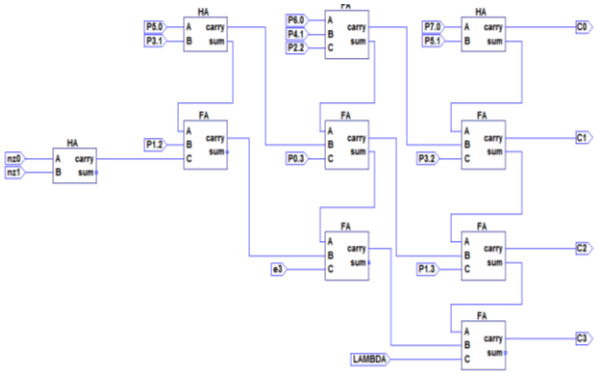


Fig.9. Proposed 8-bit compensation circuits for w=3

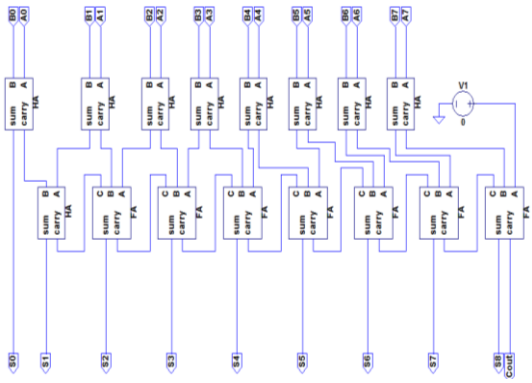


Fig.10. Carry Save Adder

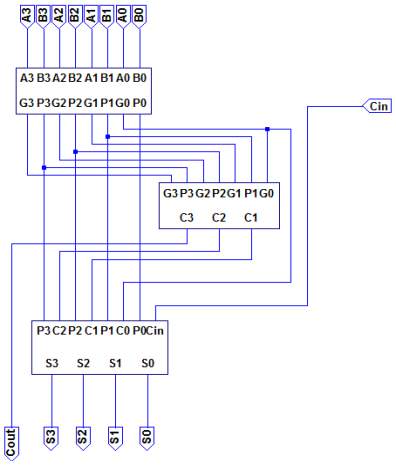


Fig.11. Parallel Prefix Adder

6. CONCLUSIONS

A fixed width, area efficient multiplier architecture using booth encoding is proposed. The architecture incorporates the features of error compensation. The various blocks like partial product generator of booth encoding tree based carry save reduction unit with parallel prefix adder and the compensation circuit are implemented in 180nm technology. For implementation predictive technology models are used in 180nm. The power analysis is done. The work will be further modified for operation frequency above 100MHz. The work will be extended to implement the design in 90nm technology by which the area and power can be further reduced.

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