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POWER GATED TECHNIQUE TO IMPROVE DESIGN METRICS OF 6T SRAM MEMORY CELL FOR LOW POWER APPLICATIONS

Hemant Kumar and Shikha Saun
Department of Electronics, Banasthali Vidyapith, India

Abstract

The SRAM is used in almost every portable device and consumes a considerate amount of device size. Lowering the power dissipation and size of the SRAM memory cell will ultimately lower the average power consumption and size of the digital system. Device scaling is generally used for decreasing the power consumption and the area of the digital system. However, the static power dissipation increases due to device scaling but significant amount of leakage power can be reduced. The low power techniques for SRAM cell implemented in this paper is Power Gating and variations of power gating i.e. using header switch (type 1) and using footer switch (type 2). The purpose of this paper is the application of low power technique in SRAM memory cell to reduce the average power dissipation and simultaneously maintaining the stability of the SRAM memory cells; hence system performance can be improved. The simulation results are carried out using the PTM models for low power on 16nm CMOS technology node using Cadence Virtuoso tool. It can be observed from the result that the power gated SRAM cell exhibits better performance in comparison of conventional 6T SRAM. Depending upon the application, the variations of the power gating technique can be used. The average power dissipated by the power gated SRAM memory cell is 18.07% less than the type 1, whereas it is 15.54% less than type 2. The Write Static Noise Margin (WSNM) of the Power gated SRAM memory cell increases by 3.66% in case of type 1 and 6.17% in case of type 2.

Keywords:

Low Power Technique, Power Gated Scheme, SRAM, Static Noise Margin, Static Power Dissipation

1. INTRODUCTION

The market for portable electronics devices is increasing tremendously. It demands compactness and longer battery life [1], [2]. The SRAM cell is used immensely and consumes large area in system-on-chip (SOC) devices [3] [4]. CMOS technology scaling is used to increase the performance and packing density of the devices [5]. As technology decreases, the leakage power consumption dominates the total power consumption [6]. Scaling of technology also scales the threshold voltage. Sub-threshold leakage current will get increased with the decrease in threshold voltage. Stability of the SRAM memory cell is of utmost care in deep submicron technologies as it becomes difficult to maintain stability with scaling down of technology. This paper presents the methods of controlling the leakage currents in SRAM by implementing low power technique for SRAM cell i.e. power gating along with the aim of maintaining the SRAM stability. Header switch implementation (type 1) and Footer Switch implementation (type 2) are the two variations of the power gating technique which are also implemented in this paper. The stability is stated as the minimum amount of voltage that flips the information stored in the cell [7]. SNM calculates the stability of the SRAM. There are several methods for calculating SNM for the SRAM cell. One that is used in this paper is the butterfly curve method. The butterfly curve is plotted by combining the VI characteristic and the inverted VI characteristic of the SRAM SNM is observed by measuring one side of the maximum possible square inside the lobe of the butterfly curve [8] [9]. Stability i.e. SNM is calculated for different modes of operation of SRAM memory cell i.e. hold, read and write mode. The CMOS technology node used is 16nm and schematic is implemented using the low- power Predictive Technology Models (PTM). PTMs are used by the designers and researchers for creating future technologies for both transistors and interconnect [10] [11]. The objective of the power gating technique is to switch off the SRAM cell during standby mode and hence leakage current can be minimized. During read/write mode, the sleep transistors are activated whereas during the standby mode the sleep transistors are deactivated [12], [16]-[19].

The paper has been arranged as follows. Section 2 explains the setup of the conventional SRAM. The power gating technique for SRAM cell and the variations of power gating technique i.e. header switch implementation of the SRAM cell (type 1) and footer switch implementation of SRAM cell (type 2) are also outlined in this section. Section 3 discusses the design metrics and simulation results. Section 4 concludes the paper.

2. POWER GATED SRAM CELL

The circuit setup of the conventional SRAM cell is displayed in Fig.1.

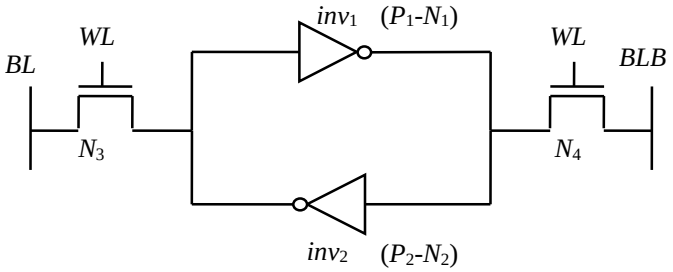

Fig.1. Circuit Setup of the SRAM cell

The inv_1 (P_1-N_1) and inv_2 (P_2-N_2) are the two cross-coupled inverters, which store information in the SRAM cell [13]. The word line (*WL*) is used for activating and deactivating the access transistors N_3 and N_4 [14]. The bit line *BL* and bit bar line *BLB* are used as input and output during the write operation and read operation respectively. With the scaling of the CMOS technology nodes, the static power dissipation of the SRAM cell increases. The static power dissipation constitutes of the sub-threshold leakage current, gate leakage current, and junction leakage current. The Fig.2 shows the leakage paths of the conventional 6T SRAM cell.

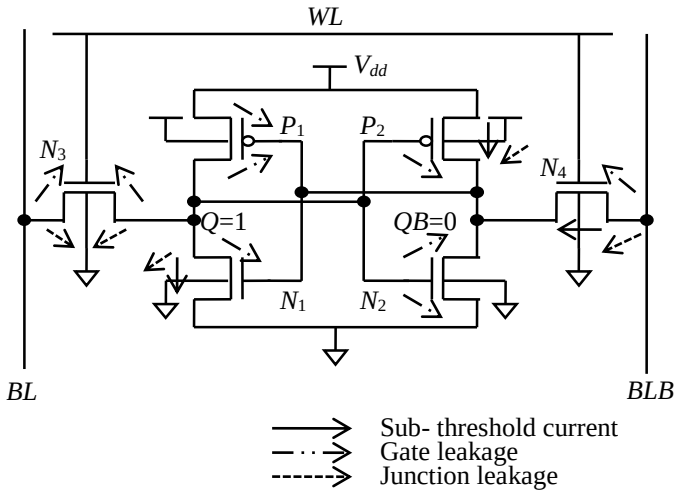

Fig.2. Leakage path of the Conventional 6T SRAM memory Cell

The low power technique employed in this paper is Power Gating. The architecture of the power gating circuit for the SRAM cell is shown in Fig.3. Power gating technique reduces the leakage power consumption of the SRAM memory cell during standby mode by shutting the power supply. Power and delay are optimized with the help of power gating (sleep transistors) [2] [5]. This technique makes use of high-V_t PMOS and NMOS. The leakage power dissipation of high-V_t transistors is low, however, the switching speed is slow. Header high-V_t PMOS sleep transistor creates a virtual power rail and it is placed between the physical power supply and virtual power rail. While Footer high-V_t NMOS sleep transistor creates a virtual ground. It is placed between the virtual ground and physical ground.

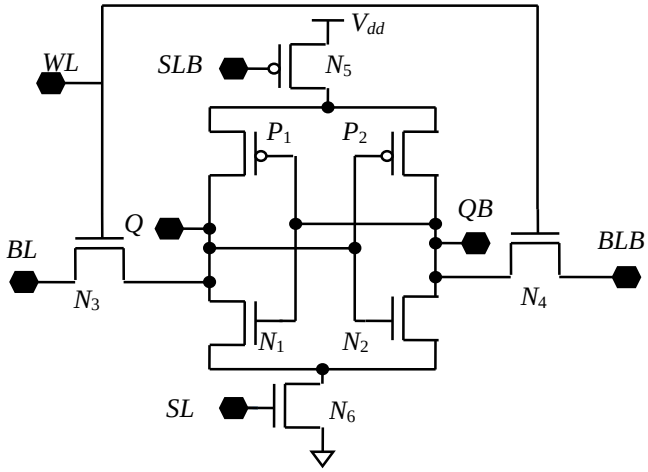

Fig.3. Schematic of the Power Gated SRAM memory cell

The schematic of the Header Switch implementation of SRAM cell is displayed in Fig.4. In this architecture high-V_t PMOS transistor is embedded between the physical power supply and virtual power rail. The leakage power consumption of the PMOS is less than the NMOS. Hence the static power dissipation of the header switch implementation is less than footer switch implementation. However, the switching speed of the PMOS is less than the NMOS, which makes the header switch implementation slower than the footer switch implementation.

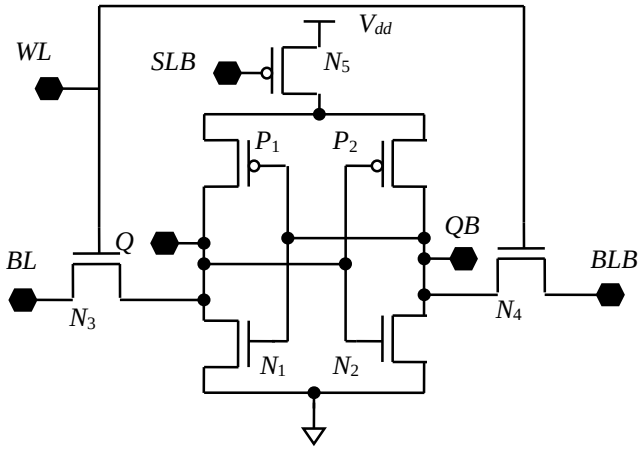

Fig.4. Schematic of the SRAM cell with Header Switch (Type-1)

The schematic of the Footer Switch implementation of SRAM memory cell is displayed in Fig.5. The architecture of footer switch implementation consists of high-V_t NMOS footer switch which is situated between the physical ground and virtual ground. The performance of the footer switch implementation is better than the header switch implementation as the switching speed of the footer switch is faster than the header switch. However, the NMOS footer switch is leakier than the PMOS header switch. Thus in footer switch implantation, the static power dissipation is more in comparison to the header switch implantation.

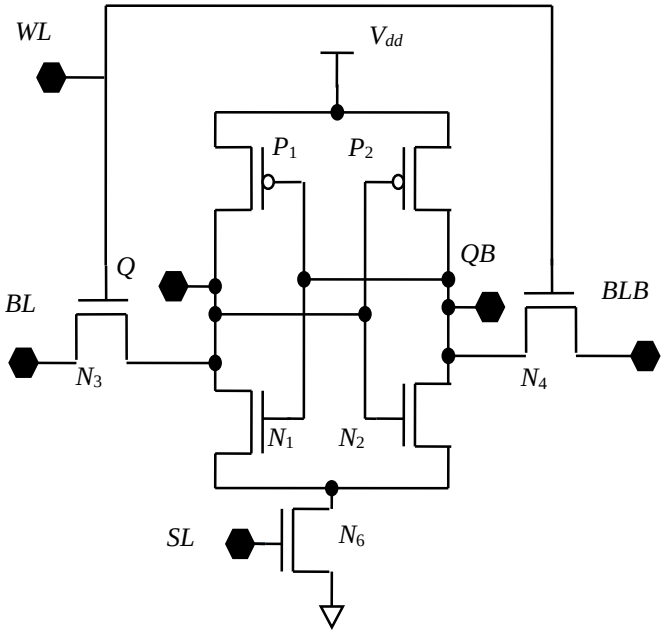

Fig.5. Schematic of the SRAM cell with Footer Switch (Type-2)

3. SIMULATION RESULTS

The results of the power gated memory cell, SRAM cell with header switch implementation and SRAM memory cell with footer switch implementation are discussed in this section. The simulation was done using low-power PTM model. The results are obtained by keeping the length and width of the PMOS and NMOS equal to the CMOS technology. The average power dissipation, delay, Power Delay Product (PDP) are evaluated for different SRAM cells i.e. conventional 6T SRAM memory cell,

power gated SRAM memory cell, header switch SRAM, and footer switch implementation. Schematics of the circuits are designed and simulated on 16nm technology node with 1V power supply using Cadence Virtuoso tool. The average power is computed for the write operation. The Fig.6 shows the transient analysis of the Power Gated SRAM cell.

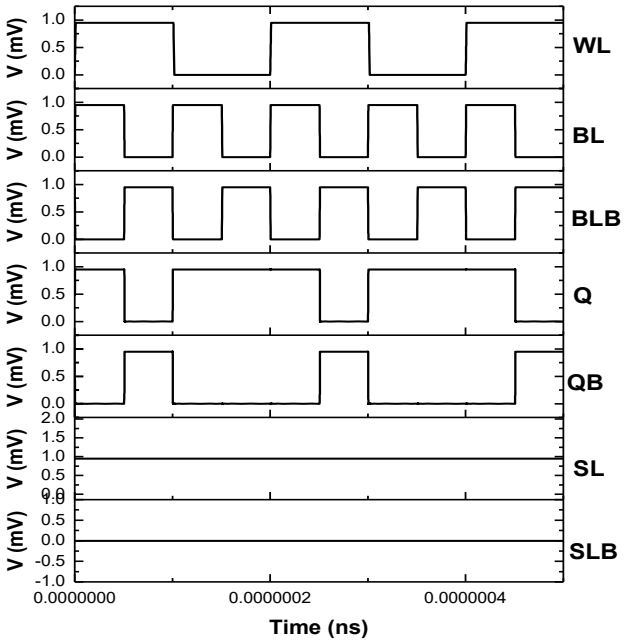

Fig.6. Transient Analysis of Power Gated SRAM cell

The Table.1 shows the comparative analysis of Conventional SRAM and low power SRAM cells on 16nm technology node. The observation made from Table.1 suggests that the power gating technique of leakage power reduction is the most efficient among type 1 and type 2. The power consumed by the power gating technique for SRAM cell is 18.07% less than type 1 and 15.54% less than type 2. Moreover, type 2 uses 3% less power than type 1.The speed of any design is predicted from its delay. The delay is the difference in time at which input is given and time at which output is obtained. The delay at the rising and falling edge is least in case of power gated SRAM memory cell.

The performance of the SRAM memory cell is predicted by calculating PDP. Less the value of PDP greater is the performance. The results illustrate that the performance of the power gated is greater than type 1 and type 2. The performance of type 2 is better than type 1.Fig.7 to Fig.11 shows the graphical representation of average power consumption, delay, PDP, WSNM, and RSNM respectively of the different SRAM cells.

Table.1. Comparative analysis of Conventional SRAM and Low-Power SRAM cells on 16nm technology node

Performance Parameters	MOS 6T SRAM	Power Gating Technique	Header Switch (Type 1)	Footer Switch (Type 2)
Power Consumption (W)	728.9p	521.9p	637p	617.9p
Delay1 (ps)	226.6p	100.1n	221.6p	226.8p
Delay0 (ps)	105.3p	96.86p	100.1p	100.9p
PDP1 (Ws)	165.1z	52.24a	141.1z	140.1z
PDP 0 (Ws)	76.73z	50.55z	63.79z	62.32z
WSNM (mV)	373	396	382	373
RSNM (mV)	97	67	99	69
HSNM (mV)	337	334	337	334

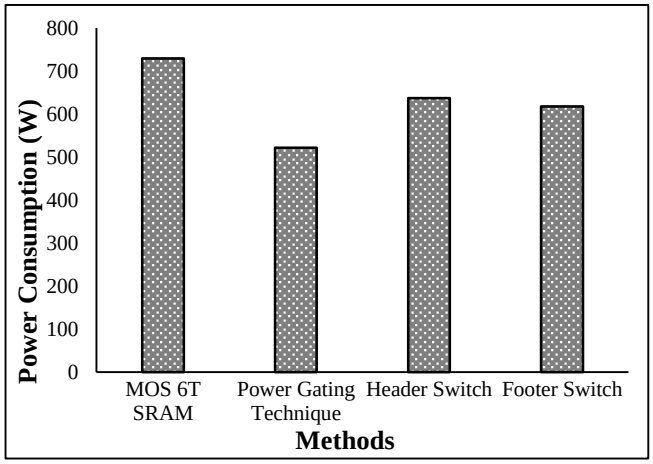

Fig.7. Power Consumption of different SRAM memory cells

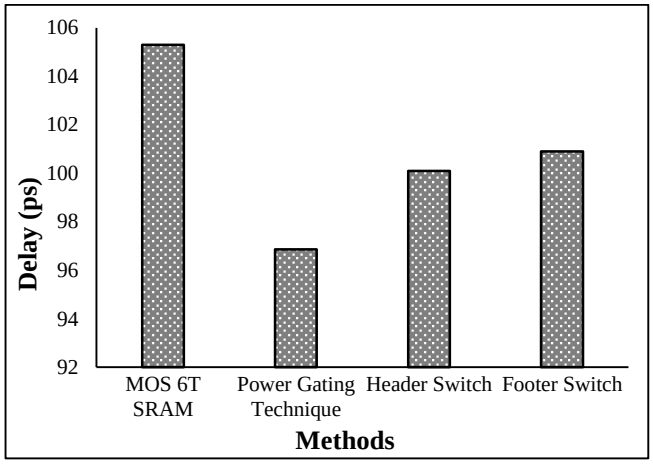

Fig.8. Delay of different SRAM memory cells

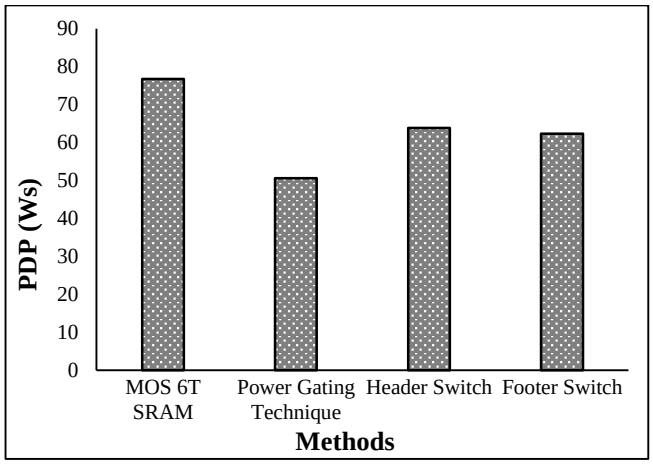

Fig.9. PDP of different SRAM memory cells

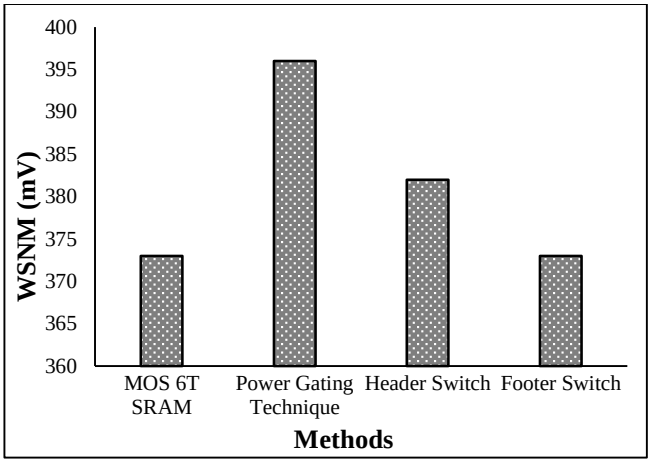

Fig.10. WSNM of different SRAM memory cells

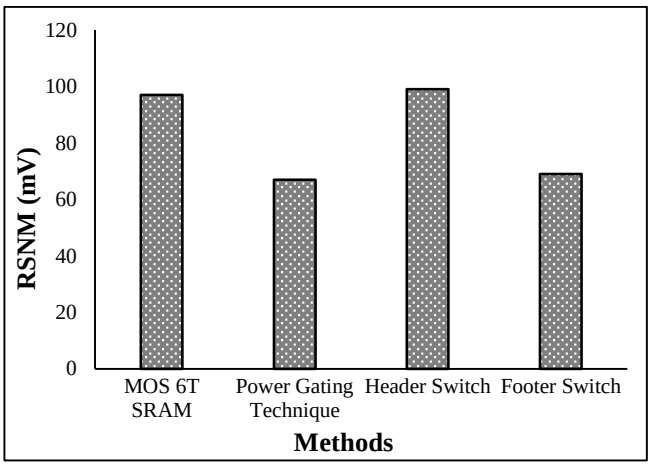

Fig.11. RSNM of different SRAM memory cells

SRAM stability is a crucial parameter [15]. SRAM cell's stability tends to decrease on decreasing the CMOS technology node. With the aim of decreasing power dissipation, the designer also focuses on maintaining the stability of the SRAM memory cell. The stability is calculated using the Static Noise Margin (SNM). More the SNM more is the stability. The stability of type 1 is increasing for all three modes of operations. On comparison with type 1 the WSNM of the power gated SRAM increases by 3.66% whereas it increases by 6.17% in case of type 2.

4. CONCLUSIONS

The performance parameters and stability analysis of power gated SRAM cell, type 1, and type 2 were comparatively analyzed on 16nm technology node. The analyses of the low power SRAM cells were done using low-power PTM models in Cadence Virtuoso software. It was noticed that the average power dissipation of the power gated SRAM memory cell is least among type 1 and type 2. The power consumption decreases by 18.07% and 15.54% in power gated SRAM cell compared to type 1 and type 2 respectively. The delay as well as the Power Delay Product is decreasing for power gated SRAM cell, which signifies the speed and performance of the power gated SRAM memory cell are high. The WSNM for the power gated SRAM memory cell increases by 3.66% in comparison to type 1 and 6.17% in comparison to type 2.

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