

SINUSOIDAL POWER CLOCK BASED PFAL

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Abstract

The following manuscript proposes a modification to the existing PFAL based adiabatic structure called 2Phase PFAL for its operation on two phase sinusoidal power clocks and lower power dissipation. Sinusoidal shaped power clocks are easier to design and can be used to operate the adiabatic circuit in two phases. This proves to be advantageous as it reduces the on-chip routing complexity and density of the power-clock logic. Moreover usage of a two phase structure over a four phase structure for adiabatic operation reduces the phase consistency relationship requirement among the power clocks to realize the potential adiabatic gains. Conventional PFAL based approach requires the usage of buffers both at the input and output stages, increasing the buffer requirement. The proposed circuit is advantageous as it operates on two phases, reducing the buffer requirement leading to savings in area and power. Simulations using a standardized test bench have been performed for CMOS, PFAL and Proposed Logic based Inverter, Inverter Chain, NAND, NOR, XOR and XNOR structures. The results show that the proposed structure require less power as compared to its nearest competitors. Lower power dissipation with phase reduction, ease of power clock generation, reduced routing complexity and phase consistency relations among the power clocks make the proposed logic an suitable candidate for use in low power digital devices operating at low frequencies such as radio-frequency identifications (RFID's), smart cards, and sensors.

Keywords:

PFAL, 2Phase PFAL, CMOS, Sinusoidal

1. INTRODUCTION

Evolution and demand of portable devices has led to the development of better display technologies and batteries with high energy storage densities [1]. Also, significant research efforts are made towards reducing power consumption of electronic circuits. The CMOS based circuit design has been used extensively in designing the digital circuits because of design ease and availability of extensive electronic design automation tools. However, the energy dissipated in these circuits is proportional to capacitive load and square of supply voltage. The charge flow occurs during charging when the load capacitance is charged to VDD via the pull-up network whereas this charge is discharged to the ground during the discharging event via the pull-down network [2]. In recent past, adiabatic logic style, which is based on adiabatic process of thermodynamics and characterized by no gain or loss of energy, has gained popularity [3]. The adiabatic logic finds its emergence and proliferation in Smart Cards and other security-centric technologies [4]. The supply voltage in adiabatic circuits is time varying clocks (sinusoidal, trapezoidal or triangular). In adiabatic logic charge recovery (i.e. energy supplied during charging is fed back to the source) while discharging takes place [5]. The guidelines for adiabatic circuit operation [6, 7] are; never switch transistor ON while a potential

difference exists between the drain and source terminals; never turn transistor OFF when there is current flow through the circuit.

Positive Feedback Adiabatic Logic (PFAL), Efficient Charge Recovery Logic (ECRL) and Two NMOS-two PMOS- two PMOS (2N2N2P) are some of the most profound adiabatic families which have thoroughly been investigated by the researchers in adiabatic literature [8]-[10]. The PFAL logic outperforms these families in terms of power and hence it has been used for further exploration in this paper. The PFAL requires four phase trapezoidal shaped power clocks for its proper operation. Power clocks play the dual role of enforcing correct logic as well as charge recovery from the output node. The generation of trapezoidal clocks is more complex and would require much more area and power overhead than sinusoidal clocks [8]. Usage of such clocks (trapezoidal, sinusoidal) in adiabatic families calls for proper phase alignment between the clocks and inputs. Such requirement is important both for correct logic as well as to realize the theoretical adiabatic gains. When implemented on a chip alongside other components, the path parasitic will delay these clocks with varying degree leading to reduced power efficiency. PFAL uses buffers to ensure phase alignment among the inputs and clocks, but introduction of such buffers increases the area and power overhead. In particular for an n-bit RCA, the buffer size grows with the order of n^2 and for higher values of n the buffer number dominates the overall area and power of the structure reducing the theoretical power efficiency. For other cascaded designs, depending upon the circuit topology the buffer size grows.

Hence to overcome shortcomings of the trapezoidal clocks, sinusoidal clocks are employed for the operation, which are easier to produce vis-à-vis trapezoidal shaped counterpart. The sinusoidal power clocks are applied to PFAL structure as it presents most power saving and is energy efficient. The modification is named as 2PHASE-PFAL where the word 2PHASE indicates two phase operation. The proposed structure is differential in operation, similar to PFAL and uses full swing sinusoidal clocks VCLK and VCLKBAR for its operation.

The paper is divided into 5 sections. The rest of the paper is divided as follows Section 2 deals with Differential Adiabatic Logic Circuits [14-18], such as PFAL. Section 3 deals with our proposed circuit 2 Phase PFAL on similar lines. Results and Simulations are presented in Section 4 while further discussion and conclusion in Section 5.

2. BACKGROUND AND RELATED WORK

2.1 ADIABATIC LOGIC

Adiabatic logic represents a class of logic circuits that reduces the energy dissipation during the switching events, and improves the possibility of recycling, or reusing the energy drawn from the

power supply. Koller and Athas [1] introduced an adiabatic latch circuit that stores the information which node was charged. Without the need to keep and restore the input signals, the energy can be recovered from the output nodes through the use of powered/clocked/pulsed power supplies. To understand the adiabatic switching, a simple RC circuit with capacitor being charged by a voltage ramp is shown in Fig.1. Since a whole cycle consists of charging and recovery event, the overall dissipation in adiabatic logic is given as:

$$E_{Dissipation} = E_{Charging} + E_{Discharging} \quad (1)$$

$$E_{Dissipation} = I^2 R_{Charging} T + I^2 R_{Discharging} T \quad (2)$$

$$E_{Dissipation} = (R_{Charging} C_L + R_{Discharging} C_L) C_L V_{DD}^2 / T \quad (3)$$

where, time period of the supply is given by T , charging /discharging path resistances are $R_{Charging}/R_{Discharging}$ respectively, load capacitance is given C_L and Supply Voltage by V_{DD} . Using Eq.(3), $E_{Dissipation}$ tends to zero when $T \gg (R_{Charging} + R_{Discharging})C_L$. This is referred to as adiabatic loss in the literature. The dissipated energy is smaller than the CMOS [1] if the charging time is larger than $2RC$. The energy dissipation can be made arbitrarily small by increasing the charging time. Reducing the resistance of the circuit will reduce the energy.

2.2 POSITIVE FEEDBACK ADIABATIC LOGIC

The PFAL (Positive Feedback Adiabatic Logic) family has been prevalent in the literature since two decades. The structure is a latch element formed by two cross-coupled inverters with the functionality implemented with an NMOS transistors connected in parallel to PMOS in latch structures. PFAL gates exhibit high immunity and lowest power consumption. However, the output node is kept floating when the magnitude of the power clock is less than the threshold voltage, leading to partial energy-recovery logic. Previously discussed logic families require multiphase trapezoidal clock which are difficult to generate. In contrast, sinusoidal waveform generators are simple and are efficient than the trapezoidal waveforms. In addition, the longer rise and fall time of sinusoidal power clock over trapezoidal power clock at the same frequency makes them more suited to the basic aim of low power adiabatic circuit design. The Fig.1 shows the design of PFAL inverter/buffer operating with four phase trapezoidal clock VCLK. The Fig.2 shows the waveform of PFAL based inverter/buffer.

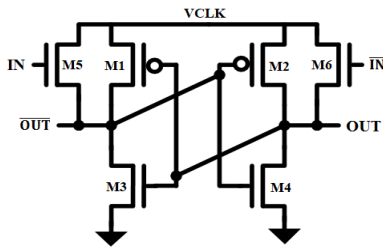


Fig.1. PFAL Inverter/Buffer

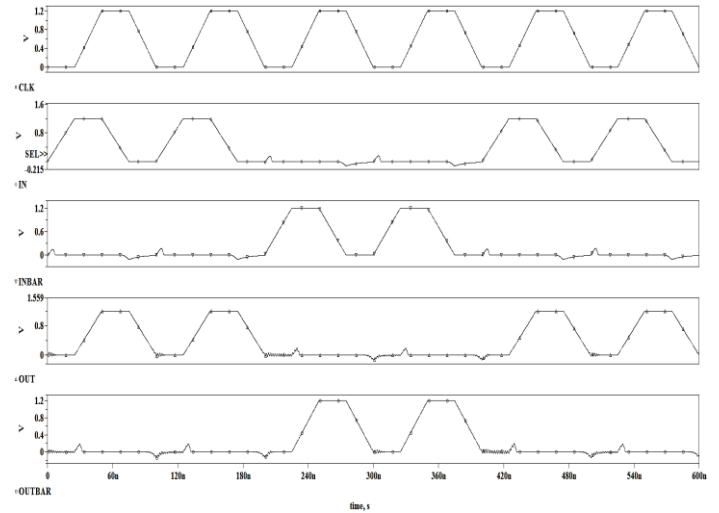


Fig.2. PFAL Inverter Waveform

2.3 SINUSOIDAL OPERATION ON POSITIVE FEEDBACK ADIABATIC LOGIC

The advantages of sinusoidal clocks both in terms of generation and phase of operation, make them a viable alternative to the existing four phase trapezoidal families in differential adiabatic logic families. Hence, we first aim to operate the conventional PFAL structure with sinusoidal clocks to study and understand the operation.

For the operation we use the conventional PFAL Inverter Structure operating with the following power clock:

$$V_{CLK} = \frac{V_{DD}}{2} + \frac{V_{DD}}{2} \sin(\omega t) \quad (4)$$

Subsequent stages of the pipeline are fed with complementary clocks for proper operation. The complete circuit was operated on two phase which are as follows:

2.3.1 Evaluate Phase:

When the VCLK goes from 0 to V_{DD} it is referred to as evaluate phase. Inputs are evaluated in this phase to decide the respective outputs.

2.3.2 Hold Phase:

When the V_{CLK} ramps down from V_{DD} to ground it is referred to as the hold phase. During this phase the output logic is kept constant and the output is used by subsequent stages for their evaluation.

Sinusoidal shaped power clocks are fed to the PFAL Inverter and the results are compared with those of conventional PFAL structure. The results of the comparison were far from being acceptable. The power dissipation in the new circuit increased manifolds from the conventional PFAL structure. Careful analysis of the circuit revealed that such losses were observed mainly due to inability of the circuit to provide complete isolation of the power clock and ground during its operation. This non-isolation leads to a short circuit between the power clock and ground leading to high power losses. When PFAL is operated on two phase clocks, the evaluation phase of one stage overlaps with the hold phase of the subsequent stage. For instance, assume that a two stage PFAL Inverter is available with IN , IN_{BAR} as the input

to the first stage, OUT_1 , OUT_{BAR1} as the outputs of first stage and OUT_2 , OUT_{BAR2} as the output of the second stage respectively. During the evaluation phase of second stage (i.e. when CLK_2 ramps towards V_{DD}), its complementary inputs (OUT_1 and OUT_{BAR1}) are HIGH (V_{DD}) and LOW (0V) respectively as shown in Fig.3. The second stage depending upon the input, evaluates the logic and the required output OUT_{BAR2} (for the above case) follows the clock. When the second stage enters the hold phase, the inputs from previous stage are no longer required for operation as the power clock is connected to the output node through one of the cross-coupled PMOS. During this time the first stage has entered into evaluate phase and its output logic can change depending upon the inputs applied. Towards the end of the hold phase, before the PMOS turns OFF, the output OUT_{BAR1} from first stage turns ON the complementary logic NMOS transistor of the second stage making a direct path between OUT_2 and the its power clock, which also turns ON the NMOS connected between ground and OUT_{BAR2} . This process occurs before the PMOS connected to OUT_{BAR2} , turns OFF. Due to this a direct path is formed between power clock and the ground, leading to short-circuit power losses. The Fig.6 also shows the current flow through the clock CLK_2 during various transitions. It shows that whenever the logic from first stage changes and towards the end of hold phase of second stage, a high amount of current flows from the power clock, indicating a short circuit.

3. PROPOSED - 2PHASE PFAL

3.1 OPERATION

To overcome the problem enshrined above and to take on the advantage of two phase sinusoidal clock operation, we propose a modification to the conventional PFAL structure. The structure is similar to basic PFAL with an addition of MT transistor as presented in Fig.4. The transistor is driven by true clock (V_{CLK}) while its source is connected to complementary clock (V_{CLKBAR}). So transistor MT turns OFF for V_{CLK} , V_{CLKBAR} and eliminates the direct path formation between power clock and ground.

The proposed logic shown in Fig.4 operates on full swing sinusoidal clocks, true V_{CLK} and complementary V_{CLKBAR} . The proposed logic operates on two phase evaluate and hold phase. During the evaluate phase V_{CLK} ramps up from 0 to V_{DD} whereas V_{CLKBAR} ramps down. During the hold phase, V_{CLK} ramps down from V_{DD} to ground and V_{CLKBAR} ramps up to V_{DD} from ground. V_{CLK} rises in the evaluate phase and supplies energy to the circuit, then during its fall, the energy flow back from the load capacitance to the power clock. For instance it is assumed that the input IN is in logic HIGH and the dual input IN_{BAR} is at logic LOW during the evaluation phase. Consequently, M5 is conducting and the output node OUT_{BAR} follows the power clock V_{CLK} . The hold phase starts with the enabling of latch when V_{CLK} reaches $V_{DD}-V_{TN}$ and V_{CLKBAR} decays to V_{TN} , node OUT follows the V_{CLKBAR} . The input IN can ramp down since the latch is ON. In the hold phase since OUT and OUT_{BAR} hold valid logic levels which they can be used as input to the other cascaded stages. The recovery phase starts when the V_{CLK} ramps down to $V_{DD}-V_{TN}$ and extends till it reaches V_{TP} . As the V_{CLK} falls, the resistance of M_1 increases until M_1 turns OFF and recovery stops. The charges are supplied back to the power clock V_{CLK} during this phase.

The Fig.5 shows simulation waveform for a two stage proposed inverter with IN , IN_{BAR} as the inputs of first stage, OUT and OUT_{BAR} first stage outputs and OUT_1 and OUT_{BAR1} the outputs of second stage. It also shows the Evaluate and Hold phases for the first power clock. The simulation waveforms show that whatever be the input (ideal or actual) the output remains same. In cascaded designs, the inputs and outputs are out of phase by 180, due to which we observe a delay of 0.5 clock cycle.

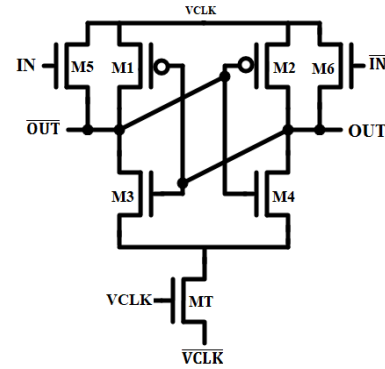


Fig.4. 2Phase-PFAL Inverter/Buffer

Table.1. Simulation Setup

Parameter	Value
Process/MOS Model	90nm PTM
Simulator	SYMICA Design Environment
MOS dimensions	135/90 for NMOS 600/90 for PMOS
Supply Voltage	1.2V
Clock Rate (F_{CLK})	Twice the Data Rate (F_{IN})
Simulation Time	10 cycles of Charging and Discharging
Threshold Voltages	PMOS = 0.243V, NMOS = 0.393V

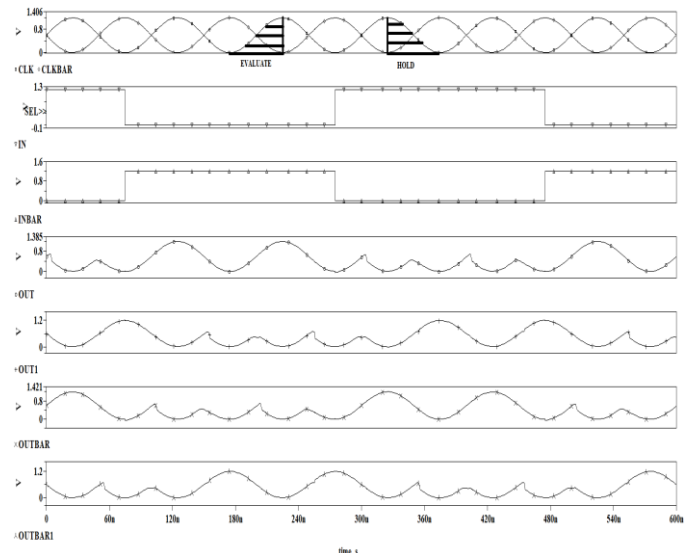


Fig.5. 2Phase-PFAL Inverter Waveform

4. SIMULATIVE INVESTIGATION

4.1 SIMULATION ENVIRONMENT

The Adiabatic Logic Circuits use time varying supplies called power clocks - trapezoidal or sinusoidal and inputs. Hence it becomes essential that that realistic supplies and inputs be used for simulating the Design Under Test (DUT) in order correctly observe circuit's behavior and the power estimate from the simulation tool be as much close to real scenario as possible. But developing these realistic inputs simulation tools is very difficult and not an effective solution. To solve this problem with view in mind for realistic analysis a standardized simulation setup [15] has been established as shown in Fig.11 wherein instead of using realistic load we have used capacitive load for simulations. It shows that the power measurements for any N input, M -output adiabatic circuit requires that any ideal signals be applied to the first stage, whereas the DUT is fed by outputs from the second stage. The Fig.11 shows the simulation setup for more accurate and realistic simulations.

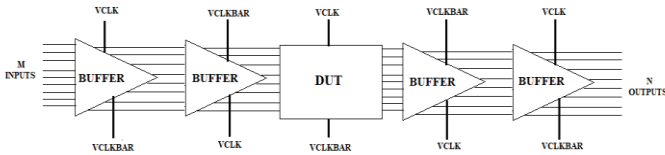


Fig.6. Standardized Simulation Setup

4.2 SINGLE STAGE CIRCUIT DESIGN USING PROPOSED LOGIC

4.2.1 Inverter - Power Dissipation with Frequency:

The Fig.7 shows the variation of Power Dissipation with Frequency for an Inverter circuit. The graph shows that proposed logic dissipate the least power among PFAL and CMOS from 10 MHz – 200 MHz. The graph shown below completely justifies our claim that the proposed logic saves on the non-adiabatic losses. Non-adiabatic losses are dominant losses for lower values of frequencies, hence our proposed logic which saves on non-adiabatic losses, shows higher savings at lower frequencies.

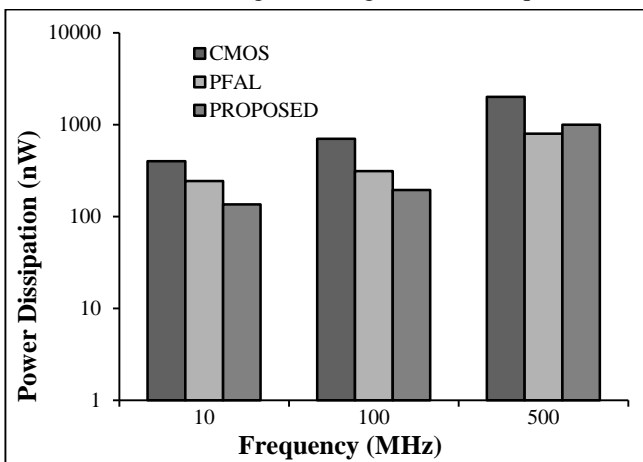


Fig.7. Power Dissipation vs. Frequency for an Inverter

The Fig.8 shows the variation of power dissipation with capacitance for an inverter circuit. The graph shows that proposed logic dissipate the least power among PFAL and CMOS from 1fF to 100fF. The graph shows that the proposed logic can work with load capacitances up to 100fF for lower power operation.

4.2.2 Power Dissipation with Capacitance:

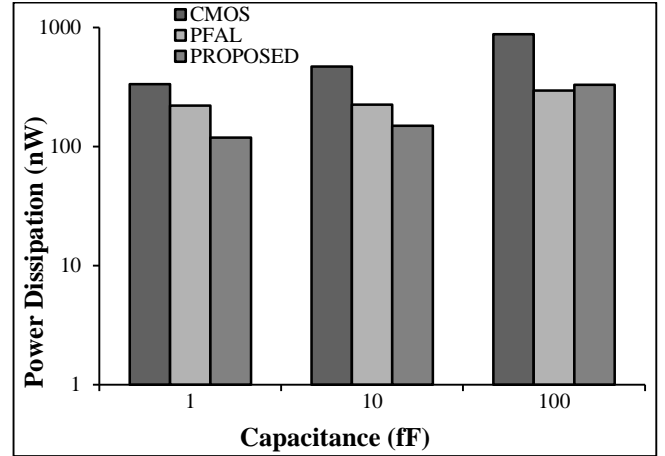


Fig.8. Power Dissipation vs. Capacitance for an Inverter

4.2.3 NAND/NOR Gate Topology:

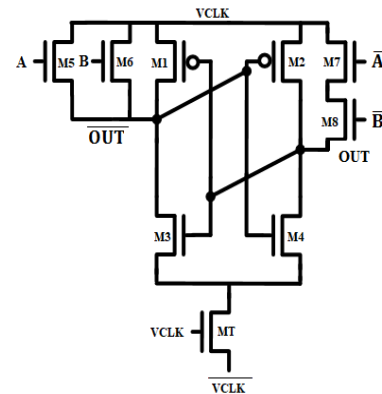


Fig.9. NOR/OR Gate

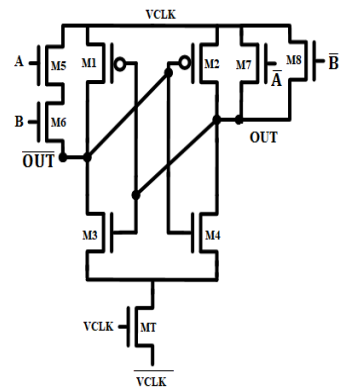


Fig.10. NAND/AND Gate

The Fig.11 shows the variation of Power Dissipation with Frequency for NAND/NOR gate topology. The graph shows that

the proposed logic dissipates low power for frequencies till 200MHz, due to complete charge recovery for reducing the non-adiabatic losses.

4.3 MULTI STAGE CIRCUIT DESIGN USING PROPOSED LOGIC - STAGE NAND OPERATIONS

The Table.2 shows Power-Transistor Product (i.e. Product of Power Dissipated and number of transistor) of a 4 Input NAND Operation, it shows that for a Multi Stage Circuit Design, the proposed logic saves both on Power and Area. The Fig.14 shows the gate level design for a 3 Stage NAND Operation

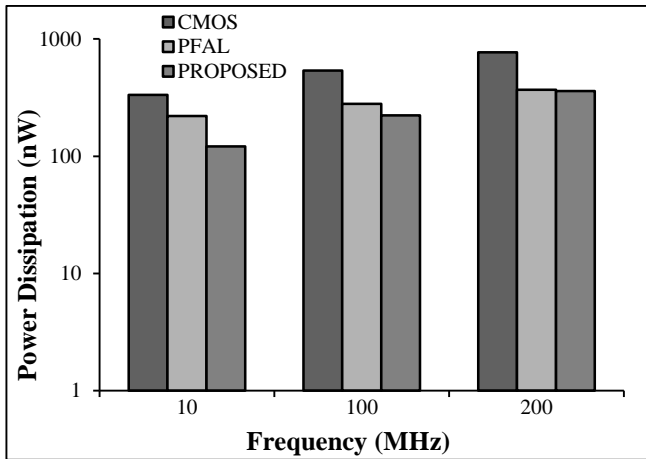


Fig.11. Power Dissipation vs. Frequency for NAND/NOR Topology

4.2.4 XOR-XNOR Gate Topology:

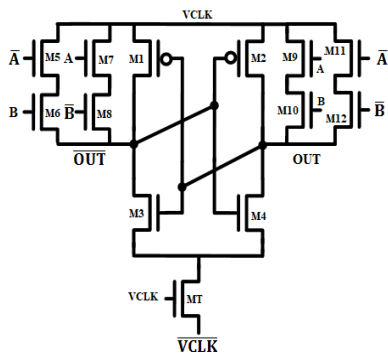


Fig.12. XOR /XNOR Gate

The Fig.13 shows the variation of Power Dissipation with Frequency for an XOR-XNOR gate topology. The graph shows that the proposed logic dissipates low power for frequencies till 200MHz, due to complete charge recovery for reducing the non-adiabatic losses.

Table.2. Power-Transistor Product for a 3 Stage NAND Operation

Frequency	10	100	200
PFAL	99000	164400	300000
Proposed	21976	44690	108240
NT(PFAL) = 60	NT (Proposed) = 41		

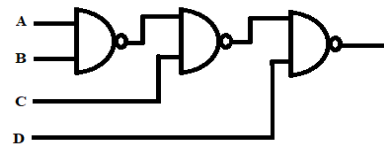


Fig. 14. Gate level Design for a 3 Stage NAND Operation

The Table.3 shows Power-Transistor Product (i.e. product of power dissipated and number of transistor) for the Maximum Length of Buffer with dissimilar phases. It shows that for a Multi Stage Circuit Design, the proposed logic saves both on Power and Area.

Table.3. Power-Transistor Product for Maximum Length of Buffer with dissimilar phases

Frequency	10	100	500
PFAL	12060	16200	37080
Proposed	952	1365	6965
NT(PFAL) = 18 (3 Buffers)	NT (Proposed) = 7 (1 Buffer)		

5. CONCLUSIONS

The Simulative Investigation shows that the proposed logic can efficiently replace PFAL based structures for lower power dissipation at low to medium frequencies. For higher frequencies, it indirectly saves power and area because of the reduced buffer requirement. In adiabatic logic circuits, to realize the theoretical gains, it is important that the power clocks, maintain their phase consistency relation throughout the operation, any deviation from these might lead to potentially higher power losses. For four phase logic circuits, this phase consistency requirement among the power clocks is manifested in form of delay of $T/4$ in each of the four consecutive power clocks. For two phase logic, this phase consistency requirement is somewhat relaxed to only two (rather than four) consecutive power clocks, separated by $T/2$ delay. Moreover, generating a sinusoidal shaped clock is much simpler and easier than generating a trapezoidal shaped clock. On-chip implementation of the four phase clock logic will require more area and increase its routing complexity and density as compared

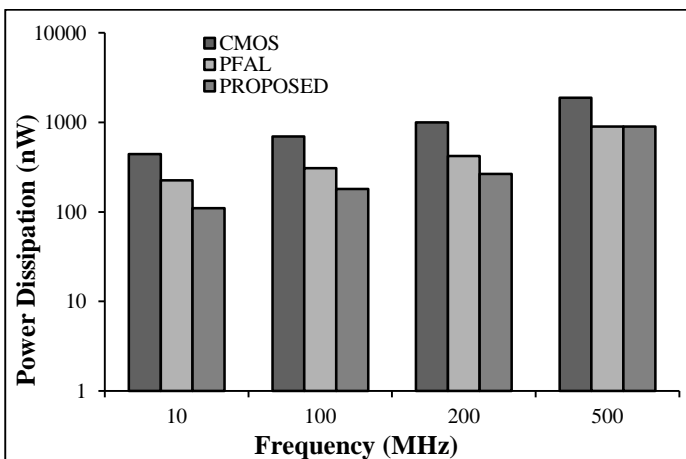


Fig.13. Power Dissipation vs. Frequency for an XOR-XNOR Gate

to two phase logic clock logic. Moreover, in adiabatic logic, the external circuitry responsible for generating the power clock must be able to recover the charge through the output node during recovery phase to realize the adiabatic gains. Practically generated sinusoidal shaped clocks are similar to the sinusoidal clocks used for theoretical calculations, but the same is not true with trapezoidal shaped clocks [1]. Hence, usage of sinusoidal clocks provides us with more reliable and practically realizable gains. Hence, we can conclude that proposed logic can be used for adiabatic logic circuit designs for higher power and area savings which are realizable both theoretically and practically.

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