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PROCESS AND MODELLING ASPECTS OF POLYIMIDE OVER SILICON FOR RF CIRCUITS REALIZATION AND ITS IMPLEMENTATION

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Abstract

The integration of RF circuits with CMOS on the same substrate is challenging and imposes lot of constraint in practical realization due to inherent losses associated with silicon Si substrate. Various mitigation techniques are proposed to overcome the same which are either process intensive or introduces multiple deleterious effects at RF frequencies. Polyimide is used both in microelectronics and MEMS industry as it can act both as a photo-resist and also having key dielectric properties. The processes presented with polyimide are standard and can be easily integratable with the existing CMOS processes. Fabrication steps and simulation study of the band pass filter topologies over polyimide are presented and the same are fabricated with the proposed process steps. Further this article details the modelling, theoretical aspects, various process steps and actual implementation with the realization of the band pass filter topology using the proposed methodology.

Keywords:

Polyimide, Silicon, Radio Frequency, Modelling

1. INTRODUCTION

CMOS circuits are fabricated on low resistivity silicon which is lossy at RF frequencies resulting in poor performance [1]. Standard silicon substrate is having low resistivity (ρ ~10-20, Ω-cm) and realized using C-Z process [2] [3]. Traditionally microwave circuits realized on the low resistivity silicon (LRS) substrates i.e. CMOS grade Si wafers, exhibits higher losses due to higher loss tangent associated with basic silicon structure [2]. One of the most common solutions is to utilize VLSI backend dielectric layers on top of Si substrate to reduce the lossy effect. The co-existence of RF circuits with CMOS [4] in this scenario is difficult unless specific process steps such as high energy implantation are introduced which causes certain defects in the wafer. Considerable research is carried out and various methodologies are introduced such as thick nitride or oxide layer over silicon employing standard silicon substrate, trench opening and filling the same but all these steps create undue stress to the wafer besides compromising the film stochimetricity due to higher film thickness. However, large loss from Si substrate is still unavoidable because of the limited thickness provided by current VLSI technology.

High resistivity wafer (ρ > 2k, Ω-cm) realized using float zone (F-Z) process can mitigate the undesirable effects [5]-[6] but high resistivity silicon (HRS) not only is costlier but exhibits higher dielectric loss [7]-[8]. Due to high frequency of operation, the dielectric behaviour of the silicon substrate, assuming to be resistive, is no longer valid below the dielectric relaxation frequency defined by

$$f_c = \frac{1}{2\pi\rho\varepsilon'} \tag{1}$$

where ρ and ε' are the resistivity of the substrate and permittivity of silicon [9]. This relation also shows strong dependency of the doping on the cut off frequency. Alternately, dielectric layer such as polyimide can be used on top of the CMOS grade substrate for the realization of the low loss microwave components. Both microstrip and coplanar waveguide transmission lines exhibit low attenuation in such circuits [10]. The reported structures either lack process information or not having mathematical modelling of the same [11]-[12]. The article encompasses both the aspects and dealt with its practical realization.

The thickness of polyimide can be easily controlled by varying spinning speed and time. Also ease of process integration and complete removal using ashing are the other aspects associated with the polyimide process which is generally employed in the realization of the capacitive sensor in MEMS [13]. The article briefs the modelling aspect of the transmission line on the substrate followed by the process steps. Further filter realization employing the above process is carried out to validate the adopted approach.

2. MODELLING ASPECTS

The demarcation line between the conductor and dielectric is the (a) substrate permittivity which relate the storage of charge associated with the dielectric and (b) dielectric relaxation frequency 'τ' which is defined as the time required for the charge density to decay to 1/*e* times its initial value. The mathematical expression of the same using constituent relationship and employing Maxwell's equation can be written as:

$$J = \sigma \cdot E \tag{2}$$

$$\nabla \cdot J = \frac{\sigma}{\varepsilon}\left(\nabla \cdot D\right) \tag{3}$$

$$\nabla \cdot J + \frac{\partial \rho}{\partial t} = 0$$

$$-\frac{\partial \rho}{\partial t} = \left(\frac{\sigma}{\varepsilon}\right)\rho \tag{4}$$

where,

$$\rho = \rho_0 e^{-(\sigma/\varepsilon)t}$$

$$\rho = \rho_0 e^{-\tau . t}$$

$$\tau = \varepsilon / \sigma \tag{5}$$

The Table.1 shows comparative analyse of the dielectric relaxation frequency using the Eq.(5).

Table.1. Relaxation time of various materials

Material	Relaxation time (τ)
Silver	1.4×10^{-19} sec
Copper	1.5×10^{-19} sec
Gold	2.0×10^{-19} sec
Si (low resistivity)	2.6×10^{-7}sec
Si (high resistivity)	15.7 min
Alumina	>100 days

As shown in Table.1, effective charge decay in the case of dielectric is much higher than the conductors. The equivalent circuit of the transmission line over silicon can be represented in Fig.1.

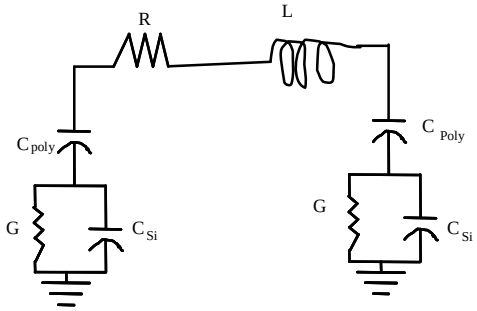

Fig.1. Transmission line equivalence

The shunt conductance is considered to be having two terms associated with the finite conductivity of standard silicon substrate. The loss tangent of lossy dielectric medium is defined as:

$$\nabla \times H = j\omega\left(\varepsilon' - j\varepsilon'' - j\frac{\sigma}{\omega}\right)E$$

$$\tan\delta = \frac{\omega\varepsilon'' + \sigma}{\omega\varepsilon'} = \tan\delta_d + \tan\delta_l$$

The first term is associated with the intrinsic loss associated with the polarization loss of the intrinsic silicon substrate and latter term is associated with the extrinsic loss from the finite conductivity of silicon substrate [5]. Electromagnetic simulation study is performed to analyze the effect of frequency variation on the electrical parameters and plot of the same is shown in Fig.2.

A band pass filter structure on HR-Si is shown at 40GHz [14] but in this article BPF over polyimide is simulated. Simulated results show that polyimide layer shift the frequency range to higher end of frequency due to change in the associated effective permittivity [11]. The effect of substrate thickness on the frequency is also studied and plotted in Fig.3 where the cut-off frequency reduces with increasing substrate height.

3. PROCESS FLOW AND IMPLEMENTATION

The standard silicon substrate (ρ~10-20, Ω-cm) is taken as a base substrate. The O/N stack is deposited over silicon using chemical vapor deposition (CVD) technique [12]. This is followed by the deposition of polyimide (top side) for which spinning speed play an important role. Curing of polyimide reduces the thickness so the step is again repeated to achieve the desired thickness. The main steps are:

- Si wafer of thickness 675μm
- Initial oxide nitride deposition. (Nitride at top and oxide at bottom)
- Single side polyimide deposition (15μm) and curing at 425°C
- Re-deposition of polyimide and curing
- Metal Al metallization - 1μm (both sides)
- Lithography and etching or ashing (Patterning)

The metal layer is deposited using sputtering and patterned employing positive photo-resist. The single mask process is used for circuit realization and the cross section schematic is shown in Fig.4.

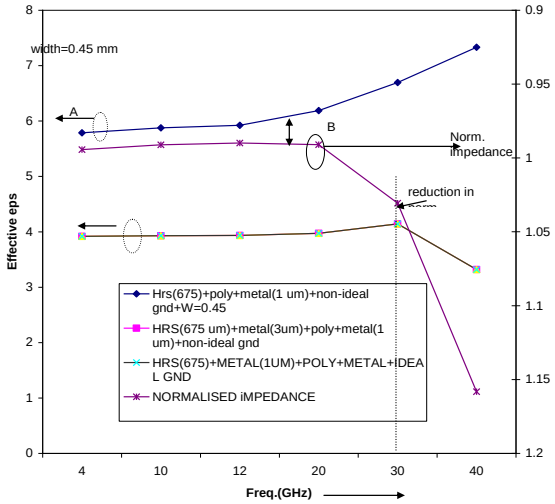

Fig.2. Frequency behavior of transmission line on various media

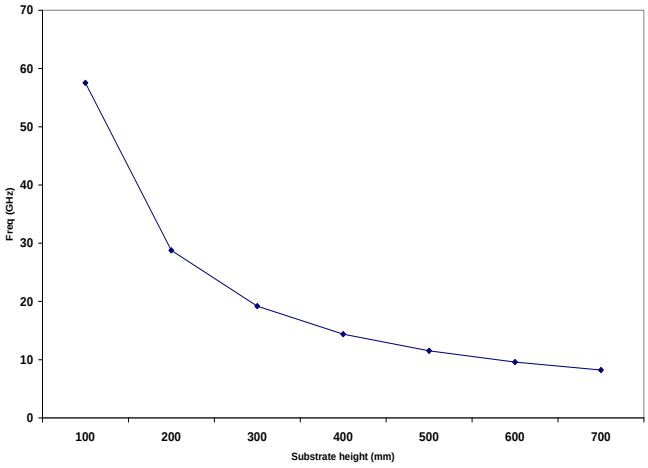

Fig.3. Effect of substrate thickness on the cut off frequency

The cross section topology and transmission line equivalence is shown in Fig.5. The circuits are fabricated on the polyimide base over silicon substrate and the same to be accounted in the design. The simulation study of the above approach is carried out with the frequency sweep and as shown in Fig.5, the losses associated with the transmission line over polyimide clearly shows minimal attenuation.

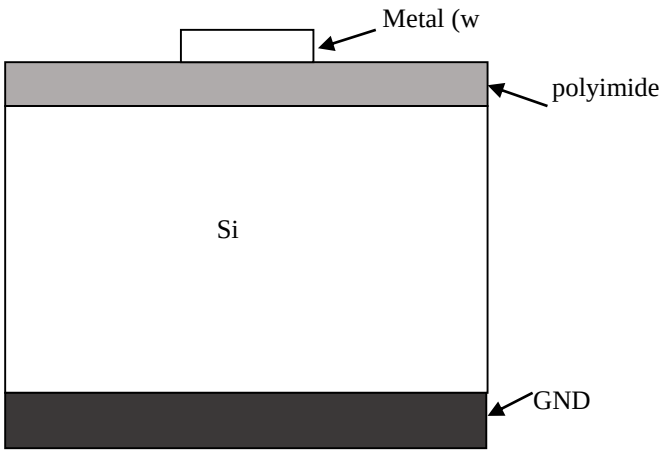

Fig.4. Cross section schematic of transmission line

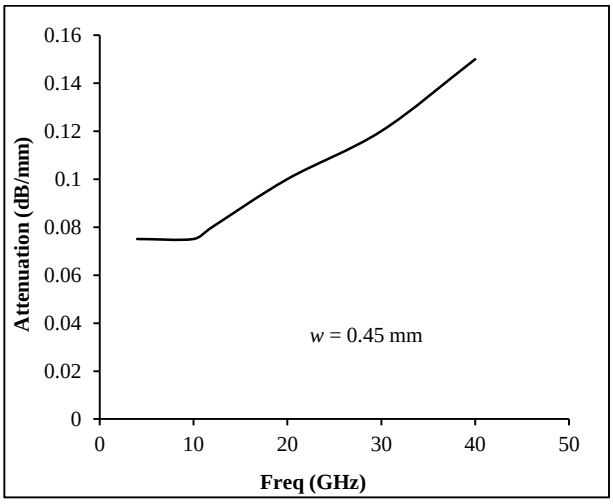

Fig.5. Simulation study of the attenuation characteristics of polyimide based TL

The realized band pass filter structures are shown in Fig.6 which is having coupled topology. The coupled lines are around 3.4mm length with the gap of 0.1mm.

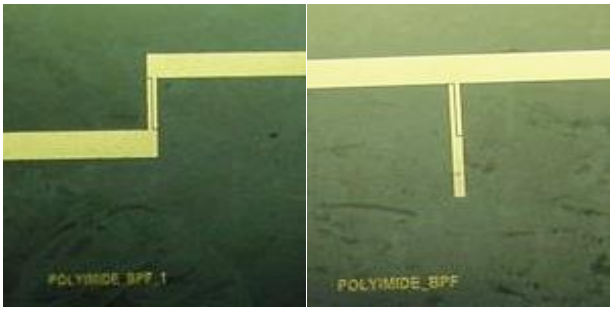

Fig.6. Fabricated BPF topology over polyimide

The Table.2 shows the comparative analysis of the losses associated with the transmission line over various options including polyimide at X-band [12].

Table.2. Loss comparison on various substrates

Feature	HRSi (675 µm)	Alumina (25 mil)	Polymide over Si
Max. Insertion loss (dB/mm)	1.3	1.0	1.01
Min. Return Loss (dB)	<25	<25	<25

It demonstrates that the process can be easily implemented to realize RF structures and the same can be extended for other frequency ranges.

4. DISCUSSIONS

Passive RF circuits on polyimide are an alternative option for RF-CMOS realization. This provides cost-effective solution besides providing ease of processing in standard foundry. Various nonconventional VLSI processes require process integration and package considerations which introduces implementation complexity. Present approach of employing polyimide over standard silicon is having inherent advantages such as: CMOS compatible process, cost effective and providing better alternative compared to alumina and quartz. Transmission line realized using this approach is characterized for losses and further the same process is employed in the realization of filter topology. This article details the modelling aspects and simple process steps for the realization of RF circuits on polyimide which will pave way for RF-CMOS integration.

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