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A MOSFET CAPACITANCE MODEL FOR ALL GATE BIASING

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Abstract

The present paper describes a modeling of the capacitance of a MOSFET operated in all regions, i.e. subthreshold linear and saturation. The model is based on the electric charges behavior under a dynamic gate biasing and sweeping the Si-SiO2 interface from deep accumulation to deep inversion. The model is based on the charge model and our I-V current model developed earlier. The proposed model which is obtained after mathematical analysis has been compared to the classical model valid each operating region, i.e., accumulation subthreshold and inversion. It has been found to be in quiet good agreements for the linear and saturation regions. In addition, our model expresses the capacitance in the subthreshold region which is not explicitly described by the corresponding classical model. The experimental data obtained on research devices are found to suite our model in all the three regions.

Keywords:

MOSFET, I-V Current Model, Capacitance Model, Gate Biasing

1. INTRODUCTION

The advancement of CMOS technology is based on the deep understanding of the MOSFET device used as the basic unit in the VLSI-ULSI Circuits [1]. Downsizing of devices resulted in many physical parameters that need be well understood in order to build reliable devices and hence reliable Integrated Circuits (ICs). Design and implementation of the basic elements relies on adequate characterization tools and modeling [2]. Device modeling is the sound for the understanding and the investigation on adequate sought device performances. Several modeling techniques and tools have been introduced recently. We can distinguish compact modeling [3],[4] which was a sound for many physical device models. In micro and nanometric devices and structures, modeling shows other constraints such as Deep Short Channel Effects (DSCE) [5] and Quantum Behaviors (QB) at ultimate dimensions [6]. Among the various device models that have been introduced, each model is based on some assumptions. These assumptions differ from one case to another. In the present case, we have introduced a model where the gate biasing is swept from accumulation to inversion. The expression of mobility variation is introduced in the gate biasing.

Our motivation is to propose a tool that can help in studying the capacitance behavior during switching operation of logic transistor. It is known that the frequency limits and leakage currents higher limits are strongly dependent on MOSFET gate capacitance. Hence, our model may help in getting a better expression of the leakage currents that affect the switching ratio I_{ON}/I_{OFF}.

The proposed model which is based on experimental study on standard experimental devices is found shows good agreements compared to various simulations using measured data for different devices operated in different gate biasing regions. In addition, the reposed model contributes to device characterization tools and can be applied for device parameters investigation and eventually for modeling using bottom up approach.

Our model shows some originality in the use of the gate biasing range, which can lead to unified capacitance model for the three biasing regions, i.e. subthreshold, linear and saturation. The mathematical coefficients introduced in the model express various physical and electrical quantities that are expressed to ease device parameter computation and extraction. Finally, the model is globally complying with experimental data in most gate bias regions.

2. THE PROPOSED MODEL

The capacitance model introduced in this work is based on the current model described in different literature and called commonly classical model. A general expression is given in Eq.(1) and some parameter substitutions have been made accordingly to comply with the short channel effects (SCE) or low dimensional device technology (LDDT) requirements. The mathematics used in the expression rearrangements and substitutions are avoided in this paper as the paper objective is not the mathematical analysis. The drain current model known as Classical Model (CM) is given in terms of drain and gate biases as:

$$I_d(V_g) = \frac{W}{L}\mu_{eff} C_{ox}(V_g - V_{th})V_d \quad (1)$$

where, W, L are the gate width and length, μ_{eff} is the carrier mobility, C_{ox} is the gate oxide capacitance, and V_{th} is the threshold voltage.

The electric charge in the channel inversion layer for the static regime is given as a function of the oxide capacitance and gate bias as follows

$$Q_{eff} = C_{ox}(V_g - V_{th}) \quad (2)$$

All symbols have their usual meanings of capacitance, voltage and threshold.

In the literature, it has been known that the effective mobility is can be expressed in terms of the standard carrier mobility by an expression including a parameter called correction factor θ_1. We have used this correction factor and introduced another correction factor θ_2.

Taking care about the SCE and LDDT effects which cause mobility degradation, the effective mobility after substitution and simplification becomes;

$$\mu_{eff} = \frac{\mu_0}{1 + \theta_1(V_{gs} - V_{th}) + \theta_2(V_{gs} - V_{th})^2} \quad (3)$$

With μ_0 the standard or initial mobility and θ_1 and θ_2 are correction factors for mobility degradation.

It is important to emphasize that in our work, two factors instead of one have been used to express the mobility degradation.

In order to use the capacitance model in the subthreshold region, we have studied the electric charge behavior in the corresponding region and used the current model we developed earlier [7]. We have introduced a correction for the channel total charge and assumed it by a hyperbolic function in terms of V_{gs}. This voltage is called effective gate voltage Vgs_{eff}.

When $(V_{gs}\text{-}V_{th}) > (\eta\varphi_t V_{th})$, V_{gseff} tends towards $(V_{gs}\text{-}V_{th})$, and after substituting using Eq.(2) and Eq.(3) in the gate voltage expression, the effective gate voltage is found to be:

$$V_{gs_{eff}} = \frac{(V_{gs}-V_{th}) - \sqrt{.V_{th}.\varphi_t} + \sqrt{(V_{gs}-V_{th})^2 + \eta.V_{th}.\varphi_t}}{2} \quad (4)$$

where, φ_t is the thermal potential and η is the threshold coefficient as introduced in this work

To suite our modeling view, the channel charge is corrected based on the gate capacitance as given in our earlier work [8] and after substitution using Eq.(4), it becomes:

$$Q_{eff} = C_{canal} V_{gs_{eff}} \quad (5)$$

As it is known the channel capacitance is a function of the gate bias and if one substitutes different terms using Eq.(3)-Eq.(5) and after mathematical analysis, the channel capacitance becomes:

$$C_{canal} = C_{ox}\left[\frac{(V_{gs}-V_{th}) + \sqrt{(V_{gs}-V_{th})^2 + \eta.V_{th}.\varphi_t}}{2\sqrt{(V_{gs}-V_{th})^2 + \eta.V_{th}.\varphi_t}}\right] \quad (6)$$

After mathematical manipulation and transformation using approximations and substitutions in Eq.(1),

$$I_{ds} = \frac{W}{L}C_{ox}\left[\frac{(V_{gs}-V_{th}) + \sqrt{(V_{gs}-V_{th})^2 + \eta.V_{th}.\varphi_t}}{2\sqrt{(V_{gs}-V_{th})^2 + \eta.V_{th}.\varphi_t}}\right].V_{gs_{eff}}.V_{ds_{eff}}.\mu_{eff} \quad (7)$$

where Vds_{eff} is given by Eq.(8).

$$V_{ds_{eff}} = \frac{(V_{ds}-V_{dsat}) + \sqrt{V_{sat}\phi_t} - \sqrt{(V_{gs}-V_{th})^2 + \beta.V_{dsat}.\varphi_t}}{2} \quad (8)$$

With β a factor related to DIBL as well short channel modelling.

The new saturation voltage is given by Eq.(9) as:

$$V_{dsat} = \frac{(V_{gs}-V_{th}) + \sqrt{(V_{gs}-V_{th})^2 + \lambda.V_{th}.\varphi_t}}{2} \quad (9)$$

and λ is a correction factor depending on V_{gs}.

The saturation regime is modified according to our earlier work done for Si MOSFETs as well as CNFETs [7] [8]. The expression used to move from classical to nanometric modeling is that given by [9].

As we reported earlier, in the saturation region current does saturate and hence shows a more or less linear evolution starting from the hard saturation of the I-V curve.

As a summary the model includes the subthreshold part, the linear part, the soft saturation and the modified saturation region as reported in [10].

The model with that given by [11] is then used and investigation on its application on device characterization is achieved

In order to confirm our results, experimental work has been achieved. This experimental work has been done at IMEP Grenoble France.

3. RESULTS AND DISCUSSIONS

A set of I-V curves measured on different devices has been achieved and a typical curve is given in Fig.1. The experiments are carried out on conventional experimental devices.

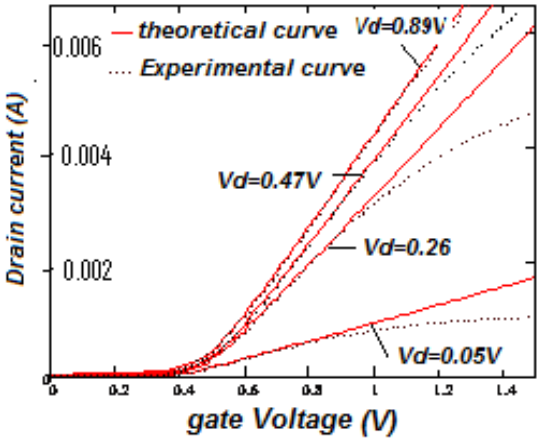

Fig.1. Drain Current-Gate Voltage variations for different Drain Bias

We can notice that as V_d gets close to 1V, theoretical and experimental curves meet and the model suites very good. We have shown only the part from below threshold to soft saturation to emphasize on the validity of the proposed model in the mentioned range.

We can see that as the drain voltage approaches 1 volt there is a good agreement between the theoretical and experimental curves for the transconductance and critical points as show in Fig.2.

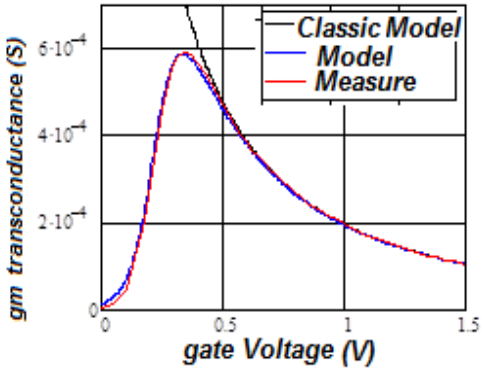

Fig.2. Transconductance Comparison between the Classical Model (black), our Model (blue) and Experimental data (red)

The model is simulated and compared to practical data obtained on MOSFET from the IMEP Grenoble France and found to be in good agreement. In addition our model suites the subthreshold region which is not modeled by the classical model including short channel effect and where experimental data are measured and found to suite our model.

Little discrepancy is observed at the staring of the saturation region which is modeled by other equations and phenomena as given by Eq.(8). The current equations given by Eq.(7), Eq.(8) and Eq.(9) confronted to experimental results showed good agreements. One has to notice that in case of low dimensional devices, there is an interdependence in phenomena in the current saturation region. Theses phenomena are mainly related to short channel effects and ultimate dimension side effects.

In order to strongly validate the model, we measured the mobility and the transconductance in terms of gate bias. We have done the plots of the three curves (classical model, proposed model and experimental data).

The mobility variation with gate bias is shown in Fig.3. Our model comes to be in good agreement with the classical model and experimental data where ever they are defined

One has to notice that the transconductance model is defined starting from V_{gs} = 0V.

In the same aspect, the mobility model behavior has been discussed and the different models have been sketched. The Fig.4 shows that the model is in a good agreement with experimental data. However, in the subthreshold region only our model that seems to give correct results.

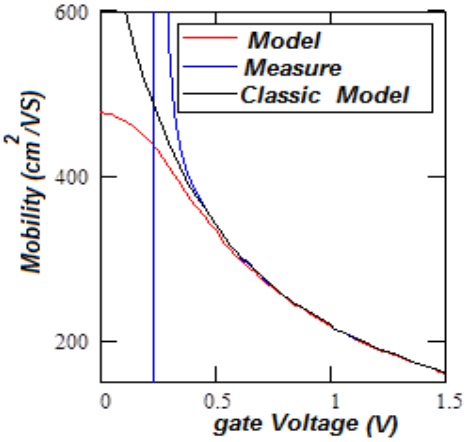

Fig.3. Comparison between the Classical Model (black), our Model (blue) and Experimental data (red)

In order to confirm our results on the capacitance measurements, we have plotted the measured and calculated values of the capacitance for both p and n channel transistors as shown in Fig.4 and for different gate voltages as shown in Fig.5. The result as are found to be in good agreement and confirms the validity of our model.

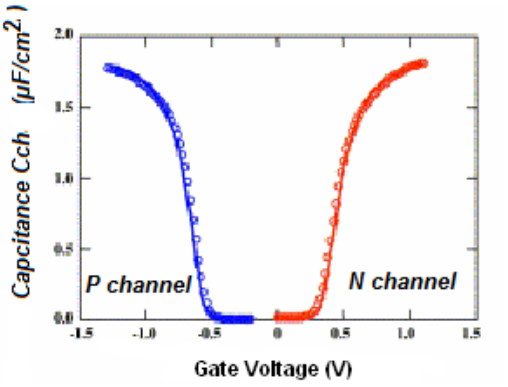

Fig.4. Experimental (symbols) and modeled (lines) C_{gc} (Vg) characteristics for N and P channel (MOSFET 10×10μm^2, C_{ox} = 1.9μF/cm^2)

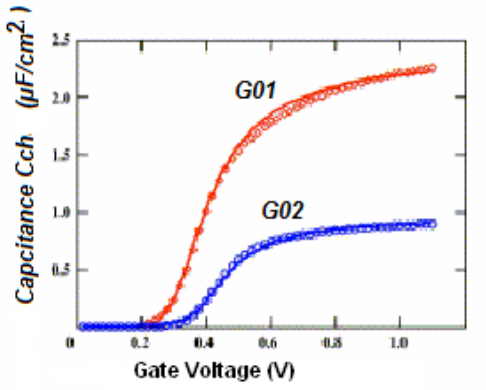

Fig.5. Experimental (symbols) and modeled (lines) C_{gc}(Vg) characteristics of two gate oxides GO_1 (C_{ox} = 2.4μF/cm^2) and GO_2 (C_{ox} = 1.0μF/cm^2) for nMOSFET

4. CONCLUSION

The present work is carried out both experimentally and theoretically, the proposed model is found to fit the experimental data in the whole range of gate voltage. To confirm the model, the experimental work has been enlarged to different sets of curves including I-V, gm-V, and mobility. The model is found experience the different variations accordingly. However, there are some discrepancies in the saturation parts of the current; this may be due to phenomena that will be investigated. The model suites the experimental data and the classical model. Moreover, it is applicable to the subthreshold region which is very interesting in device characterization. Further improvement can be done by introducing other parameters related to the low dimension effects both on channel and oxide in conjunction to the applied field. Using correspondences of experimental data and curves with the model expressions, several electrical parameters could be easily extracted. We believe that the model in conjunction with experimental data and other models will help in extracting a large variety of device parameters.

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