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DYNAMIC FIR FILTER SCHEMA USING LOW POWER BUILDING BLOCKS

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Abstract

The main objective is to design a versatile silicon chip to curtail the power consumption and to shrink the global system area. The dynamic power consumption of digital FIR filters can be reduced by employing low power building blocks. Mathematically the neurons having the components of arithmetic and logical subsystems in the whole architecture. The power optimization is achieved by low power internal units of a system such as adder and multipliers. In this research the Finite Impulse Response (FIR) filter design is made by constructing Vedic multiplier with Dual Rail Domino Logic (DRDL) logic based adders. The proposed work consists of three major concepts, initially the DRDL based homogenous adder is constructed with several bit width, then secondly the multiplier is constructed by using proposed parallel adder. Finally, the filter is designed by combining this process. To make proposed FIR filter more effective, the FIR filter with Vedic multiplier is considered. These processes are described using structural Verilog-HDL and synthesized using Cadence RTL Compiler with respect to 90nm Cadence Generic Process Design Kit (GPDK) technological library.

Keywords:

Dual Rail Domino Logic, Adder, Vertically Crosswise Multiplication, Finite Impulse Response, Power Delay Product

1. INTRODUCTION

In digital signal processing (DSP) the filters are used due to its stability, programmable filtering process and easy implementation. To satisfy the low power and high throughput, the filtering operations were performed by using adder and multiplier with low resource. Normally the FIR filter consists of 'n' number of adders and 'n+1' number of multipliers. While constructing the complex filtering operations the addition and multiplication process results in complex structure, leading to excessive area and power consumption. In order to minimize the cost of multiplier the hardware implementation is divided into two types such as multiplier-less based designs and memory based designs. The Memory-based FIR designs are divided into two types, if the process is taken by Multiple Constant Multiplication (MCM) [1] based constant multiplications and stored the result in Read Only Memory (ROM), then it is termed as Look-Up Table (LUT) methods. If the design uses bit level resources, then it is called as Distributed Arithmetic (DA) [2] methods. Normally the FIR filter response is represented by the equation,

$$Y(n) = x(n)f(n) \tag{1}$$

$$Y(n) = \sum_{k=0}^{L-1} f(k)\,x(n-k) \tag{2}$$

From the Eq.(1) and Eq.(2) the 'L' is the length of the FIR filter, $x(n)$ is the input sequence, $h(n)$ is the impulse response of the filter, $y(n)$ is the output of the FIR filter. If the above equation is represented by 'z' series, then Eq.(2) becomes, $Y(z)=x(z)f(z)$.

Several adders are used to construct the FIR filters, Franklin et al., (2014) [3] made a filter design with Ripple Carry Adder (RCA), Carry Select Adder(CSLA) using BEC (Binary to Excess-1 Converter) and CSLA using D-latch. Here the multiplication is process is made by Vedic multiplication process. Finally, Filter is designed with these adders with common multiplier.

Similar to this method the proposed method uses Dual Rail adder logic and for multiplication the Urdhya Tirbhyam Multiplier is used. This section ends in introduction part. In section 2 the detail survey is made about adders and multipliers which is used in filtering applications. In section 3, the problem is addressed and discussed about the solution. In methodology section 4, the adder, multiplier and filter concepts are made separately. Finally, experimental results were made in section 5 and the research is concluded in section 6.

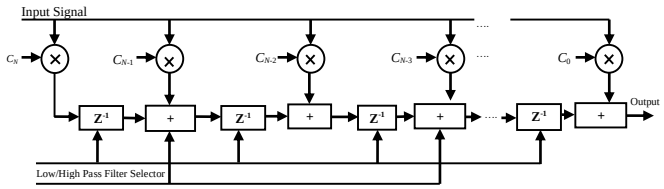

Fig.1. Representation of 'N' stage FIR filter

2. EXISTING METHOD

Martínez et al. [7] proposed a multiplier less FIR filter design, they stated the algorithm as non-recursive signed common sub expression elimination (NR-SCSE). Here two techniques were made such as graph synthesis and the classical common sub expression elimination technique.

Nehru et al. [8] proposed a 4 TAP finite impulse responses filter using Shannon based adder cell and multiplier circuit. The basic element of data path system is filters. The data path system involves adder, multiplier and memory element. The 4 TAP filter reports 3.41% improvement in switching power consumption. This circuit is analyzed using spice software with 130 µm technology. The proposed 4 TAP filter is important component of many applications like signal processing and cryptography.

Ranjini et al. [9] proposed a Finite Impulse Response (FIR) digital filter is basic component in communication systems and in many digital signal processing (DSP). FIR filter is broadly used in portable application with small area and low power. Signal decision logic and amplitude detection logic we can reduce the power of FIR filter. In FIR filter extensive variations data and in coefficients. The filter order is dynamically changed in accordance with amplitude of both filter input data and coefficients. The power of the proposed FIR filter is reduced by 5mW from previous fir filter

Karthick et al. [10] proposed a low power reconfigurable FIR filter is designed, in which the input data are monitored and the multipliers in the filter are disabled when both the coefficients and inputs are small enough to mitigate the effect on the filter output. Generally, since the amount of computation and the corresponding power consumption of FIR filter are directly proportional to the filter order, if we can dynamically change the filter order by turning off some of the multipliers, significant power savings can be achieved with minor degradation in performance. An amplitude detector block is used to monitor the inputs of the filter. A control signal generator counts the number of inputs that have small amplitude and the multipliers are disabled only when consecutive inputs are small.

Beuchat and Tessierand [4] made a survey about filtering design in digital signal processing. Huang et al. [6] presented a distributed arithmetic (DA) algorithm for Filtering applications.

3. PROPOSED METHOD

A novel design of Dual-Rail Domino Logic and Vedic Multiplier is discussed in this chapter. The adder and multiplier module is replaced in FIR filter circuit, by using Dual-Rail Domino Logic and Vedic Multiplier in order to mitigate the power consumption and to enhance the overall operation of system is described in this chapter. The most significant parameters are considered for the performance analysis of the proposed DRDL design such as power consumption, delay of the circuit and power, delay product. These parameters are used to measure the quality of the proposed circuit and to compare various circuit styles.

3.1 DUAL RAIL DOMINO LOGIC FULL ADDER

The dual rail domino logic takes true and complementary inputs and produces true and complementary outputs. The power delay product is very less in case of dual rail domino logic. Dual rail is a precharged circuit technique that can be used to enhance the speed of operation. Domino logic is comprised of a dynamic CMOS logic accompanied by a static CMOS buffer. In order to implement the required logic function the dynamic circuit is constructed with an n-MOSFET logic block, a p-MOSFET precharge transistor and an n-MOSFET evaluation transistor with clock signal applied to their gate nodes. The output node of the dynamic circuit is charged to the supply voltage level through the precharged p- MOSFET transistor during the precharge phase (CLK = 0). The output from static buffer is discharged to ground. In case of evaluation phase (CLK = 1) the dynamic circuit will stay precharged or discharged through the evaluation n-MOSFET logic block. A major benefit of dynamic logic is that power dissipation and spurious outputs can be eliminated, because of its precharge static designs styles. Dynamic logic never experiences the issue of short circuit current that stream in static circuit when a direct path from power supply to ground is provoked. In dynamic logic higher switching power dissipation occurs because every output node must be precharged during every clock cycle, certain nodes are precharged only to be instantaneously discharged again as the node is assessed in a flash. Yet in dynamic circuits, further power dissipation occurs due to the driver of the clock signal and by the distribution network. The Pipeline Scheme of DRDL is given in Fig.2.

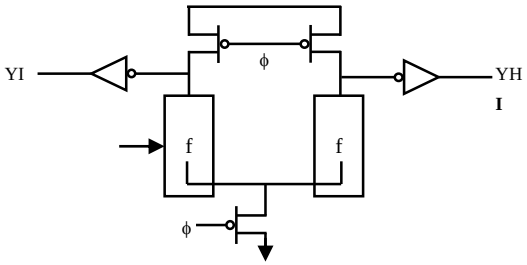

Fig.2. Dual Rail Domino Logic Full adder

3.2 VEDIC MULTIPLIER

In order to optimize the area, Urdhva Tiryagbhyam is an efficient technique in Vedic multiplier that multiplies two integers. Also, to alleviate junk output and enhance quantum cost Vedic multiplier circuits are used. The Urdhva Tiryagbhyam sutra is a general multiplication technique in Vedic multiplier and it is appropriate in all cases of multiplication. The word Urdhva means vertically and Tiryagbhyam means crosswise. The block diagram of Vedic multiplier is shown in Fig.3.

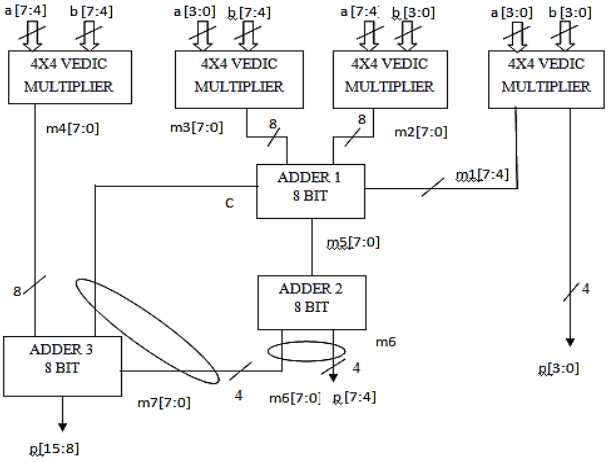

Fig.3. Vedic Multiplier – Urdhya Tiryagbhyam

Multiplication is performed vertically crosswise. The 8-bit multiplication can be performed by splitting it into two 4-bit numbers and provided as inputs to four multiplier blocks. The partial product obtained from each multiplier is added using parallel adders. The parallel adders perform addition with the help of overlapping logic fashion. The four LSB product bits B[3:0] can be obtained from one of the multipliers. The output of the second and third multiplier blocks is obtained simultaneously. Since the second and third region are overlapping it can be added directly to adder-1. The higher order bit of the first multiplier block is added to the overlapping sum of second multiplier. Final MSB bit can be obtained by appending the fourth multiplier output to the carry of first adder and higher order bits of third adder. The proposed multiplier design includes three adders.

The adder-1 consists of one half adder accompanied by seven full adders that are coupled in a ripple carry adder form. The higher order nibble of the first multiplier is added with the sum output of adder-1 by adder-2 as depicted in the Fig.4.

Adder-2 consists of three full adders, four half adders and an ex-or gate. A part of final output is obtained from the lower nibble

of adder-2. Adder-3 adds a 5-bit word and an 8-bit word. Adder-3 comprised of three half adders, four full adders and an ex-or gate. The 8-bit output of the fourth multiplier is added with the carry from the first adder and with the higher order nibble of second adder. This operation is performed by adder-3. The higher byte of the final product is obtained from the 8-bit output of adder-3. The block diagram of adder-3 is shown in Fig.5.

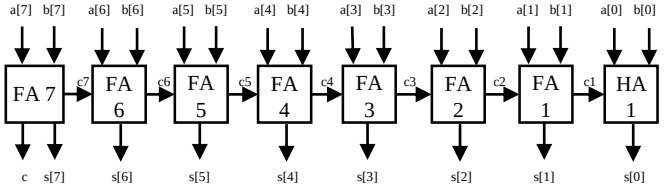

Fig.4. Block Diagram of Adder - 1

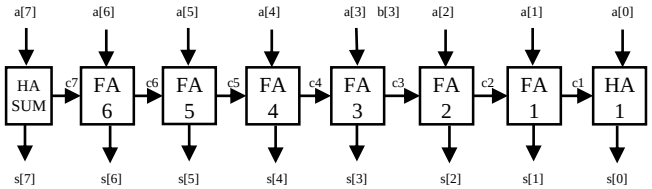

Fig.5. Block Diagram of Adder - 3

4. EXPERIMENTAL RESULTS

The proposed dual rail domino adder and Vedic multiplier based architectures are proposed in FIR filter designs are analyzed on the area, delay, total power dissipation are shown in the Table.4. These methods are described and simulated in Xilinx using Verilog-HDL and synthesized using Cadence RTL Compiler with respect to 180nm, 90nm and 45nm Cadence Generic Process Design Kit (GPDK) technological library. Simulation result of Dual rail domino adder was shown in Fig.6.

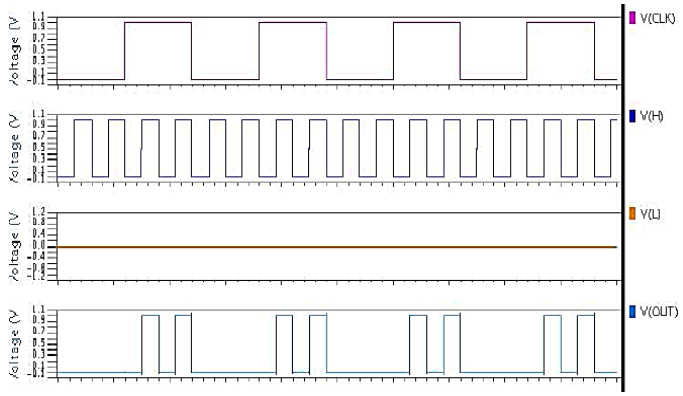

Fig.6. Waveform for Dual rail domino adder

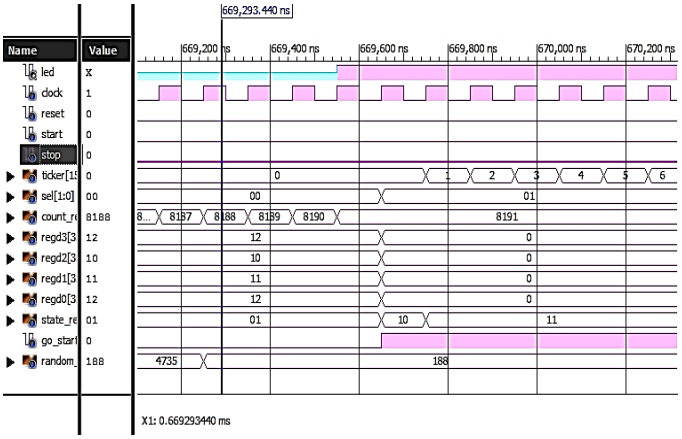

Fig.7. Wave form for Vedic Multiplier

The above waveform was Vedic Multiplier denoting the Parallel Processing operation, which was proposed in this paper.

Table.1. Simulated Result Based on 180nm, 90nm and 45nm

Parameters		Area (μm^2)	Delay (ns)	Total power Dissipation (µW)	Power Delay Product (PDP) (µW- ns)
180 nm	Adder	159	0.082	5.213	0.4274
	Vedic Multiplier	162	0.369	19.23	7.0958
	Dual Rail Domino Adder	151	0.233	16.89	3.9353
	Filter based on Vedic multiplier	436	1.632	22.56	36.817
	Proposed Filter Design	396	1.564	21.25	33.235
90 nm	Adder	83	0.062	2.650	0.1643
	Vedic Multiplier	79	0.094	9.58	0.9005
	Dual Rail Domino Adder	92	0.041	11.29	0.4628
	Filter based on Vedic multiplier	115	1.456	26.81	39.0353
	Proposed Filter Design	126	1.324	20.66	27.35384
45 nm	Adder	32	0.024	0.65	0.0156
	Vedic Multiplier	45	0.191	1.23	0.23493
	Dual Rail Domino Adder	51	0.165	1.19	0.19635
	Filter based on Vedic multiplier	62	1.263	12.36	15.61068
	Proposed Filter Design	68	0.998	09.84	9.82032

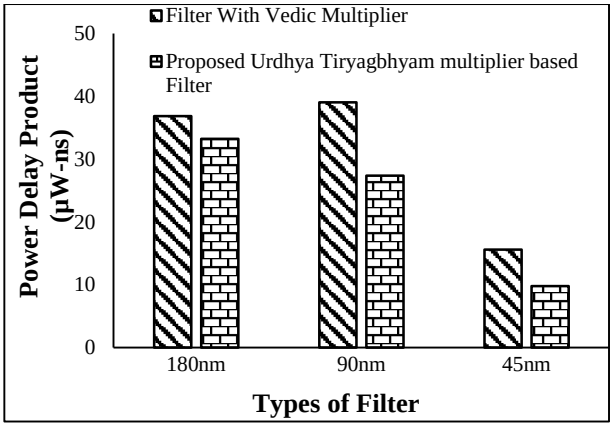

Fig.8. Power Delay Product representation for Proposed FIR filter Design

The power Delay product represents the effectiveness of designed circuit. This factor helps to implement any design in any applications. Here least value is considered as best, it is termed as switching energy. This proposed filter shows the maximum power dissipation due to dynamic and short circuit. Leakage power dissipation is negligible.

5. CONCLUSION

The proposed filtering process uses Vedic multiplier for multiplying two signed binary numbers in two's complement notation for partial product generation in that multiplier. These processes were synthesized in Cadence 180nm, 90nm and 45nm technology. Both these process combined to avoid the overflow and make a system efficient. The resource sharing is efficient and also the total power is minimized. The proposed Urdhya Tiryagbhyam multiplier based FIR filter approximately achieves 12.212% reduction in power when compared with Wallace Multiplier based FIR filter methods. The area is 9.7% more than the existing. Hence in future there is a need to concentrate in area as well as power to minimize with CMOS latest technology.

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