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COMPARATIVE ANALYSIS OF PULSE TRIGGERED FLIP FLOP DESIGN FOR LOW POWER CONSUMPTION

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Abstract

The advancement in the field of CMOS technology has motivated the research to implement more and more complicated signal processing systems on a Very Large Scale Integrated (VLSI) chip. The basic requirements of such CMOS units are to consume less power and have more functionality. The chip area, speed and power consumption are considered to be the main criteria for evaluating the quality of the systems performance. Hence, there are many types of flip flops designed based on their operation like master and slave based flip flop, conventional transmission gate flip flop and pulse triggered based flip flop. This paper, presents a different methodology using pulse triggered instead of flip flop without altering the existing design style. In this design a pulse triggered flip flop is preferred and then compared with Modified Hybrid Latch Flip Flop (MHLFF), Explicit Pulse Double Edge Triggered Flip Flop (ep-DETFF) and Adaptive Coupling Configured Flip Flop (ACFF). All the proposed flip flops have been designed using 90 nm CMOS technology and their functionality has been verified using micro wind/Dsch2 tool. From this work, the parameters like layout size, transistor count, delay and power are analyzed and compared based on the different types of flip flops. Finally, it is proved that low power Pulse triggered Flip Flop is ACFF.

Keywords:

Flip-Flop, Pulse Triggered Latch, Modified Hybrid Latch Flip Flop, Adaptive Coupling Configured Flip Flop, Explicit Pulse Double Edge Triggered Flip Flop

1. INTRODUCTION

Generally, a pulse triggered flip flop technique (PTFF) is known as one in which it can execute in a single stage instead of two stages and sometimes the PTFF acts like an edge-triggered flip flop. When there is a sufficient narrow latch present, this technique is divided in terms of two types based on their pulse generator and latch used in the circuit [1]. In implicit type of PTFF the pulse generator is present inside the flip flop, pulse generator is the built-in logic of the latch design, and no explicit pulse signals are generated. Where as in the explicit PTFF the pulse generator is present outside the flip flop. The designs of pulse generator and latch are separate a PTFF consists of a pulse generator and a latch [4].

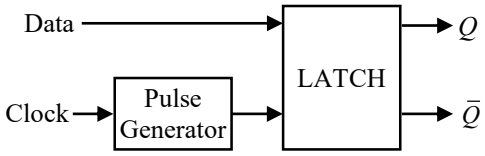

Fig.1. Triggered a D flip flop (D-FF)

The design of the proposed D Flip Flop [4] uses both Transmission gate Logic function as well as CMOS logic. Various styles in such a way that it not only reduces the number of transistors used but also it reduces the delay, Analysis of power consumption, transistor count, layout size and using various technology files are analyzed and compared [12]. Rest of the paper is organized as follows: Section 2 presents the pulsed latch technique in conventional system flip flop. Simulation results are given in section 3 and conclusions are summarized in section 4.

2. PULSE LATCH TECHNIQUE

2.1 CONVENTIONAL SYSTEM

2.1.1 Explicit Pulsed Double Edge Triggered Flip Flop (ep-DETFF) Circuit Diagram and Explanation:

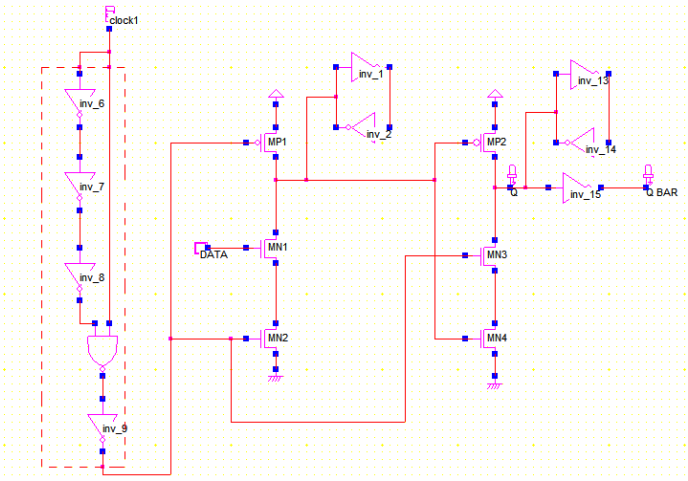

Fig.2. Explicit Pulsed Double Edge Triggered Flip Flop (ep-DETFF)

The Fig.2 illustrates ep-DETFF design and it has a NAND-logic-based pulse generator and also a semi-dynamic true-single-phase-clock (TSPC) structured latch design. A fine pulse of diminutive pulse-width. The output signal follows the input signal during this pulse. There exist few dilemmas with this design. Consider inverters inv_3 and inv_4 are used to latch data, and inverters inv_1 and inv_2 are used to hold the internal node of data between MP1 to MP2 is also called as *X* node. The pulse width is determined by the delay of three inverters. One is that during the rise of the edge, the NMOS transistors MN1 and MN2 are turned on [14] [16]. Thus if the data signal is high, node *X* shall discharge on each rising edge of the clock would operate without the loss or gain of electronic charge.

2.1.2 Modified Hybrid Latch Flip Flop (MHLFF) Circuit Diagram and Explanation:

The modified hybrid latch flip flop (MHLFF) shown in Fig.3. This also uses a static latch [11]. The keeper logic at node *X* is removed. A weak pull-up transistor MP1 controlled by the output signal Q maintains the level of node *X* when *Q* equals 0. Despite its circuit simplicity, the MHLFF design encounters two drawbacks. First, since node *X* is not pre discharged, a prolonged 0 to 1 delay is expected. The delay deteriorates further, because a level-degraded clock pulse (deviated by one VT) [19] is applied

to the discharging transistor MN3. Second, node *X* becomes floating in certain cases and its value may drift causing extra dc power. In this flip flop, the node transitions occur only when input has different logic value in two successive clocks. The operational principle of this work is explained here. When the clock (clk1) makes a transition from low to high, CLKBD remains high for a period equal to the delay of three inverters creating a transparency window. To avoid unnecessary transitions in previous hybrid logics, a modified hybrid latch flip-flop (MHLFF) is designed [14] [16].

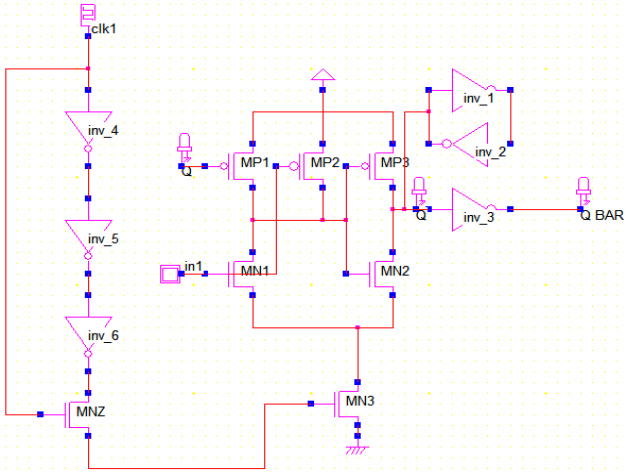

Fig.3. Modified Hybrid Latch Flip Flop (MHLFF)

2.1.3 Adaptive Coupling Configured Flip Flop (ACFF) Circuit Diagram and Explanation:

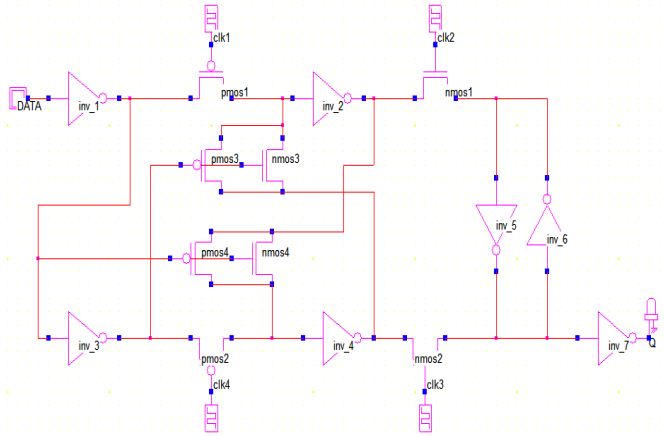

Fig.4. Adaptive Coupling Configured Flip Flop (ACFF)

The adaptive-coupling-configured FF design ACFF design leads in power efficiency because it uses a simplified PMOS latch design [11] and exhibits a lighter loading to the clock network (only four MOS [13] transistors are connected to the clock source directly). Its power efficiency is even more significant in the cases of zero or low input data switching activity [18]. Although the ACFF design leads in power efficiency, its power-delay performance is inferior to the other methods. Since pulse generation circuits are sensitive to process variations. The Fig.3 explains the basic concept of ACFF. The conventional TGFF has 2 inverters of clock buffers, which persistently consume power in every clock cycle, even at low data activity [15]. To remove these clock buffers, we consider a differential master-slave topology, shown in the lower left portion of the figure. However, the circuit is susceptible to process variations, because PMOS pass gates are too weak to pass through a substantially large drain current, in order to overcome the strong coupling in state-retention circuitry during a transition. We introduce a new method, the adaptive-coupling scheme, which configures ACFF such that the state-retention coupling is weakened if the input state is different to its internal state. This enables a transition to be easily performed, and allows ACFF to have a good tolerance to process variations. An adaptive-coupling element (ACE) is comprised of one PMOS and one NMOS, configured in parallel, and the gates are controlled by the same data signal. Consider the ACE circled in the right portion of the figure. If the gate level is high (BN node is high, B node is low), the PMOS is switched off, and the NMOS is switched on, weakening the charging ability of the G-F path. This enables the state of node F to be easily lowered to V_{DD}-V_t, during discharging through the F-B path. Since a PMOS pass gate is between the F-B paths, node F cannot be completely discharged. When node G turns into a low state by charging of node FN, node F is completely discharged to 0V through the F-G path, since the ACE NMOS allows a strong discharge current.

Flip-Flop (FF) is basically used as a memory elements in Digital circuits like Microprocessors [12] [13]. In the present scenario, power consumption [17] is a major challenge in Digital design. FF is divided into two stages, one stage is the clock system and the other is a latch that which stores data. In a conventional FF, Clock system consumes 50% of the total power which is due to the fact that the dynamic power in a MOS circuit is directly proportional to the switching activity. To reduce a drawback on Pulse-triggered Flip-Flop (P-FF) is introduced, because of a single latch is better than conventional master slave FF and transmission Gate (TG).

3. RESULT AND DISCUSSION

3.1 SIMULATION RESULTS AND WAVEFORM OF EXPLICIT PULSE DOUBLE EDGE TRIGGERED FLIP FLOP (EP-DETFF)

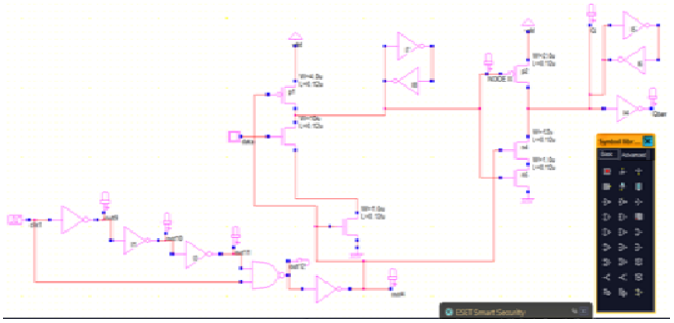

Fig.5. Circuit diagram of ep-DETFF

The Fig.5 shows this circuit diagram for Explicit Pulse Double Edge Triggered Flip Flop (ep-DETFF).

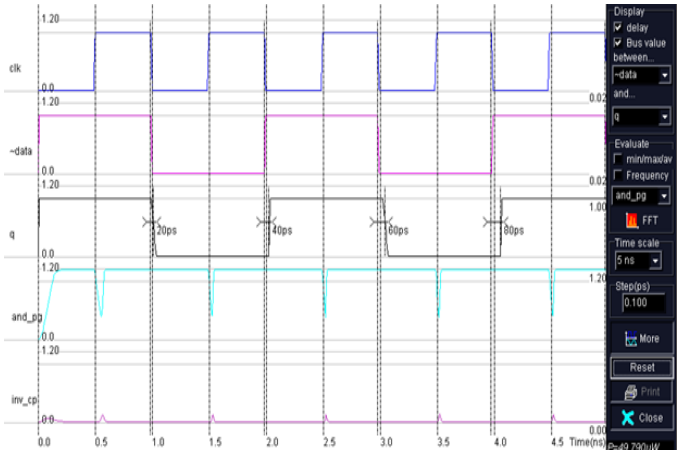

Fig.6. Simulation Waveform of ep-DETFF

The Fig.6 shows the simulated result for ep-DETFF. It can be seen that the average power of 24.1µW in 90nm technology file.

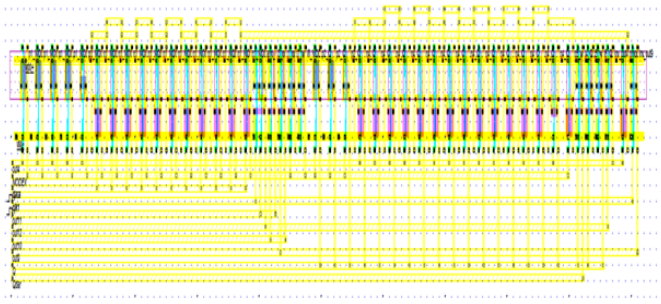

Fig.7. Layout design of ep-DETFF

The Fig.7 shows the layout design for ep-DETFF. It can be seen that the structure of layout design in 90nm technology file.

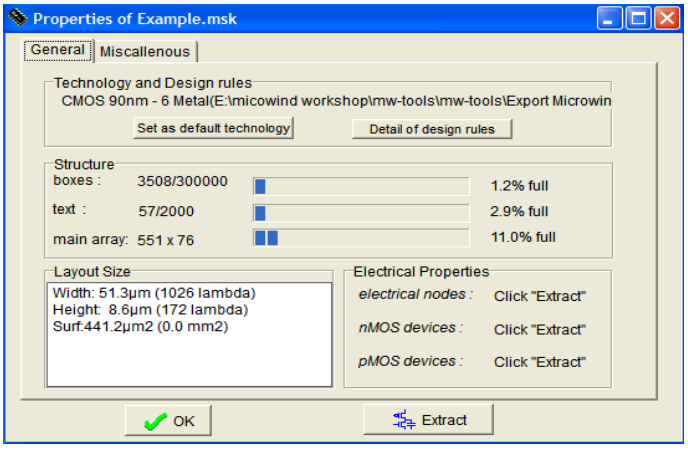

Fig.8. Analysis of layout size of ep-DETFF

The Fig.8 shows the Analysis of layout size for ep-DETFF. It can be identified that the layout area like surface, width, height, number of transistor using 90nm technology file.

3.2 SIMULATION RESULTS AND WAVEFORM MODIFIED HYBRID LATCH FLIP FLOP (MHLFF)

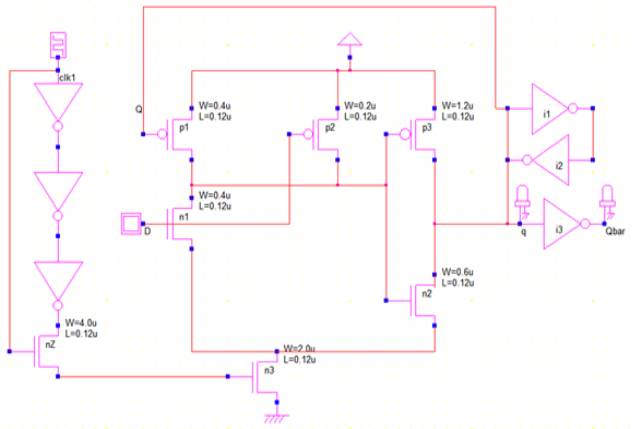

Fig.9. Circuit diagram of MHLFF

The Fig.9 shows the circuit diagram for Modified Hybrid Latch Flip Flop (MHLFF).

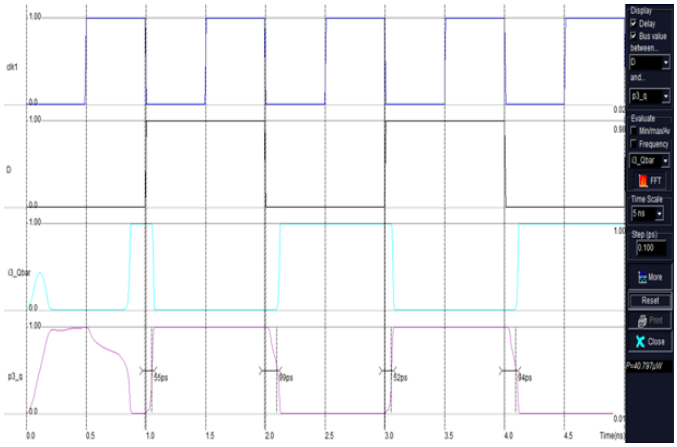

Fig.10. Simulation Waveform of MHLFF

The Fig.10 shows the simulated result for MHLFF. It can be seen that the average power of 40.7µW in 90nm technology file.

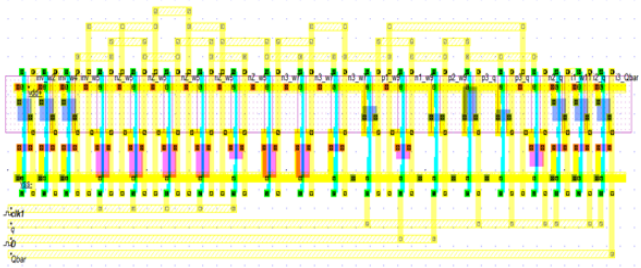

Fig.11. Layout design of MHLFF

The Fig.11 shows the layout design for MHLFF. It can be seen that the structure of layout design in 90nm technology file.

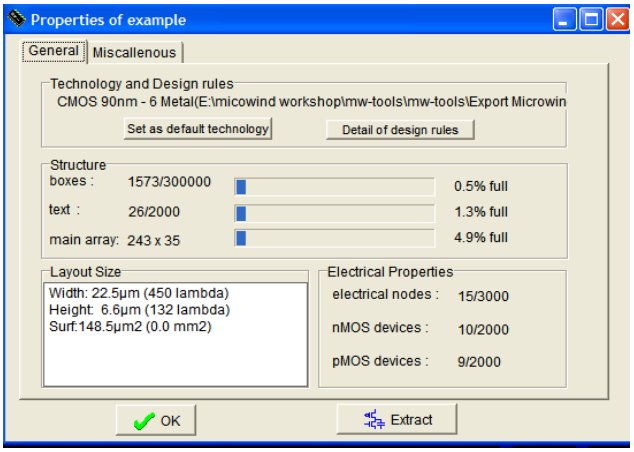

Fig.12. Analysis of layout size of MHLFF

The Fig.12 shows the Analysis of layout size for MHLFF. It can be identified that the layout area like surface, width, height, number of transistor using 90nm technology file.

3.3 SIMULATION RESULTS AND WAVEFORM OF ADAPTIVE COUPLING CONFIGURED FLIP FLOP (ACFF)

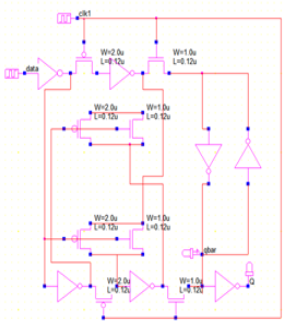

Fig.13. Circuit diagram of ACFF

The Fig.13 shows the circuit diagram for Adaptive Coupling Configured Flip Flop (ACFF).

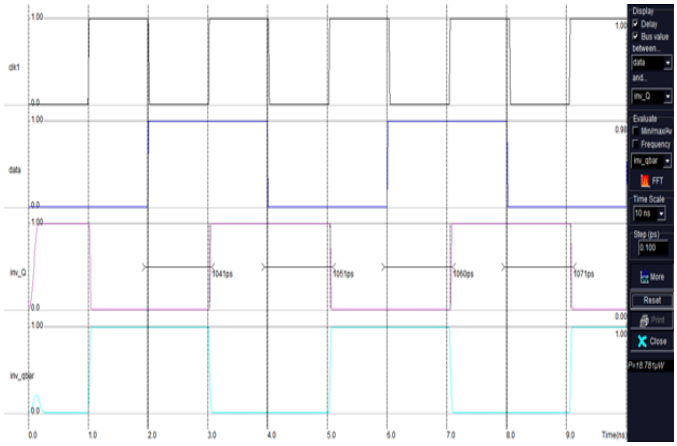

Fig.14. Simulation Waveform of ACFF

The Fig.14 shows the simulated result for ACFF. It can be seen that the average power of 22.28µW in 90nm technology file.

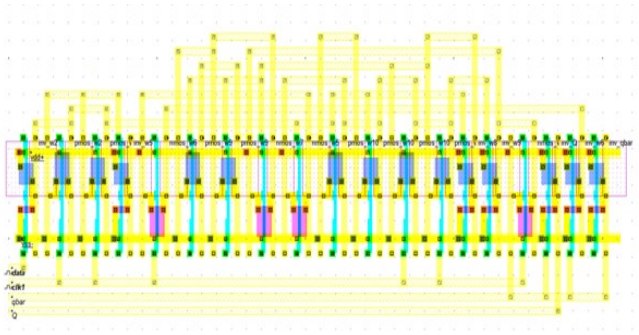

Fig.15. Layout design of ACFF

The Fig.15 shows the layout design for ACFF. It can be seen that the structure of layout design in 90nm technology file.

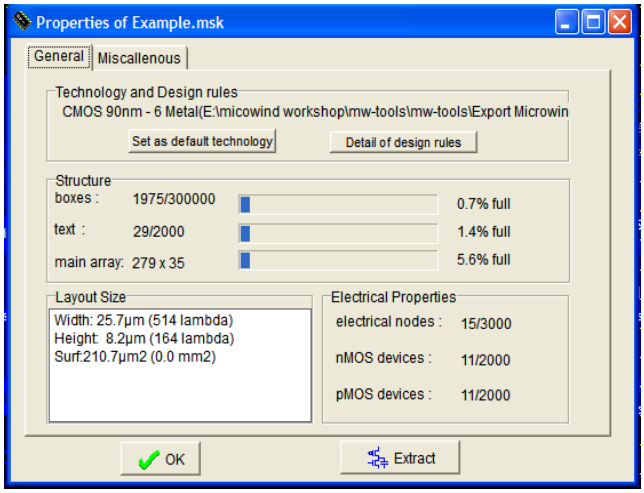

Fig.16. Analysis of layout size of ACFF

The Fig.16 shows the analysis of layout size for ACFF. It can be identified that the layout area like surface, width, height, number of transistor using 90nm technology file.

3.4 ANALYSIS REPORT

Table.1. Comparative analysis of various parameters in flip flop

Type	Layout (μm^2)	Transistor Count	Delay	Power (µw)
Ep-DCO	441.2	28	23ps	24.1µW
MHLFF	148.5	19	66ps	40.7µW
ACFF	210.7	22	15ps	22.28µW

The MHLFF is simple and easy to design. When comparing these flip flop designs, the propagation delay of Adaptive Coupling Configured Flip Flop (ACFF) has least count as 15ps. Finally, the explicit pulse Double Edge Triggered Flip Flop (ep-DETFF) has huge layout and transistor count. Comparative analysis [11] is shown in Table.1.

4. CONCLUSION

In this paper, the comparisons of various low power pulse triggered flip design is analyzed with several parameters like power, Layout, transistor count and delay. From the experimental

results it is noticed that the Modified Hybrid Latch Flip Flop (MHLFF) is almost least transistor count of 19ps. Similarly, the low power flip flop design is identified as Adaptive Coupling Configured Flip Flop (ACFF) as 22.28µW. The Explicit Pulse Double Edge triggered Flip Flop (ep-DETFF) has limitations of high transistor count and occupies large area. The ep-DETFF has 2.27µW power differences when comparing it with Adaptive Coupling Configured Flip Flop. Similarly, the Modified Hybrid Latch Flip Flop has the power difference of 50% and 58.0645% when comparing with ep-DETFF and ACFF respectively. From the result it has been found that for the best performance of power and delay it is analyzed that ACFF is best choice to use in the circuit. In future it can be extended to implement the N-stage shift register and find the possibility of memory designs.

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