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POWER EFFICIENT HIGH SPEED ADAPTIVE BIASED OPERATIONAL AMPLIFIER

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Abstract

This paper presents a new adaptive biasing technique for improving the slew rate of CMOS opamps without increasing the power consumption. All the proposed circuits for adaptive biasing are implemented using a current subtractor and NMOS based circuit. Further, the input stage of opamp in proposed circuits were substituted by Flipped Voltage Follower circuit and Self Cascode structure to study their effects on adaptive biasing circuits. The conclusion of this work is that there is a notable enhancement in slew rate, settling time and power dissipation in proposed adaptive biasing techniques. All the circuits have been designed using 180nm CMOS technology and simulated using cadence virtuoso.

Keywords:

Adaptive Biasing, Opamp, Slew Rate, Flipped Voltage Follower, Self Cascode, Power Dissipation

1. INTRODUCTION

Operational amplifier (Opamp) is a fundamental building block in analog/mixed signal systems. Its application ranges from low-dropout regulator (LDO), phase-locked loops (PLL) etc. to ADCs/DACs. The increasing demand for energy-efficient systems brings forth the need for ultra-low-power and small-sized analog circuits [1-3]. It is not only required to design a circuit in small size using low voltage but also it equivalently important to increase the device operation by increasing its operating speed. The usual method to reduce power consumption is to decrease the supply voltage. However, reducing supply voltage is not a good option because it decreases the dynamic range of circuits and the circuit suffers from problems such as bandwidth and slew rate limitations etc. The opamps particularly suffer from problems such as short-channel effects which degrade its performance [4-6]. Hence, new novel circuits and techniques may be required in low-power analog circuits. In recent years, circuits operating in the subthreshold region has gained importance because of the need for low voltage and low power operated circuits. However, operating transistors in this region give a comprehensive trade-off between high speed and low power. To neutralize this trade-off adaptive biasing technique is used [7]-[10].

The concept behind Adaptive biasing is that the biasing current changes the value depending on the applied differential voltage [11]. This method produces bias current only in the presence of input voltage. Hence, the bias current is signal conditioned. This reduces the power consumption without affecting the circuit dynamic performance.

The rest of the paper is divided into different sections. A brief explanation about slew rate and the adaptive bias circuits used is given in section 2. Section 3 contains the simulations of the circuits along with transient analysis and a comparison table. Section 4 concludes the paper.

2. SLEW RATE AND ADAPTIVE BIAS CIRCUITS

Slew rate is defined as the rate of change of output with respect to time. Its unit is V/μs or V/ms.

$$\text{Slew Rate} = \frac{dV_0}{dt} \tag{1}$$

Slew rate for an opamp is an essential factor to estimate how fast the output catches the input. In an opamp to increase the slew rate, the tail current has to be increased. The tail current is not only crucial for improving slew rate, but also for wide common mode range and improved CMRR.

$$\text{Slew rate for opamp} = \frac{I_{tail}}{C_L} \tag{2}$$

Instead of applying a tail current source or a pulsed current source, which leads to more power dissipation, an adaptive biasing technique can be used to control the tail current which not only increases the tail current but also contributes to lesser power consumption.

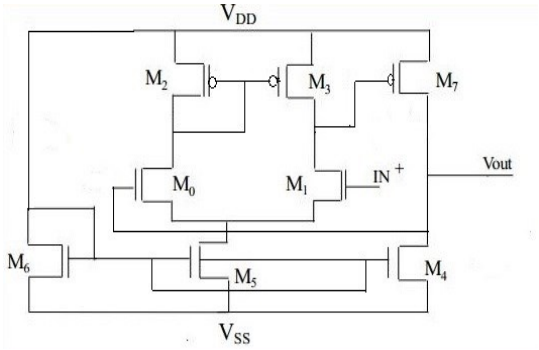

Fig.1. Opamp configured a voltage follower

Opamp as voltage follower was chosen as the base circuit. Fig.1 shows this circuit where input pair (M_1, M_2) of the input stage has been constructed using NMOS transistor. Here, p-channel transistors M_2 and M_3 act as current mirrors and they are perfectly matched. They are used in the input stage. Likewise, M_0 and M_1 are perfectly matched as well. The next stage is comprised of a NMOS based common source amplifier (M_4) and PMOS based current source load (M_7). A pulse of 1.65V was applied at the non-inverting terminal with a frequency of 1Khz. The output is partly feedback to the input hence known as a voltage follower configuration. On performing the transient analysis, it was found that the slew rate was quite low.

Two adaptive bias circuits were used to increase the slew rate of opamp based voltage follower. The Fig.2 shows a NMOS-based adaptive circuit, which is utilized to direct the tail current utilizing input voltage signal itself. It adaptively increases the tail

current and the output stage transient current for slew rate calculation.

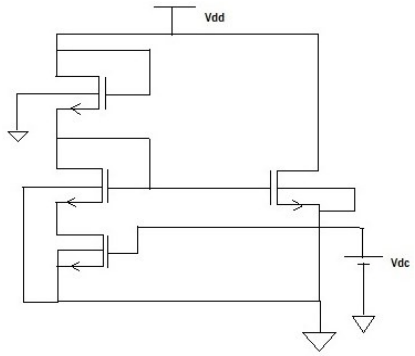

Fig.2. NMOS based Adaptive bias circuit

A NMOS-based adaptive circuit was used to regulate the tail current using input signal itself. It adaptively increases the tail current and the output stage transient current for slew rate calculation.

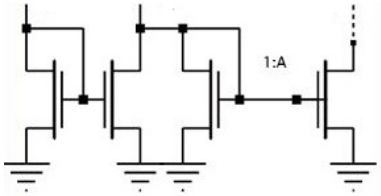

Fig.3. Current Subtractor as Adaptive bias circuit

Another Adaptive biasing circuit used was Current subtractor as shown in Fig.3. To increase the tail current in opamp, current sources are added to bias the transistors. These current sources can be realized using Current subtractor. Using this adaptive bias circuit not only the slew rate limitation was eliminated but also the power dissipation was greatly reduced.

The two adaptive biasing circuits (in Fig.2 and Fig.3) were used in Opamp based voltage follower and transient analysis was done to examine the slew rate, settling time and power dissipation. Later, the input differential stage was substituted by Flipped voltage follower (FVF) and self cascode stage and the same adaptive bias circuits (in Fig.2 and Fig.3) were used to do comparative analysis on slew rate. The performance of all proposed amplifiers are summarized and compared in Table.1, Table.2 and Table.3 respectively.

3. SIMULATIONS AND PERFORMANCE ANALYSIS

All the circuits have been designed using 180nm technology and simulated in Cadence Virtuoso. In all the proposed circuits (Fig.1-Fig.6), the supply voltage of 1.8V has been used and a pulse wave of 1.65V is applied as one of the input.

The Fig.4 shows the internal circuitry of opamp as a voltage follower. At the non-inverting terminal, the input signal is applied whereas towards the inverting terminal the output is partially fed-back in the operational amplifier.

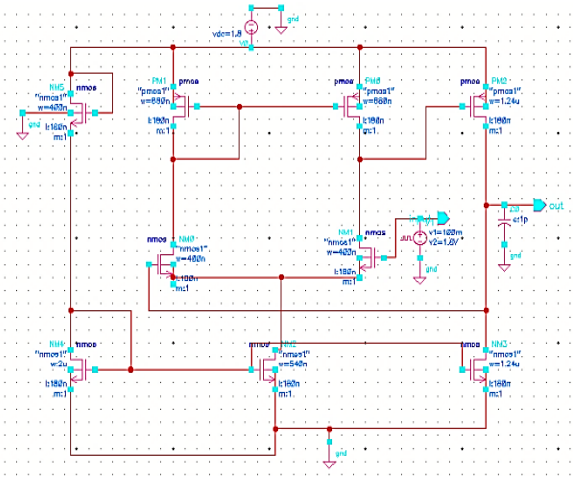

Fig.4. Opamp as a voltage follower (Base circuit)

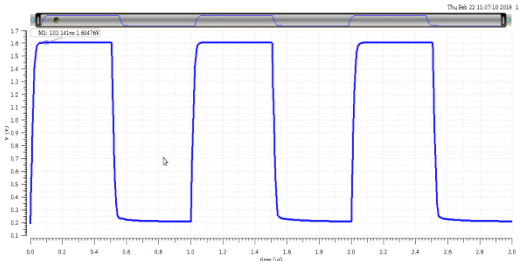

Fig.5. Transient Response and settling time of Opamp as voltage follower

The Fig.5 shows the transient response of conventional opamp as voltage follower. Transient response shows that the output follows the input. Settling time is found to be 103.14ns. Positive and negative slew rate is calculated by calculating the slope of rising and falling waveform. It is found to be 100.60(V/µs) and 57.70(V/µs) respectively. The average slew rate is 103.14(V/µs).

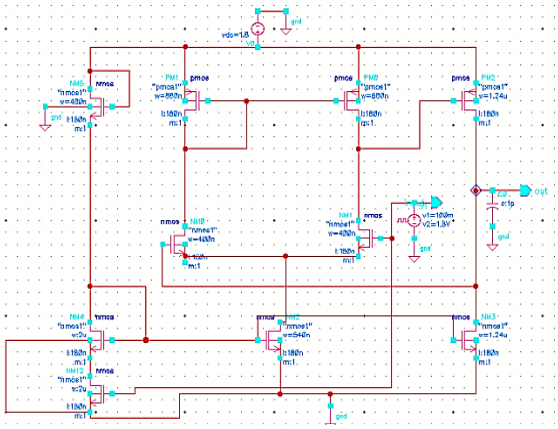

Fig.6. NMOS based adaptive biasing circuit used in base circuit (Proposed 1)

The NMOS based adaptive bias circuit incorporated in conventional opamp as voltage follower is shown in Fig.6. Here, input is applied in the non-inverting node of opamp. In the inverting terminal of the opamp, the output is partially fed-back. Here, NM12 transistor is newly added to the circuit of the conventional opamp. In the reference side of the biasing current mirror has been added.

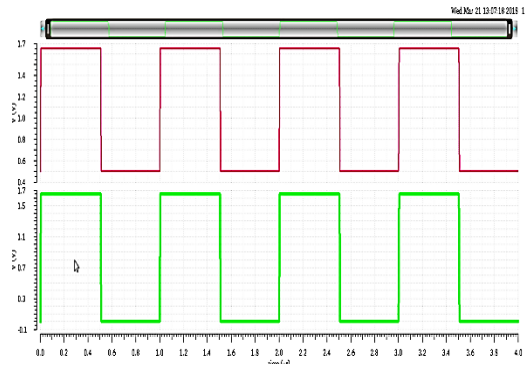

Fig.7.Transient Response of opamp with NMOS based adaptive biasing circuit

The Fig.7 shows the transient response of NMOS based adaptive bias opamp as voltage follower. Positive and negative slew rate is calculated by calculating the slope of rising and falling waveform. It is found to be 180(V/µs) and 70(V/µs) respectively. The average slew rate is calculated to be 142.40(V/µs).

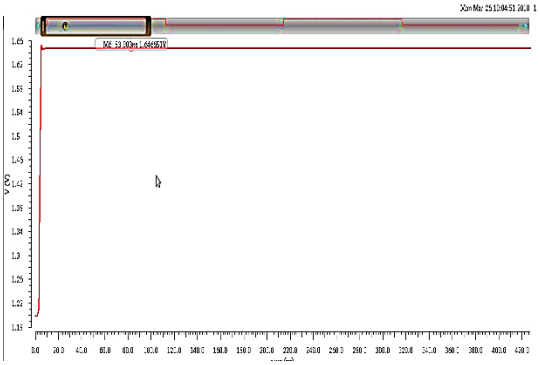

Fig.8. Settling time of opamp with NMOS based adaptive biasing circuit

The Fig.8 shows the expanded transient response of the output. This is done to find out the settling time. Settling time of NMOS based adaptive bias opamp as voltage follower is found to be 83ns

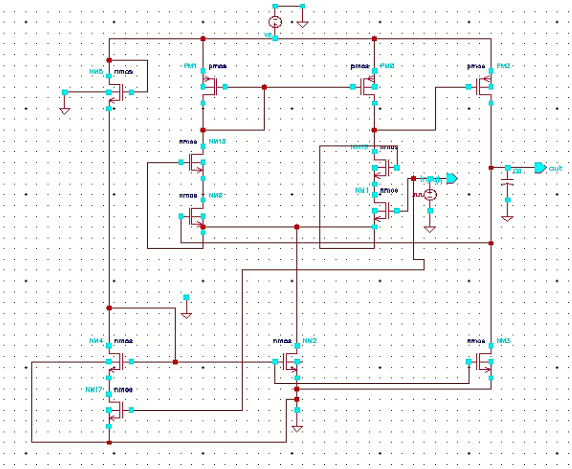

Fig.9. NMOS based adaptive bias circuit with FVF based input stage in base circuit (Proposed 2)

The Fig.9 shows the NMOS based adaptive bias circuit with FVF based input incorporated in conventional opamp as voltage follower. FVF here acts as level shifters. Here, input is applied in the non-inverting node of opamp. Towards inverting terminal of the opamp. The output is partially fed-back. Here, NM12 transistor is newly added to the circuit of the conventional opamp. It is added at the reference side of the biasing current mirror.

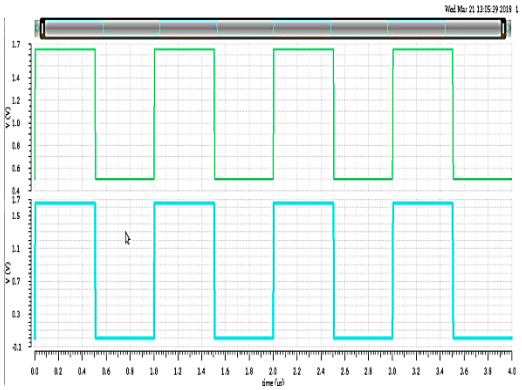

Fig.10. Transient Response of NMOS based adaptive bias circuit and FVF

The Fig.10 shows the transient response of NMOS based adaptive bias with FVF on the input stage in opamp as voltage follower. Positive and negative slew rate is calculated by calculating the slope of rising and falling waveform. It is found to be 197(V/µs) and 106(V/µs) respectively. The average slew rate is 151.15(V/µs).

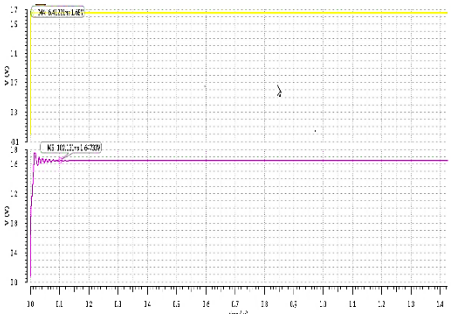

Fig.11. Settling time of NMOS based adaptive bias circuit and FVF

The Fig.11 shows the expanded transient response of the output. This is done to find out the settling time of the output. Settling time of NMOS based adaptive bias with FVF as input stage in opamp as voltage follower is found to be 102.131ns.

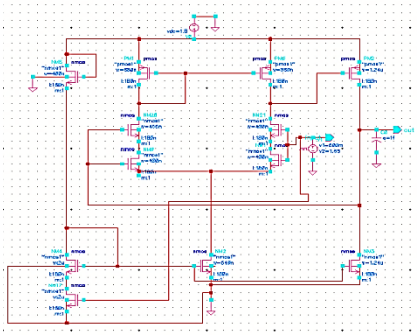

Fig.12. NMOS based adaptive bias circuit with Self-cascode based input stage in base circuit (Proposed 3)

The Fig.12 shows the NMOS based adaptive bias circuit with Self-cascode based input incorporated in conventional opamp as voltage follower. Self-cascode further enhances the slew rate and the settling time. Here, input is applied in the non-inverting node of opamp. In the inverting terminal of the opamp, the output is partially fed-back. Here, NM12 transistor is newly added to the circuit of the conventional opamp. It is added at the reference side of the biasing current mirror.

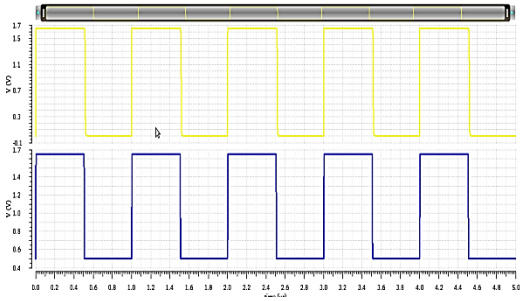

Fig.13. Transient Response of NMOS based adaptive bias circuit and Self-cascode

The Fig.13 shows the transient response of NMOS based adaptive bias with Self-cascode on the input stage in opamp as voltage follower. Positive and negative slew rate is calculated by calculating the slope of rising and falling waveform. It is found to be 205(V/µs) and 130(V/µs) respectively. The average slew rate is 165(V/µs).

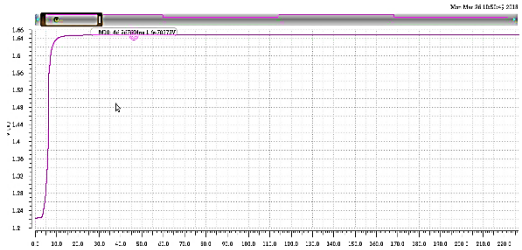

Fig.14. Settling time of NMOS based adaptive bias circuit with Self-cascode based input stage in base circuit

The Fig.13 shows the expanded transient response of the output. This is done to find out the settling time of the output. Settling time of NMOS based adaptive bias with self-cascode as input stage in opamp as voltage follower is found to be 46.276ns which is far better than the conventional opamp as voltage follower.

The Fig.14 shows the internal circuitry of opamp as a voltage follower with current subtractor as the adaptive bias circuit. The feedback current due to this adaptive bias circuit temporarily increases the bias current which helps the output to quickly catch the input. Here, input is applied in the non-inverting node of opamp. In the inverting node of the opamp, the output is partially fed-back.

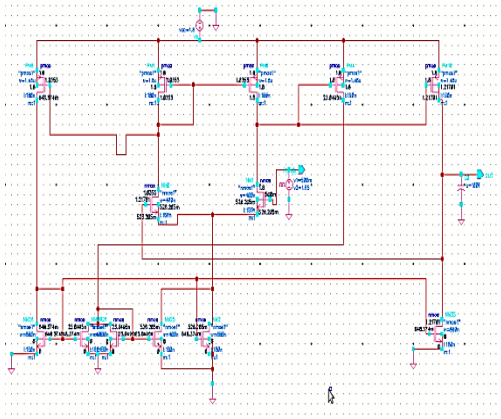

Fig.14. Current Subtractor as Adaptive biasing circuit in base circuit (Proposed 4)

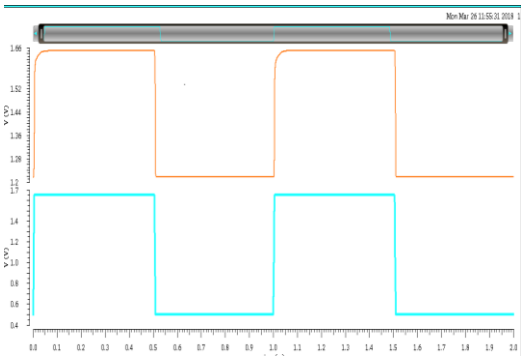

Fig.15. Transient Response of Current Subtractor as Adaptive biasing circuit in opamp

The Fig.15 shows the transient response of current subtractor based adaptive bias in opamp as voltage follower. Positive and negative slew rate is calculated by calculating the slope of rising and falling waveform. It is found to be 198.5(V/µs) and 107.5(V/µs) respectively. The average slew rate is 153(V/µs).

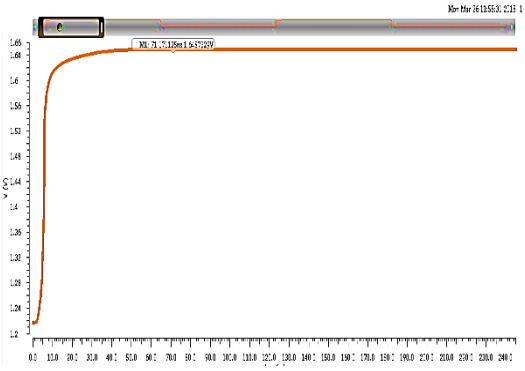

Fig.16. Settling time of Current Subtractor as Adaptive biasing circuit in opamp

The Fig.16 shows the expanded transient response of the output. This is done to find out the settling time of the output. Settling time of Current substractor adaptive bias opamp as voltage follower is found to be 71.17ns which is far better than compared to conventional opamp as voltage follower and NMOS based adaptive bias opamp.

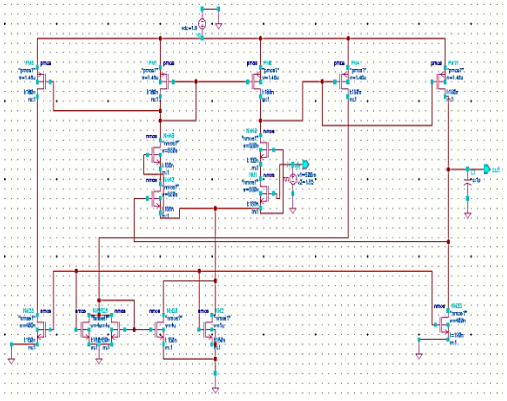

Fig.17. Current Subtractor as Adaptive biasing circuit FVF based input stage in base circuit (Proposed 5)

The Fig.17 shows the internal circuitry of Current Subtractor as Adaptive biasing circuit with FVF based input stage. The feedback current due to this adaptive bias circuit temporarily increases the bias current which helps the output to quickly catch the input. The FVF acts as a level-shifter here. This input is applied in the non-inverting node of opamp. In the inverting terminal of the opamp. the output is partially fed-back.

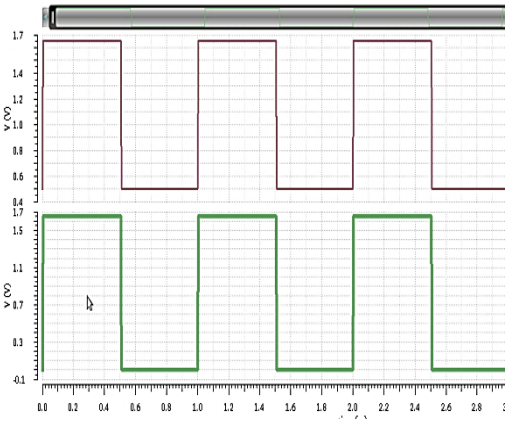

Fig.18. Transient Response of Current Subtractor as Adaptive biasing circuit in FVF based opamp

The Fig.19 shows the transient response of current subtractor based adaptive bias with FVF as input stage in opamp as voltage follower. Positive and negative slew rate is calculated by calculating the slope of rising and falling waveform. It is found to be 203(V/µs) and 134(V/µs) respectively. The average slew rate is 168.50(V/µs).

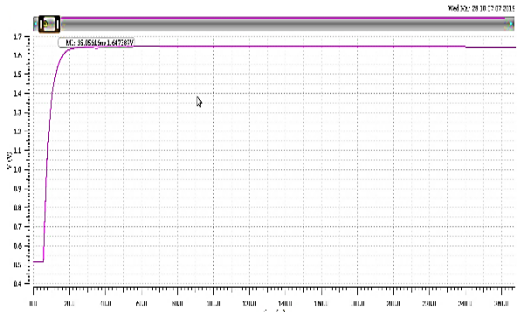

Fig.20. Settling time of Current Subtractor as Adaptive biasing circuit in FVF based opamp

The Fig.20 shows the expanded transient response of the output. This is done to find out the settling time of the output. Settling time of Current subtractor adaptive bias with FVF as input stage in opamp as voltage follower is found to be 35.95ns.

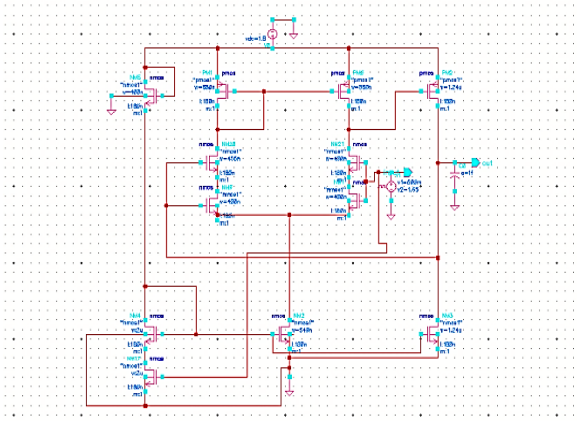

Fig.21. Current Subtractor as Adaptive biasing circuit Self-cascode based input stage in base circuit (Proposed 6)

The Fig.21 shows the internal circuitry of Current Subtractor as Adaptive biasing circuit with Self-cascode based input stage. The feedback current due to this adaptive bias circuit temporarily increases the bias current which helps the output to quickly catch the input. Here, input is applied in the non-inverting node of opamp. In the inverting terminal of the opamp. The output is partially fed-back.

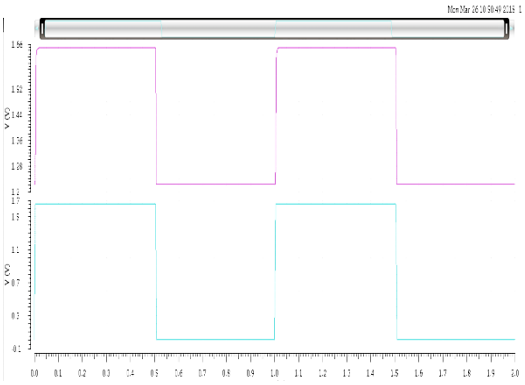

Fig.22. Transient Response of Current Subtractor as Adaptive biasing circuit in Self cascode based opamp

The Fig.22 shows the transient response of current subtractor based adaptive bias with Self-cascode as input stage in opamp as voltage follower. Positive and negative slew rate is calculated by calculating the slope of rising and falling waveform. It is found to be 293(V/µs) and 206(V/µs) respectively. The average slew rate is 249.50(V/µs).

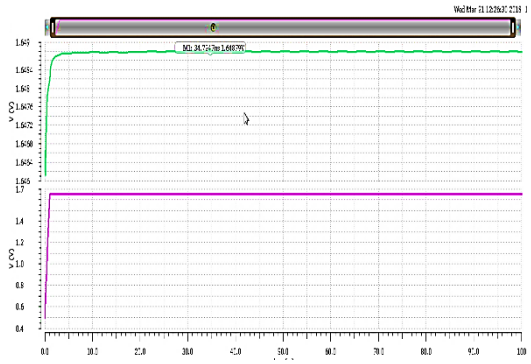

Fig.23. Settling time of Current Subtractor as Adaptive biasing circuit in Self cascode based opamp

The Fig.23 shows the expanded transient response of the output. This is done to find out the settling time of the output. Settling time of Current subtractor adaptive bias with Self-Cascode as input stage in opamp as voltage follower is found to be 34.724ns.

Table.1. Comparison table of opamp based on voltage follower, NMOS based and current subtractor based adaptive biasing circuit

Parameters	Base Circuit (Fig.4): Opamp Based Voltage Follower	Proposed 1 (Fig.6): Base Circuit+ NMOS based Adaptive Biasing Technique	Proposed 4 (Fig.14): Base Circuit + Current Subtractor as Adaptive Bias Circuit
Slew rate (+) (V/μs)	100.60	180	198.5
Slew rate (+) (V/μs)	56.70	70	107.50
Average slew rate (V/μs)	78.60	142.40	153
Settling time (ns)	103.14	83	71.17
Power dissipation (μW)	201.134	63.99	50.14

From Table.1, It is concluded that Proposed 4 circuit has a slew rate, 7.44% greater than Proposed 1 and 97.31% greater than the base circuit. It has a settling time improvement by 14.25% compared to Proposed 1 circuit and power dissipation of 50.14uW which is 21.64% better than Proposed 1 circuit. Hence we can say that current subtractor based adaptive bias circuit is better than NMOS based adaptive bias circuit. Similarly, proposed 1 circuit gives better settling time and power dissipation compared to the conventional opamp as a voltage follower.

The Table.2 shows the comparison of Proposed 2 and Proposed 5 circuit. Proposed 5 has 9.43% greater than Proposed 2. It has a settling time of 35.95ns which is 64.68% better than Proposed 2 circuit. Similarly, the power dissipation is 2.07% better when compared to Proposed 2. Hence, current subtractor works as an adaptive biasing circuit that proves to be better than NMOS based adaptive bias circuit.

Table.2. Comparison table of opamp with FVF at input stage, NMOS based and current subtractor based opamp

parameters	Proposed 2 (Fig.9): Base circuit with FVF at input stage + Adaptive biasing technique	Proposed 5 (Fig.17): Base circuit with FVF at input stage + Current subtractor
Slew rate (+) (V/μs)	197	203
Slew rate (+) (V/μs)	106	134
Average slew rate (V/μs)	151.15	168.50
Settling time (ns)	102.131	35.95
Power dissipation (μW)	105.64	103.45

Table.3. Comparison table of opamp with Self-Cascode at input stage, NMOS based and current subtractor based opamp

Parameters	Proposed 3 (Fig.12): Base circuit with self-cascode at input stage + Adaptive biasing technique and Self cascade	Proposed 6 (Fig.21): Base circuit with self-cascode at input stage + Current Subtractor
Slew rate (+) (V/μs)	205	293
Slew rate (+) (V/μs)	130	206
Average slew rate (V/μs)	165	249.5
Settling time (ns)	46.276	34.724
Power dissipation (μW)	104.909	86.27

The Table.3 shows the comparison table between Proposed 3 and Proposed 6 circuit. Proposed 6 has 51.21% greater slew rate than Proposed 3. The power dissipation has reduced by using Current subtractor as Adaptive biasing circuit compared to NMOS based Adaptive biasing circuit by 17.76%. Similarly, settling time has also improved by 24.97%.

Hence it is concluded that Proposed 4 circuit has a slew rate, 7.44% greater than Proposed 1. Similarly, proposed 5 has 9.43% greater than Proposed 2 and Proposed 6 has 51.21% greater slew rate than Proposed 3. The power dissipation has reduced by using Current Subtractor as Adaptive biasing circuit compared to NMOS based Adaptive biasing circuit. Similarly, settling time has also improved.

4. CONCLUSION

As the transistor size is reducing day-by-day the designing of an opamp is becoming more challenging because its dynamic performance is widely affected. In this work, an adaptive biasing technique is used to enhance the performance of opamp. NMOS based adaptive bias circuit and current subtractor are used to adaptive bias circuits in opamp to boost the bias current. With the increase in bias current, the slew rate is improved to a great extent.

Later in opamp, the input stages were replaced by FVF and self-cascode stages. It was found that Current subtractor as adaptive bias circuit gives a high-grade performance in terms of slew rate, Settling time and Power dissipation.

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