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ULTRA-LOW POWER VOLTAGE REFERENCE CIRCUIT UTILIZING A THRESHOLD VOLTAGE DIFFERENCE BETWEEN TWO CNFETS

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Abstract

This paper proposes a voltage reference circuit that exploits sub-threshold conduction and threshold voltage difference between two carbon nanotube field effect transistors (CNFETs) to achieve ultra-low power consumption. The circuit produces a reference voltage of 203mV at 0.5V supply voltage, consumes only 3.42pW power and exhibits excellent temperature and power supply independence. The robustness of the proposed circuit for variations in carbon nanotube (CNT) diameter and inter CNT pitch variations is also presented with Monte Carlo simulations.

Keywords:

Carbon Nanotube Field Effect Transistor, Ultra-Low Power Circuits, Voltage References

1. INTRODUCTION

Reference voltage source is a circuit that provides a dc voltage, which is highly stable and precise, irrespective of process, voltage and temperature variations. There is an increasing demand for precision voltage reference circuits which satisfy stringent requirement of ultra-low power consumption along with process, voltage and temperature tolerance [1] - [2]. Many of the modern electronic circuits and systems such as radio frequency (RF) systems, wearable, and implantable sensor systems, and portable/handheld electronic systems find voltage reference as an essential building block [3]. Precision and ultra-low power voltage references have recently become important constituents of the Internet of Things (IoT) devices consisting of battery powered sensors, actuators and networked intelligence.

For applications in portable/handheld, wearable and implantable devices, the importance of power consumption is significantly elevated. Since these applications are mostly battery powered, low power consumption is critical to extend battery life [4] - [5]. Therefore, ultra-low power consumption is of prime importance in the design of the reference voltage. In this paper, we present a voltage reference that satisfies the ultra-low power requirement of portable applications. The proposed voltage reference utilizes just two CNFETs, does not need resistors, and provides excellent temperature stability and power supply rejection. The proposed voltage reference is also investigated for its robustness against CNT diameter and inter CNT pitch variations. The most common type of voltage reference is the bandgap reference circuit. To decrease the effect of temperature and process variations, long channel designs have been preferred. Also due to short channel effects and gate leakage there are limits for achieving significant benefits due to scaling in case of analog circuits such as bandgap references [6]. Therefore in a nanometer device regime with aggressive scaling, design of precise bandgap reference has become a challenging task. Traditional bandgap references uses amplifier for error correction. Incorporation of amplifiers in voltage references results in improved temperature and supply voltage insensitivity [7] - [8]. The designs that avoid amplifiers often rely on transistors operating in saturation region, resulting in a significant power dissipation. The transistors operating in saturation region require sufficient headroom between supply and threshold voltage, limiting minimum functional V_{dd} [8] - [9]. Among the different approaches sub-threshold design is the most promising approach for ultra-low power applications. In this paper, we present a hybrid dual threshold CNFET based voltage reference, wherein transistors operate in sub-threshold region.

This paper is organized as follows, section 2 takes a review of carbon nanotube electronics and discusses important considerations for a CNFET threshold voltage. Proposed reference circuit and its HSPICE simulation results are discussed in section 3. The variability analysis of the voltage reference with respect to CNT diameter and inter CNT pitch is presented in section 4. The conclusion is given in section 5.

2. CARBON NANOTUBE ELECTRONICS

Complementary Metal Oxide Semiconductor (CMOS) technology is confronting expanding difficulties in achieving scaling along with performance gains due to the fringe capacitances, short-channel effects, and gate leakage. Silicon technology is relying on double-gate or FinFET technology to improve device performance with continued scaling [10]. At the same time, there is growing interest in emerging research devices which can provide scaling beyond that is achievable by ultimately scaled CMOS such as carbon based nano-electronics, spin-tronic devices, ferromagnetic logic, and nano-electro-mechanical (NEMS) switches [11]-[13]. Amongst them CNTs are a promising material which can replace silicon channel for carrying electric current between drain and source of a CNFET. CNTs were discovered by IJIMA of NEC Japan in 1991 [14]. Progress made in recent year's shows that the limitations of silicon MOSFETs such as the exponential increase of leakage currents in scaled devices can be overcome to some extent, and further scaling of device sizes is possible with CNFET technology. Owing to very high electron mobility, efficient transport of carriers and improved gate electrostatics carbon nanotubes serve as an excellent active channel of a transistor device. Silicon still provides the substrate, mechanical support and heat transport mechanism for the hybrid device structure of the resulting CNFET. In the sub-10nm regime of the scaled devices, CNFETs outperform potential alternatives of the conventional MOSFET. Therefore, there exists huge opportunities for the integration of CNFETs into circuits and systems for the futuristic electronic

applications. Apart from this carbon nanotubes, due to their low resistivity, high current carrying capacities and electro-migration immunity, have proved to be an excellent interconnect material [15]-[16]. Carbon nanotubes and CNFET technology have wide range of applications in fields of chemical and biological sensing, nano-electronics and optoelectronics [17]. The carbon nanotubes exist in two forms:

- Single walled carbon nanotube (SWCNT) and
- Multi-walled carbon nanotube (MWCNT).

A SWCNT consists of one cylinder only. An SWCNT can be classified as either metallic without a bandgap or a semiconductor with certain bandgap, depending on the angle of the atomic arrangement with respect to the tube axis. This is defined as the chirality vector and is denoted by the two indices (n, m). By considering indices (n, m) one can determine if a carbon nanotube is metallic or semiconducting. If p and q are two integers with p as a reminder after dividing n - m by 3 then, we can write $n - m = 3q + p$. The SWNT is semiconducting with a bandgap if $p = 1, 2$. Otherwise if $p = 0$ then SWNT is metallic with no bandgap. The diameter of the CNT expressed as a function of two indices (n, m) is given by Eq.(1),

$$D_{CNT} = \frac{a_0\sqrt{3}}{\pi}\sqrt{n^2 + nm + m^2} \tag{1}$$

where, a_0 = 0.142nm is the inter-atomic distance between each carbon atom and its neighbor [18]-[19]. The threshold voltage of the intrinsic CNT channel can be approximated to the first order as the half bandgap. The tubes with smaller diameters have a larger bandgap, and tubes with larger diameters have a smaller bandgap. There is inverse dependence of the threshold voltage on tube diameter.

$$E_g \propto \frac{0.8eV}{D_{CNT}} \tag{2}$$

$$V_{th} = \frac{E_g}{2e} = \frac{\sqrt{3}}{3}\frac{aV_\pi}{eD_{CNT}} \tag{3}$$

where, E_g is the bandgap of the CNT, a = 2.49Å is the carbon to carbon atom distance, $V\pi$ = 3.033eV is the carbon π-π bond energy in the tight bonding model, e is the unit electron charge, and D_{CNT} is the CNT diameter [20]. Threshold voltage of CNFET can be controlled by changing the chirality vector or the diameter of the CNT. As the chirality vector changes, the threshold voltage of the CNFET will also change. CNFET threshold voltages can be approximated either by solving Eq.(1) and Eq.(3) or can also be obtained by linearly extrapolating I_{DS} vs V_{GS} curves as reported in [21]. Threshold voltages for different combinations of semiconducting chiral vectors is reported in [22], for example chiral vectors (4,0), (11,0) and (14,0) gives threshold voltages 0.69V, 0.45V and 0.33V respectively.

3. DUAL THRESHOLD VOLTAGE REFERENCE CIRCUIT

The proposed circuit utilizing a combination of low V_{th} (0.12V) device and high V_{th} (0.51V) device operating in a subthreshold region is shown in Fig.1.

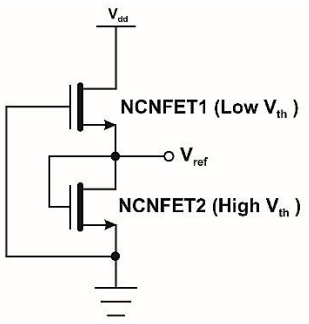

Fig.1. A dual threshold voltage reference circuit

Sub-threshold operation allows extremely low levels of supply voltages and ensures ultra-low power consumption for voltage references [8] - [9]. Voltage references employing conventional CMOS technology with transistors having different threshold voltages are reported in [8] - [9]. In this work we propose a dual diameter, dual threshold CNFET based voltage reference. A reference voltage of 203mV is achieved with 3.4145pW of power consumption. A compact spice model for CNFETs proposed in [19] has been used and the circuit is simulated with HSPICE software. CNFET device models have been developed by several research groups. Amongst them the Stanford model [19] is a compact and accurate HSPICE compatible model calibrated against experimental device data. The model covers important aspects of CNFET including parasitic capacitances, ballistic transport, band structure physics and inter channel screening. As per the model CNFET device can be instantiated in the HSPICE deck with a syntax similar for instantiating CMOS device. The Fig.2 shows HSPICE compatible device model with relevant parameters. Typical device instantiation with parameter values in the HSPICE deck for NCNFET can be,

XCNT1 Drain Gate Source Substrate NCNFET L_{ch} = 32e^{-9} L_{ss} = 32e^{-9} L_{dd} = 32e^{-9} K_{gate} = 16 T_{ox} = 4e^{-9} C_{sub} = 40e^{-12} *Pitch* = 20e^{-9} n_1 = 19 n_2 = 0 *tubes* = 3, where L_{ch} = channel length, L_{ss} = length of source side extension region, L_{dd} = length of drain side extension region, K_{gate} = dielectric constant, T_{ox} = oxide thickness, C_{sub} = coupling capacitance, *Pitch* = inter CNT pitch, n_1, n_2 = chiral vectors, *tubes* = number of CNTs.

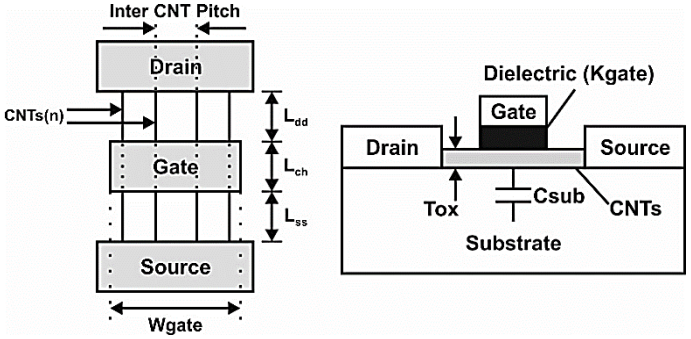

Fig.2. CNFET model with parameters

The upper transistor NCNFET1 as shown in Fig.1 with its gate tied to the ground consists of 3 nanotubes with chiral indices (24, 13). This results in a low V_{th} of 0.12V. Relatively higher V_{th} of 0.51V is used for the lower transistor NCNFET2 with chiral indices (9,1). Both the CNFETs operate in subthreshold region drawing extremely low drain to source current. The simple

expression of drain to source current I_{DS} of CNFET is given by Eq.(4).

$$I_{DS} = ng_{CNT}(V_{DD} - V_{SS} - V_{th}) \quad (4)$$

where, g_{CNT} is the transconductance of the CNFET, n is number of CNTs in a CNFET, V_{SS} is the voltage drop between inner and external source node of the transistor and V_{th} is the device threshold voltage.

To achieve a voltage reference that is insensitive to process variations such as threshold voltage an optimum value of V_{th} difference is to be maintained between the upper and lower transistor. To determine the minimum required V_{th} difference, the proposed circuit is simulated using HSPICE under different combinations of chiral vectors. As per Eq.(1) and Eq.(3) different chiral vectors gives different CNT diameters, which further results in different threshold voltages for the two transistors. For example an upper transistor with n = 24, m = 13 results in a V_{th} of 0.12V and n = 9, m = 1 results in V_{th} of 0.51V giving a net V_{th} difference of 0.39V. The Fig.3 shows reference voltage and reference current as a function of V_{th} difference between the upper and lower transistor. Similarly, Fig.4 shows reference voltage and average power dissipation as a function of V_{th} difference.

As per the simulation results shown in Fig.3 and Fig.4, for V_{th} difference greater than 0.39V V_{ref} becomes insensitive to the variations in threshold voltages. Any change in the threshold voltage of either of the two transistors will result in variation in reference voltage if the V_{th} difference falls below 0.39V, otherwise reference voltage will be maintained constant. The upper transistor operates in sub threshold region while the lower transistor determines the reference current. Higher the threshold voltage of the lower transistor as compared to the upper transistor, lower is the reference current drawn resulting in an ultra-low power consumption. CNFETs offer several benefits over conventional MOSFETs in subthreshold region and provide superior performance in subthreshold region. The drain to source current I_{DS} of CNFET in subthreshold region (weak inversion) is significantly greater than that of conventional MOSFET. CNFETs almost does not exhibit the non-ideal effects such as drain-induced barrier lowering (DIBL) and gate-induced drain leakage (GIDL). Sub-threshold conduction in the CNFETs is mainly because of the band-to-band tunneling mechanism through the semiconducting sub bands [19] - [20]. The resulting current is referred to as BTBT current I_{btbt}. The drain to source current due to band to band tunneling depends on threshold voltage V_{th} and also on the number of CNTs in the transistor.

The Fig.5 shows reference voltage generated at the node V_{ref} formed between drain-source of the two CNFETs. The gate of the upper transistor is permanently tied to ground while the reference voltage is applied to the gate of the lower transistor resulting in a cascode configuration which further makes the reference voltage immune to variations in supply voltage. The HSPICE simulations are carried out to test temperature dependence of the reference by varying temperature between -25˚C to 125˚C (V_{dd} sweep between 0 to 2V). Simulation result shows that the reference has got excellent temperature independence exhibiting near zero temperature coefficient. This is because unlike MOSFETS, in CNFET devices, the effect of temperature on threshold voltage is negligibly small [22]. Simulation results reported in [22] shows a negligible V_{th} variation for the temperature range of -25˚C to 125˚C. For the proposed voltage reference mean reference voltage is about 203mV for a range of V_{dd} between 0.3V to 2V. The minimum V_{dd} required for the circuit to provide a stable reference voltage is 0.3V.

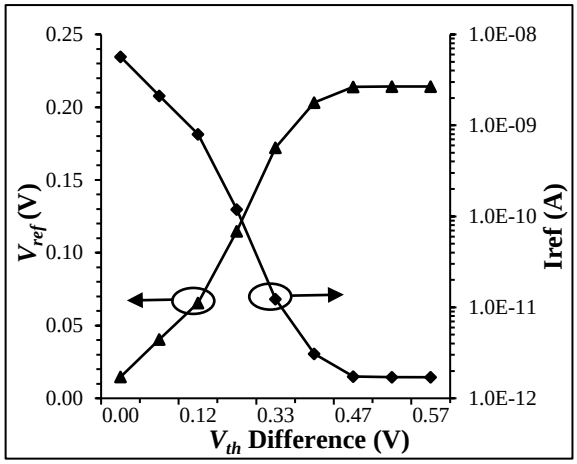

Fig.3. Reference voltage and current as a function of V_{th} difference

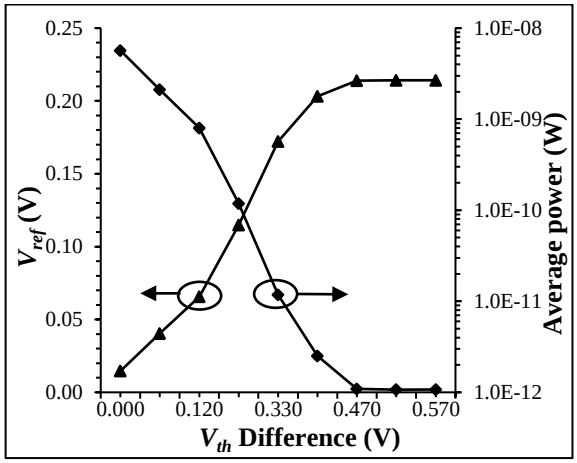

Fig.4. Reference voltage and average power consumption as a function of V_{th} difference

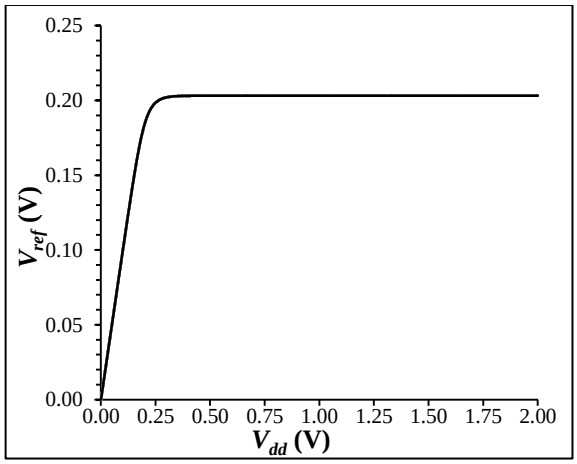

Fig.5. Reference Voltage vs V_{dd} (Temperature sweep -25˚C to 125˚C)

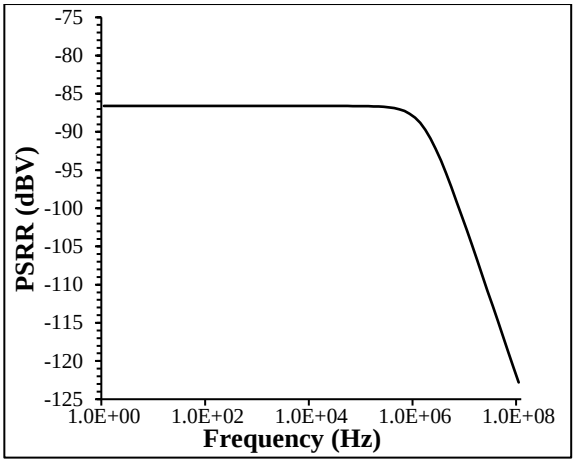

Fig.6. PSRR at 25^{0}C, V_{dd} = 0.5 V

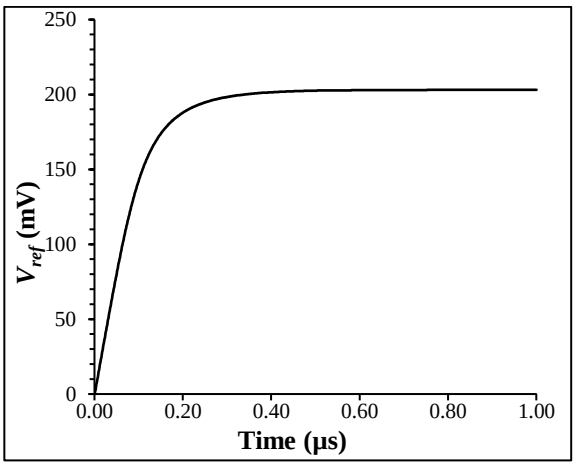

Fig.7. Transient analysis

Many of the on-chip high speed digital circuits generate noise and hence demand a good power supply rejection ratio (PSRR) over a wide frequency range from the on chip voltage reference. A good PSRR for a voltage reference indicates its ability to reject ripple or noise in the power supply. The PSSR over the range of frequency for the voltage reference is shown in Fig.6. The circuit exhibits a PSRR of -86dB at 10KHz frequency, 25^o C temperature and for V_{dd} of 0.5V. Similarly PSRR is of -102dB at 10MHz frequency. The Fig.7 show transient analysis of the proposed circuit. The output voltage settles to 203mV within 0.5µs.

4. VARIABILITY ANALYSIS OF THE VOLTAGE REFERENCE

Just like conventional CMOS, CNFETs are also prone to manufacturing variability and hence one cannot ensure manufacturing of exactly identical CNFETs. This results in device mismatch consisting of random variations in device characteristics which in turn causes behavioral variation from circuit to circuit. Monte Carlo analysis is often used to investigate the effect of such type of variability on the overall circuit performance. In this section, we present effects of diameter and inter CNT pitch variations on the proposed voltage reference using Monte Carlo simulations. Monte Carlo analysis is a statistical analysis that is used to predict overall circuit behavior under random variations of the device parameters within specified tolerance. Based on the possible variations in the parameters either a uniform or Gaussian distribution of the inputs are generated to obtain deterministic Monte Carlo simulation output. The CNT growth process involves difficulties such as controlling the diameter of the SWCNT and the percentage of metallic CNTs produced. Different CNT growth techniques such as laser ablation, chemical vapor deposition (CVD), arc discharge and high pressure CO decomposition (HPCO) are used for the manufacturing of CNTs. However, these techniques produce a mixture of CNTs with various chirality. Variations in chirality results in diameter variations that affect the drive current and the threshold voltage of the CNFETs [23]. Depending on the manufacturing process of CNTs, various mean diameters and diameter distributions are observed. Experimental results so far indicate a Gaussian distribution for the diameter of CNTs grown using different growth techniques. These growth techniques have shown that the variability can be reduced to the extent of standard deviation of the CNT diameter being controlled below 10% of the mean CNT diameter [24]-[25]. The Monte Carlo simulation (Fig.8) were performed with diameter variation achieved via variations in chirality of both the CNFETs. For the upper CNFET, a Gaussian distribution with nominal chirality of (24,13) and a 3σ variation of 0.5 is considered. For lower CNFET, a Gaussian distribution with nominal chirality of (9,1) with 3σ variation of 0.2 is considered. The results of the Monte Carlo analysis gave μ = 0.2031, σ = 0.0032 and σ/μ = 1.5807%.

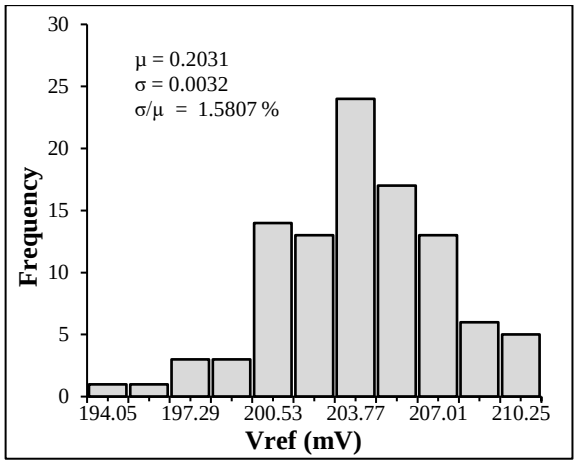

Fig.8. Effect of diameter variability on reference voltage

Another challenge in the CNT growth process is the density variation resulting in non-uniform distribution of the grown CNTs in the CNFET channel. The existing fabrication processes do not ensure uniform spacing between adjacently placed parallel tubes. It is also difficult to provide precise control of the locations of individual CNTs and maintaining consistency in the CNT count. Variations in diameter of the individual CNTs and non-uniform spacing between the tubes contribute to produce inter CNT pitch variations. Due to these variability, different CNFET devices then exhibit variations in charge screening effect [22]. This variability in charge screening effect results in large variations in CNFET drive current. To investigate the effect of inter CNT pitch variations, Monte Carlo simulations of the proposed voltage reference circuit were performed with 10nm nominal inter CNT pitch and a 3σ variation of 2.5nm. The Monte Carlo analysis

results as depicted in Fig.9, gave μ = 0.2028, σ = 0.0001 and σ/μ = 0.0467%, which signifies robust performance of the proposed voltage reference under CNT pitch variations.

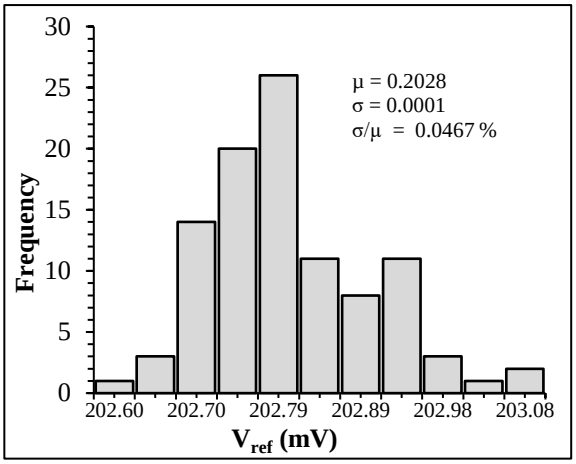

Fig.9. Effect of inter CNT pitch variability on reference voltage

5. CONCLUSION

An ultra-low power voltage reference circuit with just two CNFETs having different threshold voltages was presented. Dependence of reference voltage on the difference between threshold voltages of the CNFET pair arranged in the circuit was investigated. Reference voltage, achieved by the proposed circuit was found to be immune to the V_{th} variations, if the V_{th} difference between the CNFET pair was more than 0.39V. Furthermore, the circuit was studied for its temperature dependence, power supply sensitivity and stability analysis. The circuit exhibited excellent temperature independence, a PSRR of -86dB at 10KHz, 0.5µs settling time and achieved 203mV reference voltage while consuming only 3.4245pW. Monte Carlo simulations for CNT diameter variation, and inter CNT pitch variations gave σ/µ values 1.5807% and 0.0467% respectively, signifying a robust performance of the circuit.

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