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# PERFORMANCE ANALYSIS OF ADIABATIC TECHNIQUES USING FULL ADDER FOR EFFICIENT POWER DISSIPATION

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***Abstract***

***Adiabatic circuits are low power circuits, which deals with reversible logic that it stores the power and gives it back again. Currently Several Adiabatic techniques have been adopted for efficient power dissipation. The technique used to minimize power dissipation are Efficient Charge Recovery Logic, Positive Feedback Adiabatic Logic, and Pass Transistor Logic. The Adiabatic technique is mainly used for reducing the power dissipation in VLSI circuits which performs charging and discharging process. The full adder plays an important role in many arithmetic operations such as the adder, multiplier and divider and processors. In order to limit the power dissipation, an efficient full adder is designed for the different adiabatic techniques and all the circuits have been simulated by 125nm technology using tanner EDA tool.***

***Keywords:***

***Adiabatic logic, low power dissipation, Efficient Charge Recovery Logic, Positive Feedback Adiabatic Logic, Pass Transistor Logic, low power adder***

## 1. INTRODUCTION

Recently, power dissipation is the main issue for designing the VLSI circuits. Most of the electronic devices are based on the low power circuit design. To overcome this problem, the energy recovery principle introduced and it is known as adiabatic logic. This circuit are which the energy is recycled back to threshold voltage and no energy is wasted [1] and it also gives the rising cost of energy, less power consumption and increase in sensitivity. The main objective of low power circuit is that it increase the battery life, reduces the size, weight and the cost of the devices and also reduces the complexity in high speed devices. In digital circuits the power dissipation can be reduced by using several adiabatic logics. Adiabatic circuits use 'Reversible logic' to conserve energy. It works with the concept of switching activities which reduces the power, by giving the stored energy back to the supply, so that the power dissipation is reduced [2]. Adiabatic logic achieves low power and faster operation. The general rules are adopted by the Adiabatic techniques are (1) Never switch ON a transistor when voltage is supplied from source to drain and (2) Never switch OFF a transistor when current flows through the circuit.

Adders are the basic building blocks of any circuit in which it is designed to perform high speed arithmetic operation. And they are the most significant logic modules used in the strategy of digital VLSI circuits. It performs the basis for all calculations such as multiplying, counting and sifting etc. In amount to carrying out the responsibilities of addition, the adder precedes the source for many difficult circuits like the multipliers, subtractors, RAMs, report calculations and much more.

In this paper, a full adder is designed by using adiabatic logic and it is compared with the existing adiabatic techniques like ECRL, PTL and PFAL design.

## 2. ADIABATIC LOGIC

The term "adiabatic" refers to the thermodynamic process that do not exchange energy with the external environment, and therefore there is no amount of power or energy is dissipated. In this technique during switching process this logic reduces the dissipation of power or energy and whereas it reuses the energy by recycling it from the load capacitance, so that the same energy can be used for next operation. The Fig.1 shows that the process in which changeover occurs without energy being either lost or gained from the system rather than heat or electronic charge is preserved. Thus an ideal adiabatic logic would operate without increase or decrease of electronic charge.

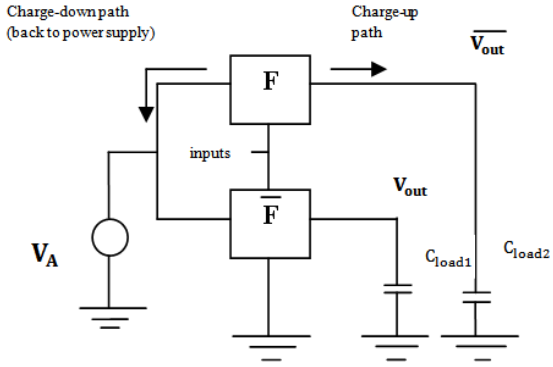


Fig.1. Adiabatic logic

This logic provides a way to reuse the energy stored in load capacitors than comparing the conventional way of discharging the load capacitors to the ground rather than wasting the energy [3]. But the charge which is grounded can be recycled back and gives to power clock.

## 3. ADIABATIC TECHNIQUES

In low power VLSI circuits are designed by using several adiabatic techniques such as efficient charge recovery logic, positive feedback adiabatic logic and pass transistor logic.

### 3.1 EFFICIENT CHARGE RECOVERY LOGIC (ECRL)

ECRL provides a new method which performs precharge and evaluation at the same time where it eliminates the precharge diode and dissipates the less energy when compared to the other

adiabatic circuits [4]. It consists of a cross-coupled PMOS transistors and two NMOS transistors in N-functional block which is constructed by using two cross-coupled transistors M1 and M2 as shown in the Fig.2. Due to the operation of cross-couple PMOS transistors a Full Swing Output is obtained in both pre charge and recovery phases.

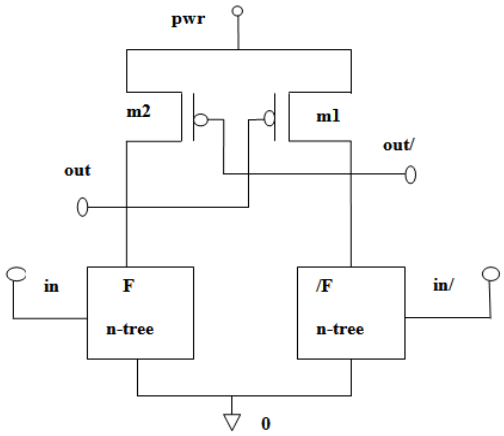


Fig.2. ECRL

It works with a four phase power clock based on the Evaluation, Hold, Recover and Wait operation. This clock works efficiently to recover the charge delivered by the supply clock. Each stage of the clock is followed by the next stage of the clock with a 90° phase lag. So that when the previous stage is in the hold phase, the next stage must be evaluated by the logic values in the precharge and evaluation process [5].

### 3.2 POSITIVE FEEDBACK ADIABATIC LOGIC (PFAL)

The PFAL is a partial energy recovery circuit with dual rail network. To avoid a logic level degradation on the output nodes PFAL gate with a latch made up of two PMOS transistor M1, M2 and two NMOS transistor M3, M4 are used. Both transistor generates a two complemented outputs. A four phase power clock is also known as time varying source which is used for adiabatic charging purpose [6]. When the input is high the value of power clock increases which attains the transistors M5 and M1 to be in ON state. Due to this process the out is connected to the ground and/out will be based on the changes of power clock. When the power clock reaches, out will become zero and or out will be turned to $V_{dd}$ which will be act as an input for the next stage of the operation. Let us consider the power clock varies from $V_{dd}$ to 0 then the energy will be recovered through the transistor M1.

The functional blocks of Fig.3 are connected in parallel with the PMOSFET of adiabatic amplifier and thus it is created with a transmission gate process. The two F trees are realized by using the logic functions of PFAL and it is also used to generate the positive and negative output swings [7].

### 3.3 PASS TRANSISTOR LOGIC (PTL)

Pass transistor logic is one of the types of well-known nMOS logic style. In Integrated circuits design it uses several logic families. It reduces the transistor count by eliminating the redundant transistors which is used to make different logic gates.

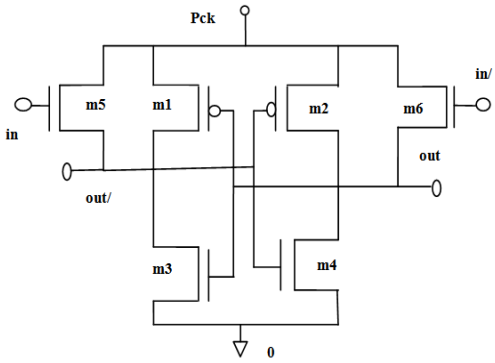


Fig.3. PFAL

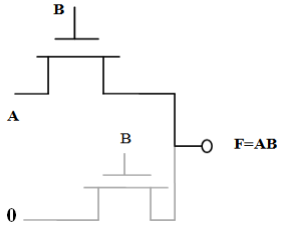


Fig.4. PTL Circuit

When compared to complementary CMOS logic PTL uses minimum transistors, high speed, and requires low power. In other logic families input is applied to the gate terminal of transistor but in PTL it is also applied to the source or drain terminal of the transistor as shown in the Fig.4. When using this as a pass transistor, the device may conduct current in either direction of the device.

## 4. CIRCUIT IMPLEMENTATION OF ADIABATIC TECHNIQUES USING FULL ADDER

This section deals with the circuit implementation of full adder for different adiabatic logic techniques and the performance has been analysed using different parameters.

### 4.1 ECRL BASED FULL ADDER

In ECRL technique, a power clock signal is differentiated into four phases: wait, evaluate, hold, and recover. During wait phase, an input signal is prepared by the previous logic gates. During evaluate phase, an input signals are kept stable and the gate outputs are calculated based on the stable signals. During hold phase, a supply voltage is kept constant to VDD and the input signal is decreased. During recover phase, a clocked VDD becomes lower and the energy from the output nodes is recycled during the discharging process. Hence, Fig.5 shows the outputs from the previous stage are used as an input for the current stage and they are synchronized using the phases of clock cycle [8].

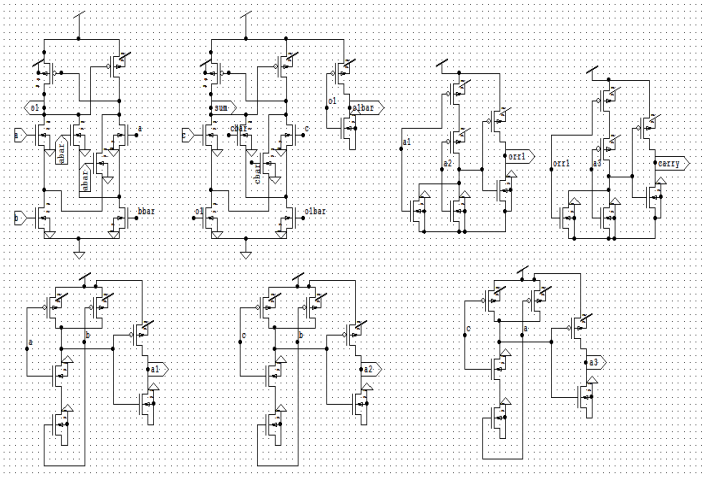

Fig.5. ECRL based Full Adder Circuit

## 4.2 PFAL BASED FULL ADDER

PFAL is same as the 2N-2P logic. The sum and carry equations are implemented on the bases of two N-MOS and two P-MOS transistors and it produces two outputs separately. The Fig.6 consist of 24 transistors in sum circuit and Fig.7 consist of 16 transistors in carry circuit. The Sum, Sum bar, Carry and Carry bar are the four outputs of this circuit [9].

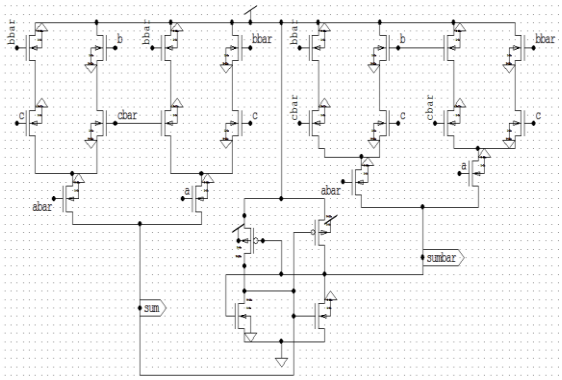


Fig.6. PFAL based Full Adder sum Circuit

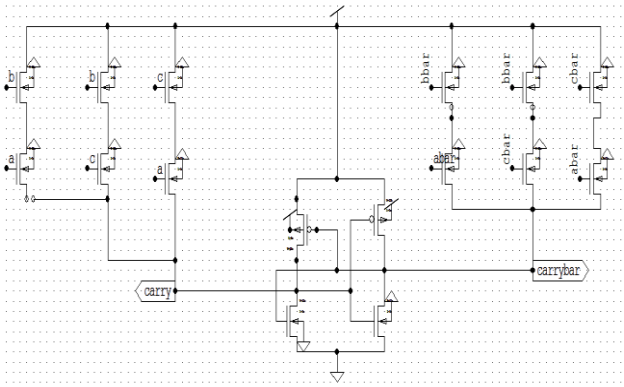


Fig.7. PFAL based Full Adder carry Circuit

PFAL logic which minimize the coupling effects and in construction, its logic is made up of two NMOSFETS and two PMOSFETS. A Four phase power clock is used in PFAL, which performs the evaluate operation, hold operation, wait operation and recover operation [10].

## 4.3 PTL BASED FULL ADDER

The PTL is driven by a periodic clock signal and acts as an access switch to either charge up or charge down the parasitic capacitance, depending upon the input signal. The Fig.8 consists of nine nMOS transistors the inputs are a, b, c and the outputs are considered as sum and carry. The possible operations are logic "1" and logic "0" when the clock signal is active the logic "1" operation performs charging up the capacitance to a logic-high level and when the logic "0" operation performs charging down the capacitance to a logic-low level. In other case, the output of the NMOS inverter assumes a logic low or a logic-high level, depending upon the voltage [11].

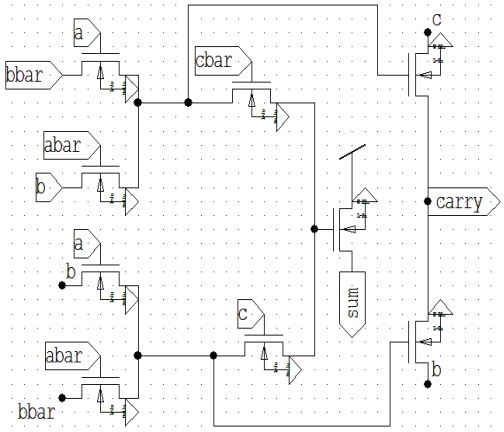


Fig.8. PTL based Full Adder Circuit

## 5. RESULTS AND DISCUSSION

The simulation results of full adder in different adiabatic logic circuits have been simulated and discussed in this section. These Simulations are carried out using Tanner 7 at 125nm technology. The average power consumption of the full adder is analyzed for every logic style and the comparison is mentioned in Table.1.

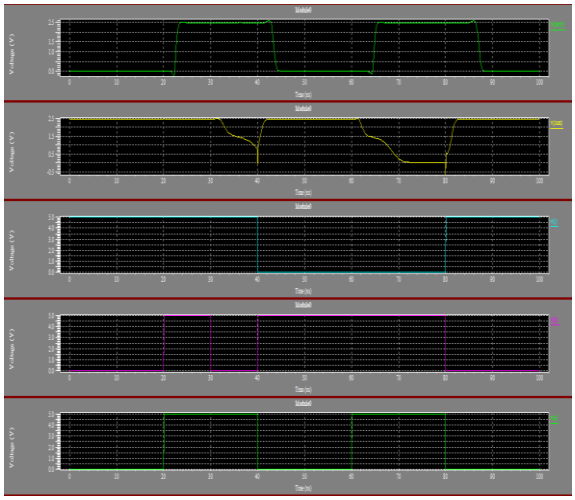

Fig.9. Output waveform of ECRL Full adder

The Fig.9 shows the simulated result for ECRL full adder. The input values are based on the truth table of full adder for example

the value assigned for 1st bit ECRL based full adder is when A = 0, B = 0, C = 1 where the obtained output is Sum = 1, Carry = 0. Based on this operation the obtained average power is 14.35µw.

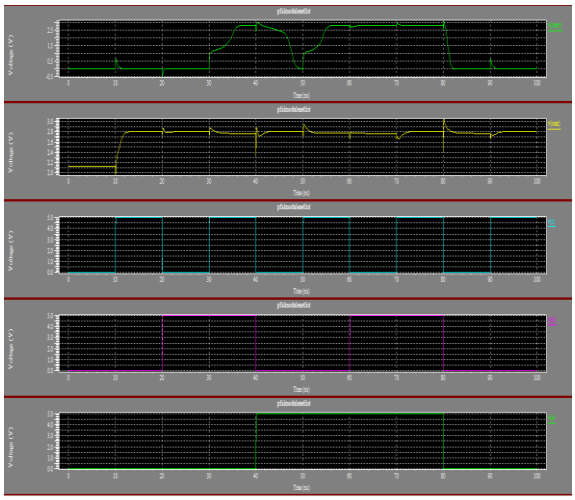

Fig.10. Output waveform of PFAL Full adder

The Fig.10 shows the simulated result for PFAL full adder. The input values are based on the truth table of full adder for example the value assigned for 1st bit PFAL based full adder is when A = 0, B = 0, C = 0 where the obtained output is Sum = 0, Carry = 0. Based on this operation the obtained average power is 16.13µw.

The Fig.11 shows the simulated result for PTL full adder. The input values are based on the truth table of full adder for example the value assigned for 1st bit PTL based full adder is when A = 0, B = 0, C = 1 where the obtained output is Sum = 1, Carry = 0. Based on this operation the obtained average power is 13.17µw.

The PTL logic gives the better performance in terms of average power dissipation compare with previous two techniques. Further, by using this technique transistor count also be minimized.

The Table.1 compares the analysis of various parameters such as power supply, average power and transistor count and technology are calculated by this table.

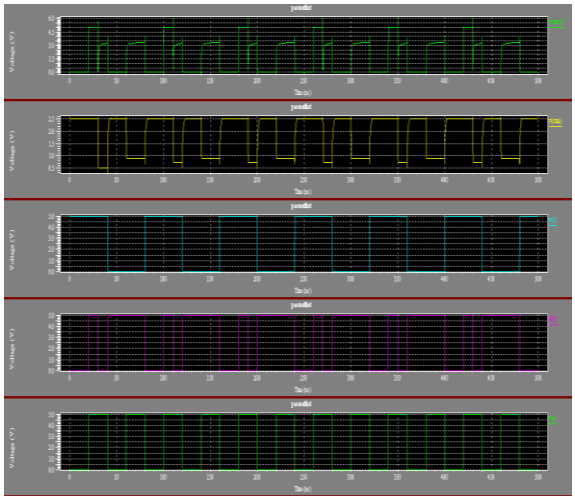

Fig.11. Output waveform of PTL Full adder

Table.1. Simulation parameters for different adiabatic full adder techniques

| Parameters | ECRL Full Adder | PFAL Full Adder | PTL Full Adder |
|---|---|---|---|
| Technology | 125nm | 125nm | 125nm |
| Power supply | 2.5v | 3.0v | 2.5v |
| Average power | 14.35µw | 16.13µw | 13.71µw |
| Transistor count | 48 | 40 | 09 |

The Table.1 shows that, the simulation parameters are considered for various adiabatic techniques. 125nm technology has been adopted for all three techniques.

## 6. CONCLUSION

In this study, we compare three full adders, namely, ECRL Full Adder, PFAL Full Adder and PTL Full Adder to study its power consumption during the operation of circuit. When comparing the three adiabatic techniques PTL consumes low power and less transistor count. But ECRL and PFAL performs high power and increased transistor count than PTL. Thus the result shows that the proposed adiabatic logic has less power dissipation of 13.71µw and efficient energy recovery process. In future, the PTL Full Adder is applied to microprocessors for reducing power dissipation.

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