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LOW POWER AND HIGH PERFORMANCE SHIFT REGISTERS USING PULSED LATCH TECHNIQUE

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Abstract

This work presents an elegant methodology using pulsed latch instead of flip-flop without altering the existing design style. Pulsed-latch technique retain the advantages of both latches and flip-flops and thus one can achieve both high speed and lower power consumption simultaneously. In this work, pulsed latch technique has been used to reduce the delay of various shift registers without increasing any power consumption. In very high speed VLSI circuits due to heavy pipelining there is requirement of low power edge triggered flip-flops. However, for low power consumption in these very high speed VLSI circuits, the migration from flip-flop to pulsed latch technique has become a great success. In the proposed work, non-overlapped delayed pulse clock has been used in pulse latch technique to eliminate the timing problem between the pulsed latches. All the proposed shift registers have been designed in 90 nm CMOS technology and their functionality have been verified using Cadence Virtuoso. From this work, it has been concluded that, the pulse latch technique reduces the power consumption significantly in the designed registers and overall there is an improvement in power delay product. Further, it is pertinent to mention that the proposed registers require less number of transistors for their implementation as compared to conventional versions.

Keywords:

Low Power, Non-Overlapped Pulse, Pulsed Latch Technique, Flip-Flop, Delay, Shift Register

1. INTRODUCTION

Recently, many methodologies have been introduced for reducing dynamic power for systems-on-chip (SoCs). These methodologies, however, impose restrictive physical constraints which have schedule impact or which are heavily dependent on logic functions such as clock gating. Dynamic power is consumed across all elements of a chip. The clock network is one of the large consumers of dynamic power. Therefore, reducing power in the clock network can impact the overall dynamic power significantly. Designers already use a variety of techniques to reduce the clock power using smaller clock buffers, reducing the overall wiring capacitance, employing clock gating to reduce the dynamic power, and de-cloning to move the clock buffers at higher levels of hierarchy.

Even with these techniques, the dynamic power of clock network can be large since registers are used as state elements in the design. In general, a flip-flop is used as the register or you can say sequential circuits [1]. For mobile devices, where power consumption is the prime concern with high speed of operation, there is requirement of low power flip-flops in designs. Many other applications where shift registers are commonly utilized such as digital filters [2], communication receivers [3] and image processing IC's [4]. In particular, edge-triggered sequential circuits, which consist of combinational blocks that lie between D flip-flops, are the most common form of sequential circuits in ASIC designs due to their convenience of timing verification.

A flip-flop is sequential edge triggered circuit which is integral part in most applications [5]. Flip-flops, however, impose significant overhead in terms of delay (setup time and clock-to-Q delay), clock load, and area than latches do. This is unavoidable since flip-flops are typically constructed by connecting two level sensitive latches in a master-slave fashion. Latches are therefore superior to flip-flops in terms of overhead of sequencing elements. Level-sensitive sequential circuits based on latches, nevertheless, make timing verification very difficult, since combinational blocks are not isolated each other due to transparent nature of latches. On the other hand, this transparency offers more flexibility in design, which is why they are widely used in high-performance microprocessors [5]. Flip-flop synchronization with the clock edge is widely used because it is matched with static timing analysis (STA). Timing optimization based on STA is must for SoCs. On the other hand, designers may choose to use a latch for storing the state. A latch is simple and consumes much less power than that of the flip-flop. However, it is difficult to apply static timing analysis with latch design because of the data transparent behavior.

Using flip-flop leads to large power dissipation, counting upto 50 percent of overall power of circuit. Hence, there is requirement of replacing the flip-flop with more efficient circuit which has same functionality while achieving low power, area and robustness to PVT variations [6]. Pulsed latch technique is one of the most feasible solution to this problem. This technique uses latches triggered with pulse clock waveforms. The most attractive feature of pulsed latch technique is that designers can apply static timing analysis and timing optimization to a latch design while reducing the dynamic power of the clock networks.

Rest of the paper is organized as follows: Section 2 presents the principle of pulsed latch technique. In section 3, the pulsed latch applications namely shift register, universal shift register and a ring counter have been implemented. Simulation results are given in section 4 and conclusions are summarized in section 5.

2. PULSED LATCH TECHNIQUE

Flip-flop is the most common form of sequencing elements. Flip-flop synchronization with the clock edge is widely used because it is matched with static timing analysis, however, high sequencing leads to overhead in terms of delay, power and area. A latch is quite simple and at the same time consumes much less power than that of the flip-flop. However, it is little difficult to apply static timing analysis with latch design because of the data transparent behavior. A latch is capable of capturing data during the time duration determined by the width of clock waveform. This time duration is known to be very sensitive to its operation.

It is possible to trigger a latch using pulse clock waveform. A latch synchronized by a pulse clock is known as pulsed latch and its behavior is similar to an edge-triggered flip-flop because the rising and falling edges of the pulse clock are almost identical in terms of timing. In a pulsed latch technique, the setup times of pulsed latch are expressed with respect to the rising edge of the pulse clock and hold times are expressed with respect to the falling edge of the pulse clock. Thus timing models of pulsed latch is very similar to that of the edge-triggered flip-flop.

The Fig.1. shows a NAND based D latch. A D flip-flop is implemented using two D latch, shown in Fig.2. Pulsed latch technique broadly comprises of a pulse generator and a latch [7]. A pulsed latch having same functionality as D flip-flop is shown in Fig.3. Thus a Pulsed latch circuit consists of one D latch and a basic pulse generator to give similar functionality as D flip-flop. The most attractive feature of using pulse latch technique is that regardless of master slave configuration of latch in flip-flop, pulsed latch eliminates one latch from each cycle and clock's complement. Another important advantage of using pulse latch technique is that the performance of existing designed can be improved without altering the existing design style.

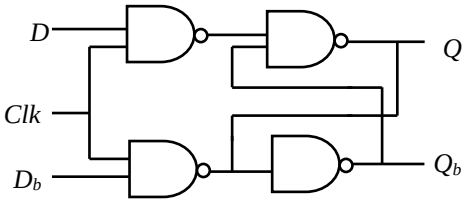

Fig.1. NAND based D latch

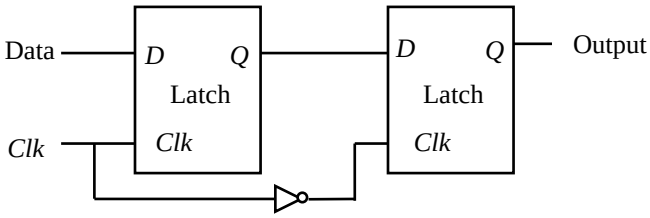

Fig.2. D Flip-flop

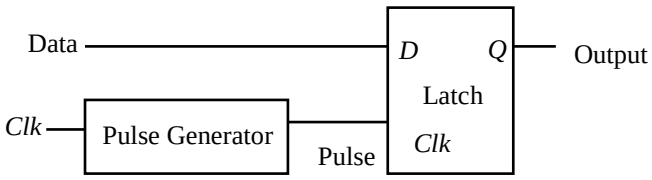

Fig.3. Pulsed latch technique

The timing models of a pulsed latch is similar to that of edge-triggered flip-flop. The Fig.3 depicts the pulse generator consisting of AND gate and NOT gate. It generates pulse clock for source clock input. Pulse width of generated pulse clock is adjusted with the help of NOT gate or by inserting delay block in series with the NOT gate. This generated pulse clock is provided to latch. The pulse generator, whose output pulse clock is provided to latch, leads to the functionality same as that of a flip-flop.

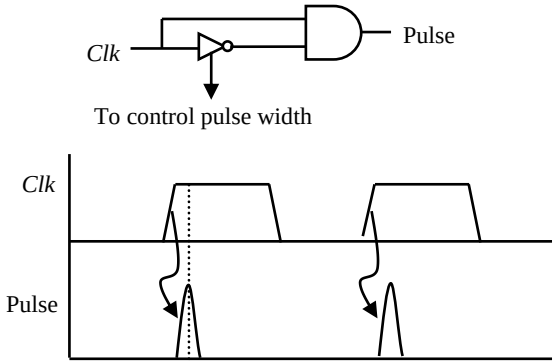

Fig.3. Pulse Generator and its waveform

In pulsed latch, the setup time is expressed in terms of rising edge of pulse clock, while hold time is expressed in terms of falling edge of pulse clock. This means timing model of pulsed latch is similar to that of flip-flop. Regardless of master slave configuration of latch in flip-flop, pulsed latch eliminates one latch from each cycle and clock's complement. The sequencing overhead is about twice that of latches for flip-flop. Time borrowing capacity as well as use of non-overlapping clocking in flip-flop, complicates its timing analysis. In addition, flip-flop holds data for long period of time, increasing the chances of hold time violations. While in case of pulsed latches, the amount of time borrowing capability is better and very less pulse width offer design to simplify its timing model. Even the sequencing overhead of the pulsed latches is lower than compared to flip-flop. Hence pulsed latch can be approximated as a faster and smaller flip-flop which have advantages of both flip-flop and latches [5].

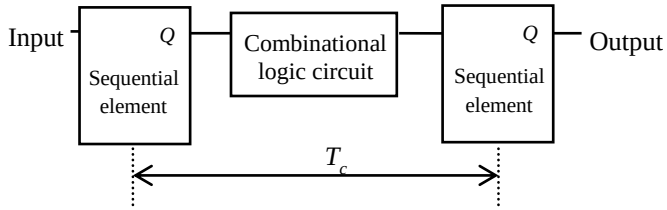

Fig.4. Sequencing circuit

In Fig.4 shows sequencing circuit where combinational logic circuit is between sequencing element which can be flip-flop or pulsed latch. In first case, taking flip-flop as sequencing element, then combinational logic propagation delay represented as t_{pd} can be expressed as,

$$t_{pd} \le T_c - \left(t_{pcq} + t_{setup}\right) \quad (1)$$

where, T_c is clock period, t_{pcq} is sequential element clock to output Q propagation delay and t_{setup} is sequential element setup time. $t_{pcq} + t_{setup}$ is figure of merit or sequencing overhead of flip-flop. t_{pd} is circuit dependent. For flip-flop data needs to arrive before the clock edge hence t_{setup} is positive therefore sequencing overhead is much higher. In second case, taking pulsed latch as sequencing element and t_{pd} can be expressed as

$$t_{pd} \le T_c - \max\left(t_{pdq}, t_{pcq} + t_{setup} - t_{pw}\right) \quad (2)$$

where, t_{pdq} is latch D to output Q propagation delay and t_{pw} is pulse width of clock given to latch of pulsed latch. In this case for pulsed latch, there are two possibilities of transition. First when pulse should be wide enough such that only one latch is critical in one

time period so it facilitates the transition or second where pulse should be narrower than setup time such that data must setup before the pulses rises. Therefore for pulsed latch the sequencing overhead is maximum of any one of possibilities overhead. In this case, the data can arrive even after the clock edge hence setup time may be negative. From above discussions and Eq.(2), it is clear that sequencing overhead for pulsed latch is lower than that of flip-flop.

3. PROPOSED SHIFT REGISTERS

Pulsed latch technique can be used in various low power design applications where flip-flop could be replaced either in pipelining or as sequencing element or as register. In this section Serial in serial out shift register (SISO), Serial in parallel out shift register (SIPO), Parallel in serial out shift register (PISO), Parallel in parallel out shift register (PIPO) and universal shift register is implemented using pulsed latch technique.

For heavy pipelining back to back connection of register or flip-flop is required. If flip-flop is replaced with pulsed latch, then pulse generator circuit can be shared for all pulsed latches. This will lead to saving of total area and power consumption with respect to flip-flop. Shift register using pulsed latch consists of several latches one after the other with pulse clock input to each latch. However, This cannot be implemented because of the timing problem. The input given to first latch doesn't change during clock pulse width thus providing correct output but the second latch provides instead output because input to this latch changes the during the clock pulse width. In this work it has been proposed to use multiple non-overlaps delayed pulsed clock signals as a solution to this problem in pulsed latch technique [7]-[9].

The delayed pulsed clock generator and its output is shown in Fig.5. In delayed pulse clock generator, the delay block is added to generate the delayed pulse of proper pulse width. The series of (N+1) delayed pulses are generated using this circuit. The frequency of clock *Clk* input to delayed pulse clock generator should be twice the total sum of required number of pulse width i.e. sum of pulse width of (N+1)generated delayed pulse clock.

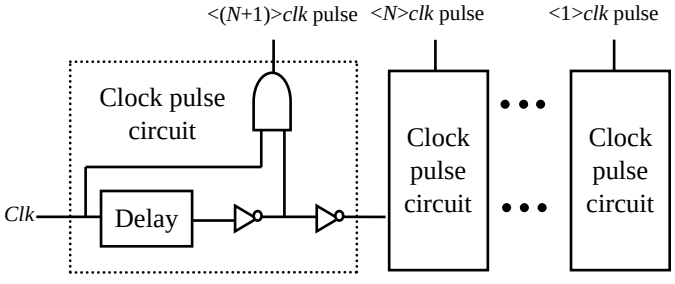

Fig.5. Delayed pulsed clock generator

In the following section, delayed pulse generator has been used for implementing five registers namely Serial In Serial Out, Serial In Parallel Out, Parallel In Serial Out, Parallel In Parallel Out and universal shift register is implemented. Data can be moved either left or right with clock pulse in Serial in serial out shift register and output can be taken from rightmost sequential element or leftmost sequential element respectively. Utilizing the delayed pulse clock generator for implementing shift register can be done by dividing shift register into '*M*' number of sub shift registers where each sub shift register has (N+1) number of latches which require (N+1) number of delayed clock pulse respectively for each latch. With this technique implementation of (M×N) bits of SISO, SIPO, PISO, PIPO and universal shift register can be done. For example in case for implementing 16-bit shift register or (4×4) bit shift register, four number of sub shift registers are required with five number of latches performs the shift operation using five number of non-overlapped delayed pulse clock. In the sub shift register, four latches are used to store 4-bit data and one latch is used as temporary latch which store the last bit data of 4-bit register. The output of temporary latch is provided to first latch of next sub shift register. In delayed pulse clock generator, it can be noticed that sequence of generated delayed pulse is reversed while providing to the latches. Hence sequence of updating of data in latch is in order from last latch to first latch. The working of all sub shift register is same just that the first latch of sub shift register is provided input by previous temporary latch output and the input is given to first latch of first sub shift register. The sequence of (N+1) delayed pulse clock is provided to each sub shift register, therefore number of pulse clock is reduced or else separate pulse clock have to provided have to be provided to each latch. Instead the number of latches is increased, but the overall power dissipation and area is reduced using this technique. The total number of latches for (M×N) shift register is (M×N)+N. Shift registers are used as pulse extenders, ALU's etc.

3.1 PROPOSED SISO SHIFT REGISTER

The Fig.6 shows the implementation of 4-bit SISO using pulsed latch. Method of using delayed pulse clock generator discussed in previous section is utilized in this application to avoid the timing problem.

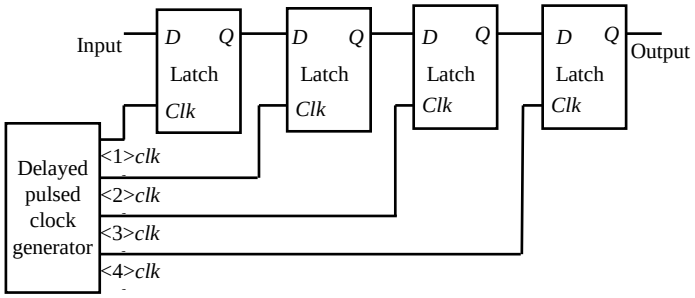

Fig.6. Proposed SISO Shift Register

The input is to be applied to the first latch of the register and sequentially the data is transferred from first latch to second latch and so on. The output is obtained from last latch sequentially according to input provided at first latch. The output would be obtained after four pulse clock for given input.

3.2 PROPOSED SIPO SHIFT REGISTER

The Fig.7 shows implementation of SIPO using pulsed latch technique employing delayed pulse clock generator. The input bit is provided to the first latch in same manner as SISO but output bits are taken from each latch as soon as the data is stored in respective latch. This application is usually attached to the output of microprocessor when more general purpose input or output pins are required than the available ones.

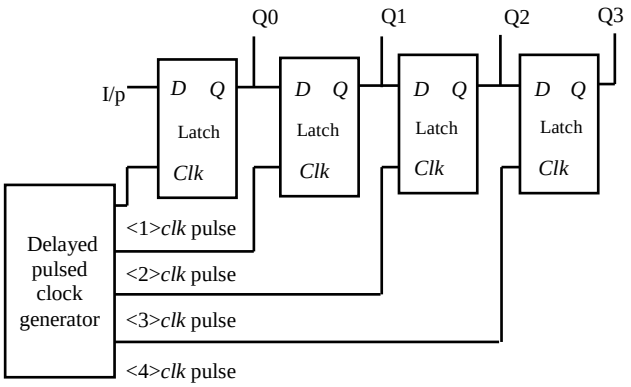

Fig.7. proposed SIPO Shift Register

3.3 PROPOSED PISO SHIFT REGISTER

The implementation of PISO using pulsed latch technique is shown in Fig.8. As it can be seen in the figure, parallel inputs D0 to D3 are provided to each latch respectively. When the value of control signal Shift/load is low, input is loaded in each latch. When the value of control signal Shift/load is high, the shift operation is done and output is taken out serially from last latch. This application of pulsed latch technique is used to add more binary inputs to microprocessor than available ones.

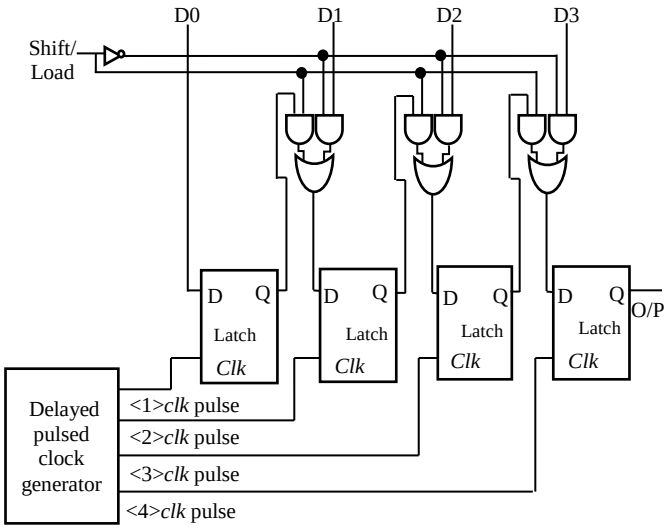

Fig.8. Proposed PISO Shift Register

3.4 PROPOSED PIPO SHIFT REGISTER

The implementation of PIPO using pulsed latch technique is shown in Fig.9. The main feature of this implementation is that the output is obtained instantly from each latch as soon as the input is given to each latch. Once the latches are triggered with pulse clock, input given to latch provides the output simultaneously.

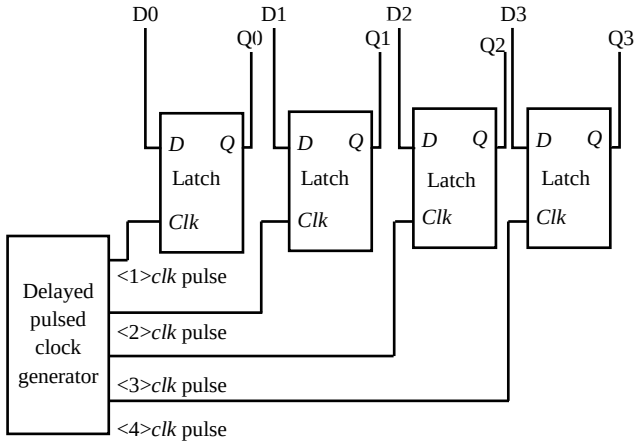

Fig.9. PIPO using pulsed latch Shift Register

3.5 PROPOSED UNIVERSAL SHIFT REGISTER

Universal shift register using pulsed latch is shown in Fig.10. The delayed pulse clock generator is utilized in this implementation. All the shift and loading operations can be done in universal shift register i.e. parallel loading, taking parallel output, shifting right or shifting left. The mode of operation of the register is controlled by select lines of multiplexer and explained in tabulated format in Table.1.

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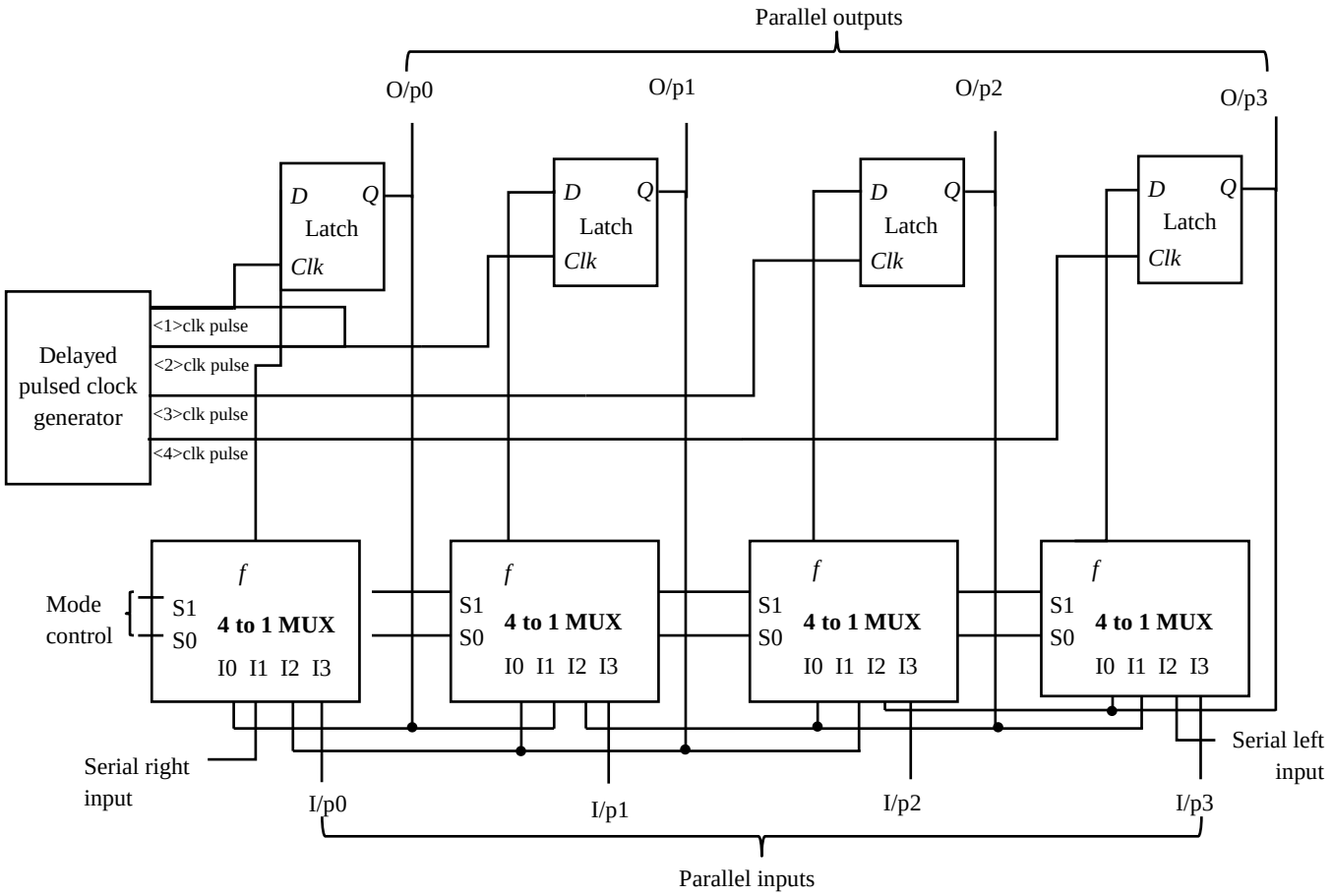

Fig.10. Proposed Universal shift register

Table.1. Mode of operation

Select lines S1 S0	Mode of operation
0 0	Hold
0 1	Shift right
1 0	Shift left
1 1	Parallel load

4. SIMULATION RESULT AND DISCUSSION

Simulations of all the circuits were performed in Cadence Virtuoso using 90nm CMOS technology. The supply voltage is varied from 1.2V to 2V and clock frequency of 200MHz is used. All the proposed shift registers have been compared with conventional versions which are designed using D flip-flop. The D Flip-flop is by far the most important of the clocked flip-flops as it ensures that ensures that inputs S and R are never equal to one at the same time. The Fig.11 shows the results for D flip-flop shown in Fig.2. From the results is can be seen that at negative edge of clock, output follows the input and last waveform provides average power dissipation in flip-flop. Thus D flip-flop tracks the input, making transitions with match those of the input D.

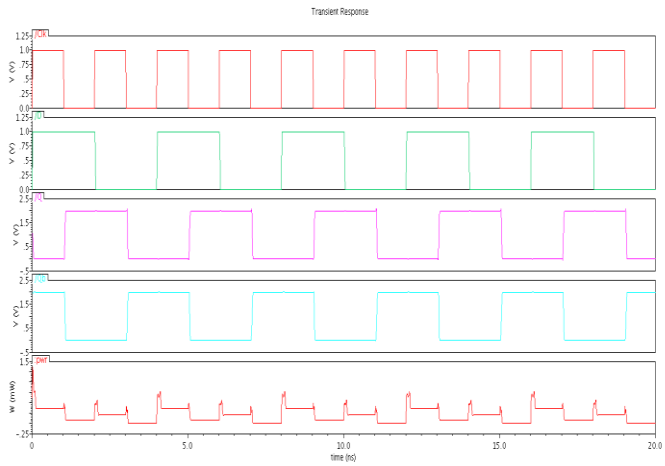

Fig.11. Flip-Flop waveform

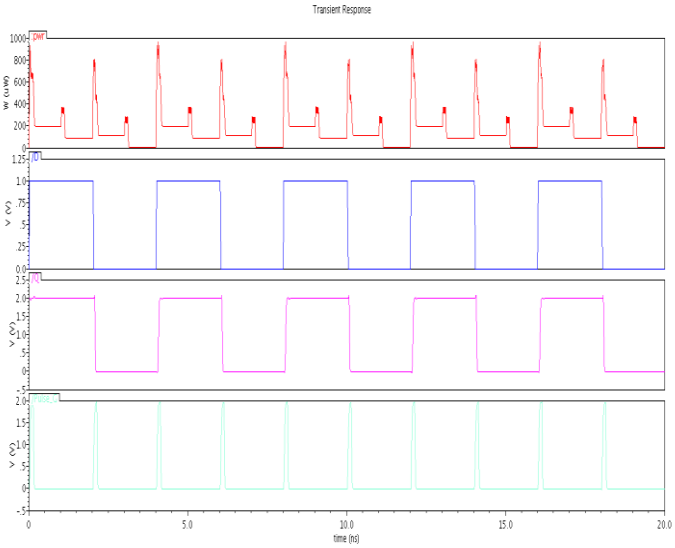

Fig.12. Pulsed latch waveform

The Fig.12 shows the waveform for pulsed latch circuit in Fig.3. At every clock pulse, output follows the input and red waveform provides the average power consumption in the circuit. As pulsed latch technique share the pulses from the Pulsed clock generator therefore due to this sharing of the pulse generation circuit the area and power consumption of the circuits reduces significantly

Table.2. Comparison of performance parameters of D latch, D flip-flop, Pulsed latch

Parameter	D latch	D flip-flop	Pulsed latch
Power (uW)	3.395	206.9	167
Delay (ps)	238.4	52.76	51.49
Power delay product (fWs)	0.81	10.91	8.59
No. of transistors	16	34	24

The Table.2 summarizes the results obtained for D latch, D flip-flop and pulsed latch. It is observed that pulsed latch technique has better performance. The power dissipation, power delay product and transistor count is reduced using pulsed latch technique. This technique saves 19% of power consumption and improves power delay product by 21.26% as compared to flip-flop.

The Fig.13 shows the output of delayed pulse clock generator which gives five delayed pulses of 126ps pulse width for 200MHz clock frequency input.

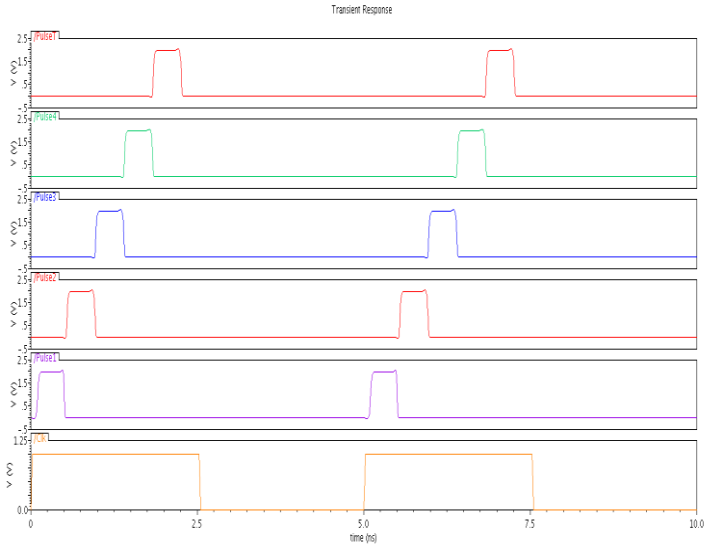

Fig.13. Delayed pulse clock generator waveform

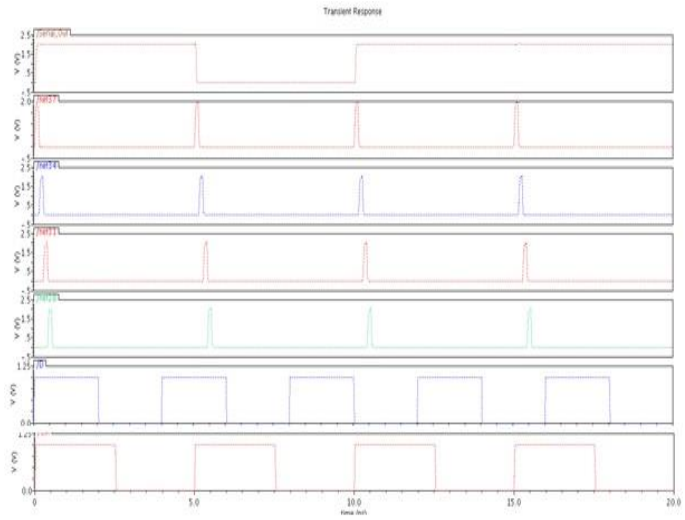

Fig.14. Proposed SISO shift register waveform

In Fig.14, waveform of operation of SISO shift register is shown, where serial out is obtained for serial in according to clock pulses.

Table.3. Power delay product performance of SISO Shift register

SISO Shift Register	Delay (ps)	Power Consumption (µW)	Power delay Product (fWs)
With D flip-flop	50.6	541.8	27.41
With pulsed latch technique	24.34	246.3	5.99

The Table.3 provides the simulation results which states that the implementation of SISO shift register using pulsed latch have better performance in comparison to SISO shift register using flip-flop.

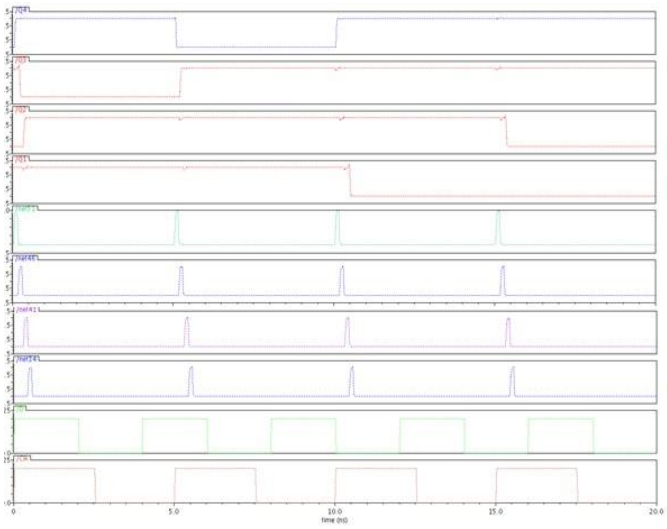

Fig.15. Proposed SIPO shift register waveform

The working of SIPO shift register is verified through waveform provided in Fig.15, for serial input adjacent parallel output was taken.

Table.4. Power delay product performance of SIPO Shift register

SIPO Shift Register	Delay (ps)	Power Consumption (µW)	Power delay Product (fWs)
With D flip-flop	44.79	541.8	24.26
With pulsed latch technique	34.31	246.3	8.45

From Table.4, it is clear that power consumption and power delay product reduces for SIPO shift register using pulsed latches rather than SIPO shift register using flip-flop.

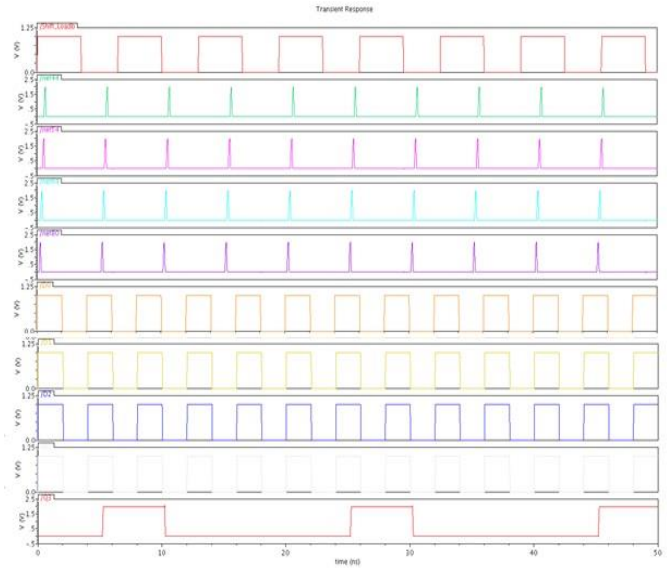

Fig.16. Proposed PISO shift register waveform

In Fig.16, shows the working of PISO shift register using pulsed latch has been proved, the same parallel input is given to all latches and serial output taken from last latch.

Table.5. Power delay product performance of PISO Shift register

PISO Shift Register	Delay (ps)	Power Consumption (µW)	Power delay Product (fWs)
With D flip-flop	35.87	660.1	23.67
With pulsed latch technique	27.67	489.7	13.55

The Table.5 summarizes that performance of PISO shift register using pulsed latch provides reduced power consumption and power delay product with respect to PISO shift register using flip-flop.

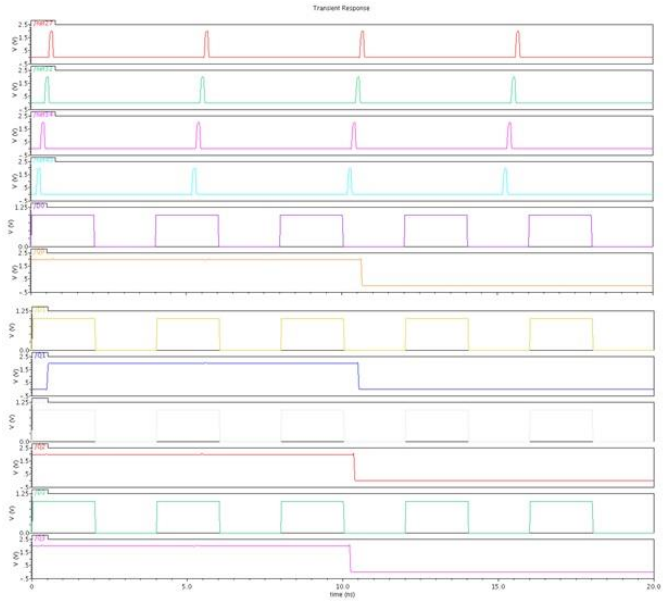

Fig.17. Proposed PIPO shift register waveform

The operation of PIPO shift register is clear through the waveform provided in Fig.17. The input to each latch is provided at that respective latch output when pulsed clock is encountered.

Table.6. Power delay product performance of PIPO Shift register

PIPO Shift Register	Delay (ps)	Power Consumption (µW)	Power delay Product (fWs)
With D flip-flop	159	436	69.32
With pulsed latch technique	37.62	406.3	15.28

From Table.6, it can be briefed that the power delay product is significantly reduced for PIPO shift register using pulsed latch with respect to PIPO shift register using flip-flop while power consumption also is quiet low.

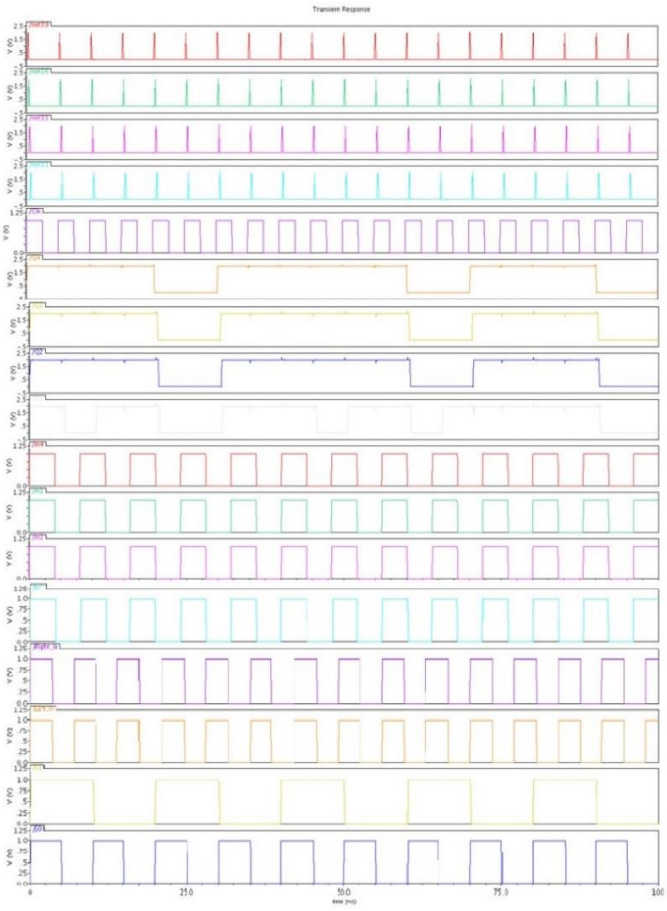

Fig.18. Proposed Universal shift register waveform

Universal Shift Register can be configured to load and/or retrieve the data in any mode i.e. either serial or parallel by shifting it either towards right or towards left. Thus a combined design of unidirectional (either right- or left-shift of data bits as in case of SISO, SIPO, PISO, PIPO) and bidirectional shift register along with parallel load provision is universal shift register. From Fig.18, the working of universal shift register has been verified. By changing the values of control signals S1, S0 the operation of universal shift register was controlled and respective output was obtained.

Table.7. Power delay product performance of Universal Shift register

Universal Shift Register	Delay (ps)	Power Consumption (µW)	Power delay Product (fWs)
With D flip-flop	56	2.351	131.65
With pulsed latch technique	43.31	2.09	90.51

The performance improvement of proposed registers using pulsed latch technique is listed in tabulated form in Table.8.

Table.9. Percentage improvement in the performance of shift registers using pulsed latch technique

Proposed design using pulsed latch technique	% reduction in power consumption	% reduction in power delay product
SISO shift register	54.5	78.14
SIPO shift register	54.5	65.16
PISO shift register	25.81	42.75
PIPO shift register	6.81	77.95
Universal shift register	11.1	31.2

From the simulation results it has been inferred that Pulsed latch saves power consumption and delay with respect to flip-flop. Hence the application of pulsed latch shows better performance in comparison to flip-flop.

5. CONCLUSION

Replacement of flip-flop with pulsed latch can save appreciable amount of power consumption hence now days it is preferred in low power ASIC design. This paper proposed different types of shift registers using pulsed latch technique in 90nm CMOS technology. The number of transistors utilized in pulsed latch is less than that of flip-flop, hence area is significantly reduced. Pulsed latch circuit saves 19% of power consumption and 21.26% power delay product in comparison with flip-flop circuit hence it can be inferred from the results that the circuits using the pulsed latches can be used instead of flip-flop for low power, less area and high speed applications. Pulsed latches are faster than flip-flops and offer some time borrowing capability at the expense of greater hold times. They have fewer clocked transistors and hence lower power consumption. The advantages of pulsed latch over flip-flop are saving clock period, power consumption, delay and area. The trading towards applications using pulsed latches from conventional flip-flop circuits in heavy pipelining, mobile devices or in low power ASIC circuits is immense achievement in field of VLSI designing. The proposed designs have been evaluated and analyzed in a standard 90nm CMOS technology in Cadence.

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