# CNTFET BASED NOVEL 14T ADDER CELL FOR LOW POWER COMPUTATION

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*Abstract*

*This paper focuses on the design of a 14 transistor one bit adder cell designed using CNTFET 32nm Technology to address the power and speed issues of high performance computational systems. The performance metrics of the proposed adder cell is compared by benchmarking with conventional full adder design, Transmission gate based full adder and Shannon's expression based full adders using CNTFET technology. The proposed design has lesser delay and very low power consumption. The design embraces Stanford 32nm planar CNTFET library model with a power supply of 1 volt and single walled CNT. Extensive simulation has been carried out on the adder cells considered and the parameters such as power, delay and PDP are investigated. The effect of temperature variation on the power consumption of proposed 14T adder cell is also observed to examine the robustness. The simulation results demonstrate that the proposed adder delivers stable output drivability with substantial diminution in the leakage power.*

*Keywords:*
*CNTFET, Adder Cell, Full Adder, Low Power, PDP*

## 1. INTRODUCTION

Development of carbon nanotube based transistors in building digital systems is playing a spirited role in today's shrinking technology and bids various advantages such as high channel mobility and improved gate capacitance against input gate voltage. The ITRS is focussed on the research of post silicon devices to build efficient logic circuits and it is witnessed that carbon nano tube transistors supports this extensively w.r.t scaling and performance. The evolution in CNT device modelling shall open contests to accelerate the research in nano-scaled devices and circuits under sub 32nm regime. The design of adder circuits based on CNTFETS is an important area of research and it is crucial for uniting computational logic in SoCs. These devices have enormously constructive Characteristics in submicron regime in comparison with conventional MOSFETs and yields greater performance when considered for SoC design. Due to the similarities in the operational characteristics with that of MOSFET and a low off state-current during cut-off, the CNTFET appears to be more promising successor to the conventional MOSFET technology [2]. Implementation of adders using CNTFET leverages the advantage of fast processing when employed in multiply and accumulate (MAC) units of SoCs. There are several variants of adders such as carry save adder, carry look-ahead adder, ripple carry adder etc., that form the important logic blocks for multi bit addition chains.

This work focuses on the performance of a single bit full adder cell that performs the arithmetic operations in ALU of any processor. Though the function of full adders is to add or subtract a 1-bit binary number, the structure with which it is built is responsible for the performance metrics of it and in turn affects the entire computational block. A full adder can be implemented in many ways such as with a full custom transistors or with a logic composed of XOR/XNOR gates or by using any suitable pass transistor logic which consumes a minimum logic density. Also in conventional way a one bit full adder can be constructed from cascading two half adders and the circuits can be operated to carry out parallel addition or subtraction. The evolution of realizing different adders always highlights area efficient and power efficient computation under process constraints. In addition to this, if incorporation of CNTFET devices to build the logic is engaged, we leverage the several advantages of scaling. However, the proper selection of CNTFET device model parameters to support the miniaturization of systems is an important concern of the design. The speed of computation is major constraint in latest high frequency processors that are designed to be suitable for image and video processing. The rapid growth of portable electronic devices like mobile phones has driven the research towards low power implementation of the digital logic because of the lacuna in battery and power storage technology which has not advanced at the rate of microprocessor integration technology as predicted by Moore [5].

To overcome the limitation of battery technology, it is highly necessary to implement logic that consumes minimum power even under high speed computation. In the conventional adder cell design using complementary MOS logic, the expressions for Sum and Carry outputs is obtained by MOSFET like ballistic planar CNTFET pull up and pull down transistors and in building this cell, it is important to consider the effect of aspect ratio of the devices on the performance. This work uses CNTFET 32nm process technology to attain minimum aspect ratio and low power consumption for the devices.

This design work has been has been initialized with the conventional approach to construct the adder cell with CNTFET adders having complimentary pull-up PCNTFET and pull down NCNTFET networks. This adder required 42 transistors for generating sum and carry outputs. An alternative adder design using XOR logic and transmission gate is also investigated in which the transistor count is reduced to 30 when we build transistor level XOR gates to attain adders.

The power consumption is also greatly reduced when operated at temperature of 26 degree Celsius. After the performance analysis of the above mentioned designs, in this paper it has been worked on the design of a CNTFET based 14 transistor full adder cells and compared the same with the simulation results of conventional and Shannon's expression based full adders, at the same process technology.

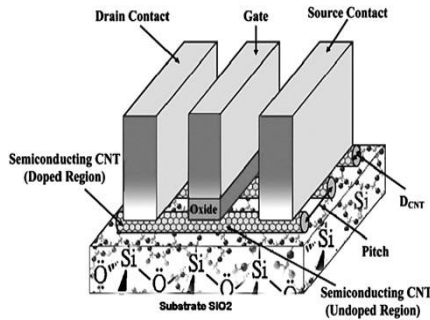## 2. REVIEW OF CNTFET TECHNOLOGY



Fig.1. Structure of CNTFET [3]

A layer of graphene known as graphene ribbon is the parent material to form a CNT. It is a honeycomb lattice layer consisting of $sp_2$-hybridized carbon atoms. Each unit cell of the graphene ribbon is defined by the vectors $a_1$ and $a_2$ as depicted in Fig.1. The tube is formed by rolling the sheet based on the chiral axis parallel to the translational vector $T$ [2].

$$d = \frac{a_{cc}\sqrt{3(n^2 + m^2 + nm)}}{\pi} \quad (1)$$

From Eq.(1) $a_{cc}$ is 1.44Å is the distance between the nearest neighbor carbon atoms in graphene sheet and integers $m$ and $n$ are chosen such that always $0 \leq m \leq n$.

From Eq.(2), the angle $\theta$ formed between $C_h$ and $a_1$ is very important in measuring the electronic properties of the single walled carbon nano tube. It is known as the angle of chirality [2].

$$\cos\theta = \frac{2n + m}{2\sqrt{(n^2 + m^2 + nm)}} \quad (2)$$

The single walled CNTs can be categorized into two types: [3] Zig Zag and armchair nanotubes having chiral values, $C_h = (n,n)$ and $C_h = (n,0)$, respectively [2]. In the proposed work, we have considered a planar MOSFET like CNTFET with zigzag semiconducting SWCNT to determine the voltage vs drain current characteristics upon variation of diameter. The diameter size of CNT will influence the drain current $I_d$ and in turn the on/off characteristics of the device. Planar CNTFETs are widely fabricated as they offer compatibility to fabrication technologies similar to that are used in existing MOS device fabrication [3].

CNTFETs can be fabricated with Ohmic or Schottky contacts. Mechanism of current transportation and IV characteristics are dependent on the type of the contact. In the SB-CNTFETs, metallic electrodes are utilized and tunneling of electrons and holes from potential barriers at the source and drain junctions constitutes the current [4]. The SB brings high resistance in CNT–metal junction and reduces the on-current of the CNTFET. Moreover, SB-CNTFETs are ambipolar. In ohmic contact heavily doped source and drain are used and lock of SB in source channel causes lower off leakage current and higher on-current [1]. The IV characteristic of the ohmic contact CNTFET is similar to the MOSFET. Therefore, CNTFET with ohmic contact is known as MOSFET-type CNTFET and is more suitable for circuit design based on CMOS architecture. Desired threshold voltage in CNTFET can be adjusted by changing the nanotube diameter easily. This privilege makes it perfect to design MVL circuits. The CNTFET threshold voltage can be computed based on the Eq.(3),

$$V_{th} = \frac{0.43}{D_{CNT}(nm)} \quad (3)$$

From Eq.(3), $V_\pi$ = 3.033 eV is the carbon $\pi$–$\pi$ bond energy in the tight bonding model, $e$ is the unit electron charge and DCNT is the CNT diameter as per Eq.(1), the threshold voltage of the CNTFET is inversely related to the nanotube diameter [1].

Table.1. CNTFET Device Model Parameters Considered for Proposed Adder Cell

| Parameter | Description | Value |
|---|---|---|
| $L_{ch}$ | Physical channel length | 32nm |
| $L_{geff}$ | Free path in intrinsic channel | 100nm |
| $L_{ss}$ | Source side extension length | 32nm |
| $L_{dd}$ | Drain side extension length | 32nm |
| $K_{gate}$ | Dielectric constant | 16 |
| $T_{ox}$ | Oxide thickness | 4nm |
| $C_{sub}$ | Coupling capacitance between channel and substrate | 40 pF/M |
| Pitch | Distance between adjacent CNTs | 20nm |

## 3. PREVIOUS WORK

In recent developments of VLSI technology, numerous works have been carried out in designing the low power adder cells, the structure of conventional adder is altered such that binary or ternary operation is achieved to derive the sum and carry of the adder cell. In [8] the design incorporates the Ternary logic function where inverter and gates are used as logic cells built using standard ternary inverter (STI), Positive ternary inverter (PTI) and negative ternary inverter (NTI) Techniques. This design involves usage of decoder circuit to drive the inputs for half and full adder cells. The advantage is that we can perform computation in three different voltage levels. Another method used in implementation of adder cells is the use of Gate diffusion input (GDI) technique which uses a GDI cell having inputs to driver and load devices along with that of the gate input. [14] Has proposed a CMOS full adder built using XOR logic using GDI technique. Though this method can be area efficient, there is a huge impact of body effect on this design, since there are three inputs employed for the GDI design, any little amount of variation substrate potential can increase the threshold voltage and can cause increased power dissipation and also increased delay. The Fig.2 represents the CMOS GDI adder cell used in [14].

To board for low power computation of the cell, this work firstly follows the classical approach of designing adder cell using standard expressions of sum and carry and then uses the pass transistor and transmission gate method. The 32nm CNTFET device model is used to authenticate the performance for low power requirement. The designs using pass transistor logic and TGs has a drawback of threshold voltage drop and tend to reduce the delay. In [15] CMOS adder cell is built using TGs and TFA logic obtaining the sum and carry output under supply voltage variation. Apart from the above styles, there are other hybrid

methods incorporating XNORes and MUXes for binary or ternary logic to arrive at the SUM and Carry outputs.
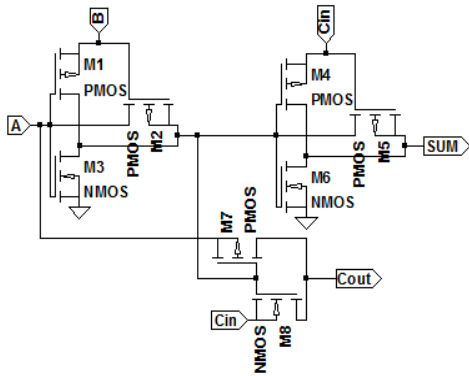


Fig.2. CMOS full adder using GDI inverter cells [14]

In addition to the above there are other designs in the literature which operate the cell at low voltages to target low power dissipation, but reducing the power supply will reduce the driving strength of the cell and adversely affects the voltage scaling into various parts. Along with the some primary techniques, this work also emphasizes on investigating the performance of Shannon's expression based adder cell, which is one of the area and power efficient techniques to assess the adder performance. The proposed 14T CNTFET full adder performance is benchmarked with the primary adder designs enumerated above.
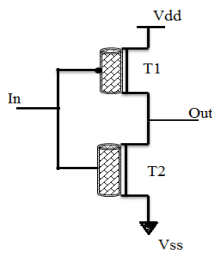
## 3.1 CNTFET INVERTER LOGIC



Fig.3. CNTFET Inverter

The digital inverter is a basic building block in various digital systems, $T_1$ is the PCNFET forming the pull up device and $T_2$ is the NCNFET forming the pull-down device. In the proposed 14T adder cell, the CNTFET inverter is used to obtain the complemented logics of inputs $A$, $B$ and $C_{in}$. The proposed adder uses SWCNTs with 3 tubes and chirality of (0,13) and a pitch of 20nm. This paper examines the various structures of one bit full adder logic implemented by CNTFETs and executed comparative analysis with proposed 14T mux based full adder targeted for low power consumption

## 4. ADDER DESIGN USING CNTFETS

In this work, the initial part of conventional CNTFET full adder design has incurred 42 transistors including that of complemented inputs based on the expressions of Sum and carry. Since number of transistors count is more, the research of adder design has traversed with many different logic structures that are area efficient or power efficient in achieving the output expressions [6]. In the design of full adder by cascading two half

adders stages, we need 12 transistors for each half adder stage and an AND gate logic for carry output comprising of 6 transistors as depicted in Fig.5. In this work we have initially designed and simulated the conventional FA with 42T. The transient analysis of this conventional FA at the normal temperature of 26 degree Celsius has delivered a worst case time delay of 502 ps for the input to output propagation. The maximum power consumption of the conventional 42T full adder is found out to be around 98.79 µW because of swift switching of transistors for different input combinations. Hence this work examines towards the adder cell design with less transistor count and low energy consumption. The reduction in transistors leads to reduced parasitic capacitance and reduced output leakage current.
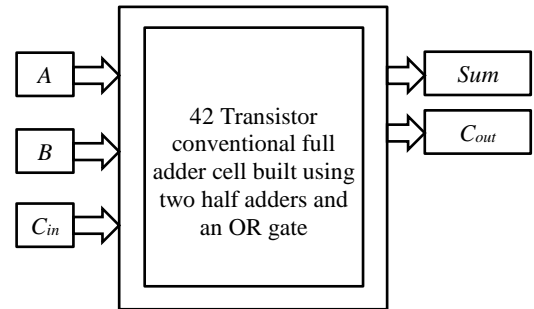


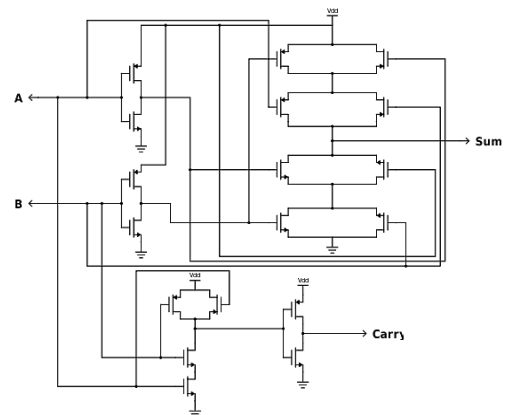Fig.4. CNTFET based 42T conventional full adder cell



Fig.5. CNTFET based conventional 18T half adder

The Fig.5 depicts the schematic CNTFET based half adder cell having 18 devices to design the half adder output logic of Sum and carry expressions. This design was net listed with CNTFET 32nm library model. The Fig.6 depicts the schematic of modified half adder cell with transmission gate (TG) and an AND gate to attain the output expressions.

The conventional full adder cell having three inputs $A$, $B$ and *Carry-in* ($C_{in}$) and outputs Sum and carry is obtained using cascading of two half adder circuits. The first half adder is used to add $A$ and $B$ to produce a partial Sum. The second half adder is used to add $C_{in}$ to the partial Sum produced by the first half adder to get the final SUM output. The Fig.4 depicts the CNTFET based conventional full adder incurring 42 devices built with CNTFETS and simulated using HSPICE.
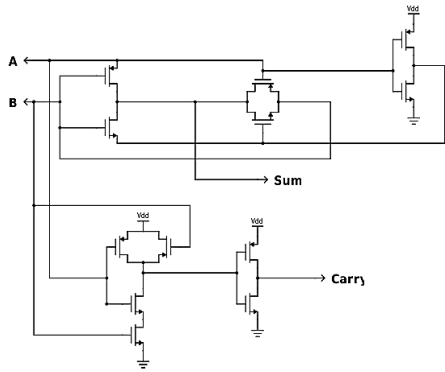
Fig.6. CNTFET based half adder cell using TG

## 4.1 SHANNON'S FULL ADDER

The design of CNTFET full adder with Shannon's expansion method reduces the transistor count and makes the design area efficient. The Shannon theorem elucidates that the logic expressions are divided into two parts wherein in the first part a variable value is set to logic 1 and multiplied by a multiplier variable and in the next part the original variable that was set to logic 1 is then set to logic 0 followed by its multiplication with complement of multiplier variable. The entire logic can be reduced by reiterating the Shannon's theorem [5]. The generalized Shannon expression of many variables is as depicted below.

The $f(a_0, a_1, a_2, y, a_i, y, a_n)$ can be written as the sum of two terms, one with a particular variable (say $a_i$) set to 0, and one with it is set to 1 [5]. $f(a_0, a_1, a_2, \ldots, a_i, \ldots, a_n) = a_i' f(a_0, a_1, a_2, \ldots, 0, \ldots, a_n) + a_i f(a_0, a_1, a_2, \ldots, 1, \ldots, a_n)$ [6].

The Fig.7 represents the Shannon's full adder network built with CNT devices and simulated in HSPICE environment. In this ($n$-1) variables are used as control inputs connected to gates of the transistors based on whose value the data available at inputs of the pass transistors are transmitted towards the output [5]. In case of a one bit full adder in Fig.5, the input $B$ and complement of $B$ deliver transmission path to original and complimented variables of $A$ and $Carry$-$in$, Thus realizing the sum expression in a simple transistor structure. In Shannon's adder it is important to note that control signal lines are connected to gates to control the switching and the data inputs are connected to drains of the transistors to pass the data.
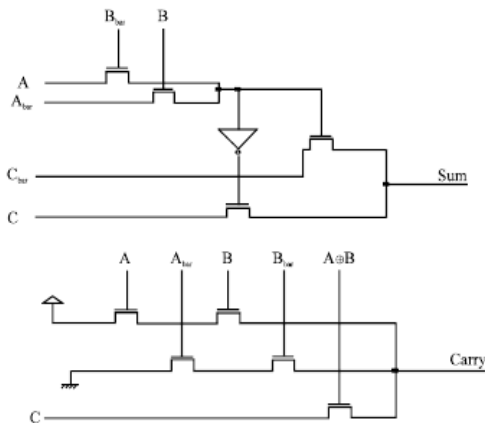


Fig.7. CNTFET based Shannon's expression based full adder cell

In carry out design we use carry in from a previous stage, $V_{dd}$ (logic 1), and ground (logic 0) as pass variables. In Shannon's full adder, the sum logic is a two input XOR operation built with multiplexer method

## 5. PROPOSED 14T CNTFET ADDER CELL

Adder accomplishment using CNTFETs has become fascinating topic in computational research in current shrinking technology due to the significance of targeted constraints such as area, power and speed. This paper proposes a one bit full adder by using 14 CN transistors depicted in Fig.8, targeted for low power consumption. The proposed design features conventional logic inversion wherever needed and avoided the Shannon based pass transition method for sum and carry. In the proposed circuit, by not using pass transistors it has been improvised to reduce the effect of signal degradation that occurs due to passing of data in a longer adder chains. $T_1$ to $T_6$ devices are used for signal complementing while other transistors build the sum and carry logic function of the full adder. Since the design incorporates a low operating voltage of one volt, and a transistor count of 14 the design yields lesser power consumption and less losses due to parasitic capacitances. Also the problem of voltage swing restoration can be circumvented. The propagation speed from any of the three inputs to sum or carry outputs is also improved. The 14 transistor CNTFET adder is faster than that of 30 transistors and 42T based full adders discussed earlier. This is achieved because of the implementation of three multiplexers implemented with two NCNFET transistors is as depicted in Fig.7 to select among input combinations of $A$, $B$ and $C_{in}$. The maximum power consumption is significantly reduced to 1.39μW compared to all the designs discussed earlier.
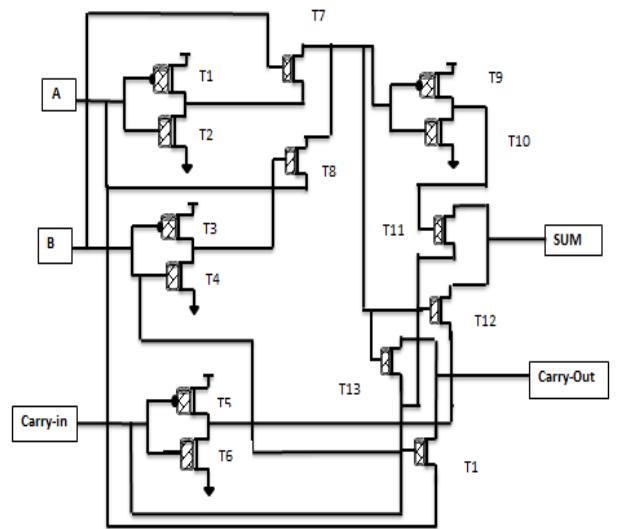


Fig.8 Proposed 14T full adder using CNTFET 32nm Technology and chirality of single walled zigzag tubes with ratio (0,13)

The Fig.9 depicts the input-output timing diagram of 14-T CNTFET adder circuit with inputs A, B and $C_{in}$ and outputs C-out and SUM as depicted. It is evident that the timing diagram obtained satisfies the one bit addition operation with little or no glitches for all input combinations. The circuit is simulated in full custom method in HSPICE with CNTFET 32nm Stanford library

models for targeted performance metrics such as power consumption, delay and PDP that are tabulated in next section.
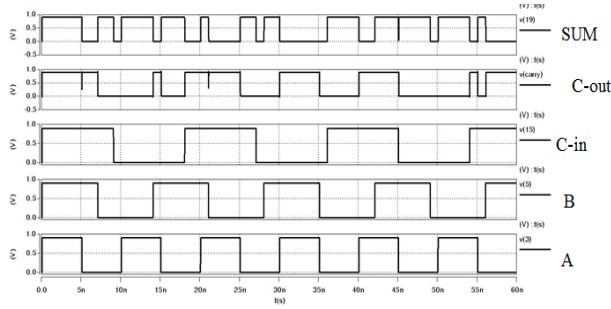


Fig.9. Input Output timing diagram of 14-T CNTFET adder circuit

# 6. COMAPARITIVE ANALYSIS

In these section comparative analyses is carried out for the proposed adder cell with respect to power, delay and PDP with respect to conventional and Shannon adders.

In Table.2, the output metrics of the proposed CNTFET 14T adder are compared with that of CNTFET based conventional 42T full adder, Transmission gate based 30T full adder and Shannon's full adder. The proposed adder outperforms the other adder circuits considered in all output parameters under load and temperature variation. The 14T CNTFET adder has an average power consumption of 30.15μW under normal operation. This leverages the advantage of energy efficiency in multi bit operation where a chain of adder cells are forming the logic block to drive the sum and carry outputs. The worst case delay is measured through the SPICE programming techniques of delay measurement using the relations $T_d = (T_{plh} + T_{phl})/2$ between an input and output signal at 50% signal amplitude. The time consumed between mid-point of signal low to high and high to low of input and output parameters is recorded for tracing the worst case delay. It is observed that the proposed adder has drastic enhancement in delay parameter which is vital for high speed computation.

The Table.3 and Table.4 depict the impact of variation of temperature and variation of load respectively on the delay of the proposed adder cell. The delay and PDP under load and temperature variation is recorded to assert the stability of the cell. It is found that the energy consumption of the circuit is as less as $1.80 \times 10\text{-}17$ (J) with a power supply of 1V.

Table.2. Comparative analysis of proposed adder with other adders of literature

| Parameter | Delay in Pico-Seconds | Delay in Pico-Seconds |
|---|---|---|
| Type | Conventional 42T CNTFET FA With Operating Temperature $26^0$ C and Load Capacitance 1fF | HA cascaded 30T CNTFET FA With TG Operating Temperature $26^0$ C and Load Capacitance 1fF |
| Input A to Sum | 502.1 | 705 |

| | | |
|---|---|---|
| Input A to Carryout | 355 | 758 |
| Input B to Sum | 325 | 388.2 |
| Input B to Carryout | 489 | 163 |
| Input $C_{in}$ to Sum | 115.68 | 168 |
| Input $C_{in}$ to Carryout | 241.53 | 502 |
| Worst case delay | 502.1ps | 758ps |
| Average Power | 98.79uW | 86μW |
| **Parameter** | **Delay in Pico-Seconds** | **Delay in Pico-Seconds** |
| Type | Shannon's18T CNTFET FA With Operating Temperature $26^0$ C and Load Capacitance 1fF | Proposed 14T CNTFET FA With Operating Temperature $26^0$ C and Load Capacitance 1fF |
| Input A to Sum | 19.16 | 12.21 |
| Input A to Carryout | 18.8 | 7.78 |
| Input B to Sum | 20.77 | 4.08 |
| Input B to Carryout | 17.22 | 6.91 |
| Input $C_{in}$ to Sum | 15.68 | 4.46 |
| Input $C_{in}$ to Carryout | 20.23 | 7.78 |
| Worst case delay | 20.77ps | 12.21ps |
| Average Power | 45μW | 30.15μW |
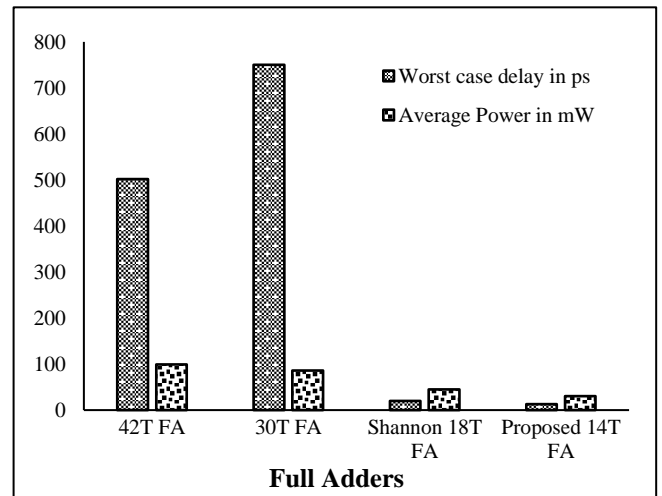


Fig.10. Comparative analysis of considered adder cells with proposed adder cell

Table.3. Power consumption of proposed adder with variation in temperature with an input power supply of one volt

| Temperature ($0C$) | WC delay (Sum) Pico Seconds | WC delay carry Pico Seconds | Power (μW) | PDP $\times 10^{-17}$ (J) |
|---|---|---|---|---|
| 26 | 12.21 | 7.78 | 1.39 | 1.69 |
| 50 | 12.21 | 7.78 | 1.39 | 1.69 |
| 75 | 12.5 | 8 | 1.4 | 1.73 |
| 100 | 13.0 | 8.2 | 1.4 | 1.80 |
| 150 | 13.0 | 8.2 | 1.4 | 1.80 |

Table.4. Power consumption of proposed adder with variation in load capacitance

| Voltage (V) | Load (fF) | WC delay (Sum) Pico Seconds | WC delay carry Pico Seconds | Power (µW) | PDP × 10⁻¹⁷ (J) |
|---|---|---|---|---|---|
| 1 | 1 | 12.21 | 7.78 | 1.4 | 1.73 |
| | 2 | 12.21 | 7.78 | 1.4 | 1.73 |
| | 3 | 12.5 | 8 | 1.4 | 1.73 |
| | 4 | 13 | 8.2 | 1.42 | 1.80 |
| | 5 | 13. | 8.2 | 1.42 | 1.80 |

## 7. CONCLUSION

The Proposed CNTFET adder circuit is designed for low power operation and a stable logic propagation using new 14T logic with 32nm device scaling. The design used a maximum power supply of 1 volt and attaining an average power dissipation of 1.39 micro watts is a swift improvement in comparison with the adder structures considered from the literature. The design has also yielded the results that are rather less in power dissipation under linear variation of load capacitance and temperature. The proposed CNTFET adder also possesses a low and steady propagation delay when compared to the compact Shannon's expression based full adder. With lesser delay due to its transistor architecture, the influence of this adder cell in high speed data computation systems will be effectual and with exploiting the merits of CNTFET technology, the proposed design can be a pragmatic logic element in a low power and high speed ALU design.

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