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DESIGN AND SIMULATION OF A 10 GSPS LOW POWER SAMPLE AND HOLD LESS ANALOG TO DIGITAL CONVERTER USING CARBON NANOTUBE FIELD EFFECT TRANSISTORS

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Abstract

A 5 bit sample-and-hold less pipelined ADC is presented for high speed and low power applications. The architecture is designed using 32nm CNFET model in Hspice and simulation is carried out at 10 GSPS sampling rate. From the simulation results, the SNDR is found out to be 32.89dB at Nyquist frequency and the ERBW is found to be 3GHz from 2 to 5GHz in which ENOB is guaranteed to be above 4.6. The average power consumed is 5.031mW for a supply voltage of 1.4V and FoM is 53.32fJ/step.

Keywords:

CNFET, ADC, Pipelined, GSPS

1. INTRODUCTION

Multi-Giga-samples per second Analog to Digital converters (ADCs) that could work at as low power as possible, preferably a few milliwatts, are a need of time as the next generations of communication systems continue to emerge. Medium resolution ADCs working at low power levels, particularly in the ISM band i.e. 2 to 5GHz range will serve as a boon from the applications perspective. There have been implementations of such multi-GSPS ADCs working around 5 to 10 GSPS range using the Complementary Metal Oxide Semiconductor technology with various architectures such as pipelined, time-interleaving, Successive Approximation Register (SAR) and flash with flash being the most popular choice of architecture [1-5].

With the emergence of newer technologies such as Carbon Nanotube FETs [6-7] which require 6 times less current and with gate capacitance which is about 1000 times less than their CMOS counterparts, an ADC built with CNFET is bound to be better in terms of speed and power both than that of CMOS. Attempts have been made to simulate a 3 bit ADC with CNFET [8], but with the use of Flash architecture which has the well-known disadvantages of substantial area and power requirements as the resolution is increased. A pipelined architecture can overcome these disadvantages because the power and area requirements increase linearly with increase in resolution in case of pipelined architecture as opposed to the quadratic increase in power and area with increase in resolution in case of Flash [9].

Hence, this work aims at designing and simulating in Hspice an ADC with 5 bit resolution, working at only a few milliwatts and at speed of 10GSPS, with CNFET model defined for 32nm in [6-7] using a sample and hold less pipelined architecture. Although the designs of sub-circuits in the pipelined architecture may seem traditional, the use of CNFET for their implementation significantly makes them faster and more power efficient.

Section 2 describes the proposed one bit per stage pipelined architecture. Section 3 describes the developments of individual blocks in the one bit stage. Section 4 describes the adjustments done in the architecture and how the need for sample and hold has been eliminated. Section 5 gives the static and dynamic performance parameters of the ADC done with Hspice simulation. Concluding remarks along with comparison with state-of-the-art is given in section 6.

2. DESIGN OF PIPELINED ARCHITECTURE

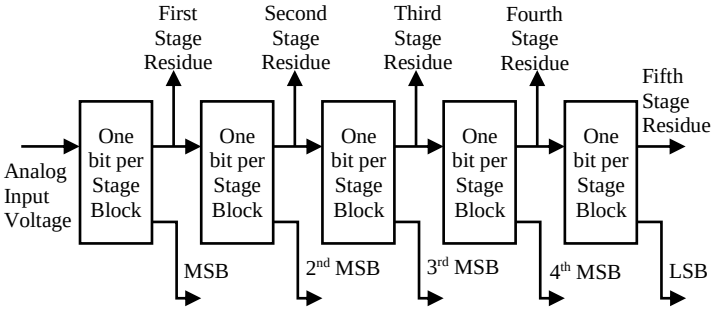


Fig.1. Pipelined architecture of ADC

The architecture of the 5 bit pipelined ADC is as shown in the Fig.1. It is implementation of the binary search algorithm with one bit per stage by comparing the analog input with (V_{max}/2) as the threshold voltage of the comparator and calculating the appropriate residue in each stage to be sent over to the next stage.

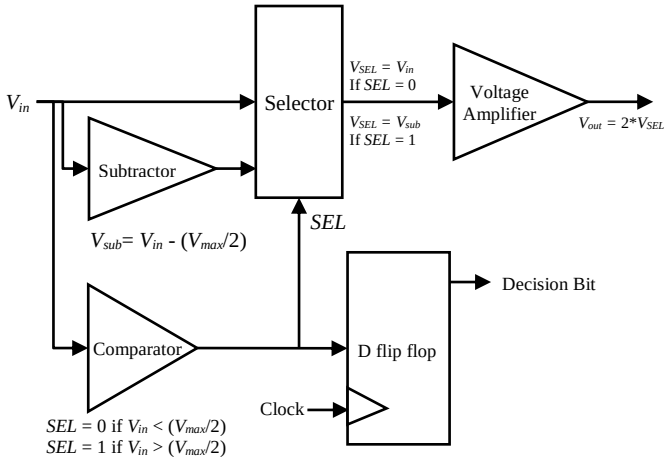


Fig.2. One bit per stage block

The residue is calculated based on the decision of the comparator using following algorithm:

$$V_{residue} = 2V_{in} \text{ if } V_{in} < (V_{max}/2)$$
$$V_{residue} = 2(V_{in} - (V_{max}/2)) \text{ if } V_{in} > (V_{max}/2) \quad (1)$$

The decision for the most significant bit (MSB) is given by the first stage and the significance of the bits decreases for each successive stage, the fifth stage giving the decision of the least significant bit (LSB).

Generally, two stages of pipelined ADC have a sample-and-hold block in between for the independent working of the stages but if it is made sure that the settling time for sub-circuits in each individual stage very small then a sample-and-hold less approach can also be experimented with. Here such sample-and-hold less approach is attempted.

The Fig.2 shows the internal details of the One-bit-per stage block. The selector is a switch passes the appropriate residue to the next stage depending upon the comparator output. The decision bit i.e. the output of the comparator is sampled by using a flip/flop. The voltage amplifier then multiplies the selector output voltage by a factor of two to generate the residue for the next stage. The subsequent section describes how these individual blocks are developed at the circuit level using Carbon Nanotube FET.

3. DEVELOPMENT OF BLOCKS

3.1 FOLDED CASCODE OPERATIONAL AMPLIFIER

To have a comparator with a fast and accurate response, for accurate analog voltage subtraction and for linear voltage amplification, it seemed necessary to design an Operational Amplifier. The folded cascode topology seemed to be most attractive because it offers advantages such as self-compensation, good input common mode range, gain of two stage Op Amp and improved CMRR and PSRR over push-pull configuration. The Fig.3 shows the implementation of folded cascode Op Amp at the circuit level using CNFETs.

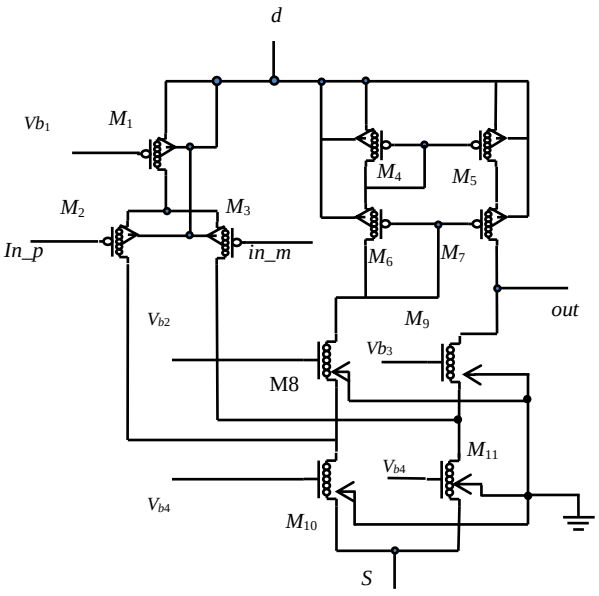


Fig.3. Circuit of Folded Cascode OpAmp with CNFET

The CNFET model used is described in [6-7] which is compatible with Hspice. The threshold voltage V_{th} of the CNFET is related to the diameter of the nanotube by the following formula,

$$V_t = \frac{E_g}{2e} = \frac{\sqrt{3}aV_\pi}{3eD_{CNT}} = \frac{0.43}{D_{CNT}}nm \quad (2)$$

where, V_π(3.033eV) is the carbon π-π bond energy in the tight bonding model and e is the unit electron charge (1.6×10^{-19}C). The CNFET Hspice model allows the change in the diameter by varying the chirality parameters m, n according to the following formula,

$$D_{CNT} = \frac{\sqrt{3}a_{c-c}\sqrt{m^2+mn+n^2}}{\pi} \quad (3)$$

where, $a_{c\text{-}c}$ = 2.49A^0 is lattice constant. The number of nanotubes in one CNFET can be increased to increase the current capacity of the CNFET. It is assumed that the technology supports usage of different diameters of nanotubes of CNFET so carbon nanotube diameter can be used as a design variable. Following design steps were followed while designing the OpAmp:

- Choice of CNFET diameter and number of tubes in the output stage is based on slew rate desired and load driving capacity. Slew rate required is 1.8V/10picoseconds. Load to be driven is 1 femto farad. Hence output current capacity of OpAmp is 200μA. Hence output stage CNFETs [M4 to M11] have 2 nanometer diameter and 5 tubes.
- Hence M4 to M11 have threshold voltages V_{th} = 0.403/2 = 0.2V. All transistors must be in saturation for OPAMP to work properly. Transistors are biased such that they are in the middle of saturation region. Accordingly the bias voltages V_{b1} and V_{b2} are chosen.
- $+V_{sup}$ and $-V_{sup}$ is to be chosen such that $+V_{maxout}$ = 0.9V and V_{minout} = -0.9V. CNFETs in output stages drop 0.25V across them in saturation and hence $+V_{sup}$ = 1.4V and $-V_{sup}$ = -1.4V.

Input stage differential amplifier bias transistor M_1 must provide current that is less than one third of that of the output current mirror current. Hence it is chosen with Diameter 1.5nm and 2 tubes.

Table.1. Parameters of CNFETs

Parameter	Description	Value
L_{ch}	Physical Channel Length	32nm
L_{geff}	Mean free path in the intrinsic CNT channel	100nm
L_{ss}, L_{dd}	Length of doped source, drain side extension region	32nm
K_{gate}	The dielectric constant of the high-k top gate dielectric material	16
T_{ox}	Gate oxide material thickness	4nm
C_{sub}	Coupling capacitance between channel region and substrate	20pF/m

The CNFETs used in the Op Amp circuit have the parameters given in Table.1. The non-ideality parameters of the designed Op Amp are given in Table.2 and the frequency response for various capacitive loads is given in Fig.4.

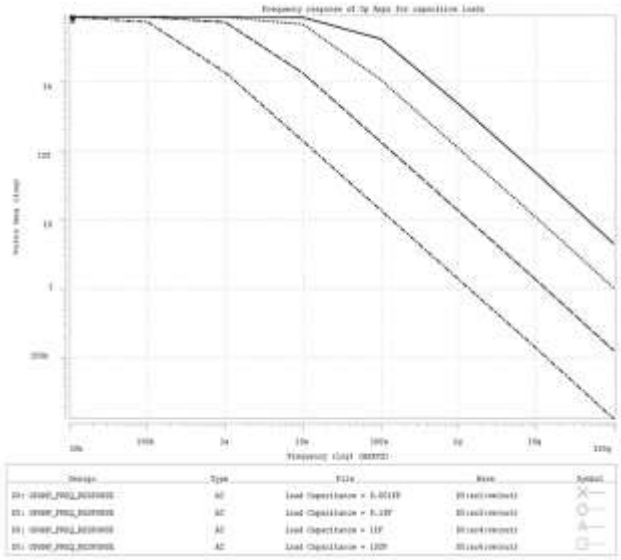


Fig.4. Frequency Response of OpAmp for capacitive loads

This Op Amp is used as the basic building block in the development of comparator, Subtractor and voltage amplifier of gain of two.

Table.2. Op Amp Non-Idealities

Non-Ideality Parameter	Value
Offset Voltage (V_{off})	4.002nV
Bias Current (I_{B+})	15nA
Bias Current (I_{B-})	17nA
DC Gain	~ 20K
Unity Gain Frequency (F_T)	~ 10GHz
Input Impedance (R_{in})	~ 10 Tera Ω
Output Impedance (R_{out})	~20Ω
Common Mode Rejection Ratio	100dB
Power Supply Rejection Ratio	130dB

3.2 COMPARATOR

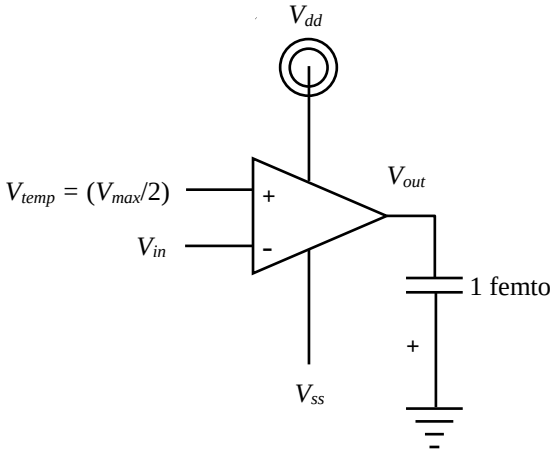


Fig.5. Comparator

The folded cascode Op-Amp is used in open loop configuration to act as the comparator shown in Fig.5. The inverting input is given the voltage of (V_{max}/2) which is compared with the voltage at the non-inverting input terminal and the output voltage V_{out} is decided by,

$$V_{out} = V_{dd} \text{ if } V_{in} > (V_{max}/2)$$
$$V_{out} = V_{ss} \text{ if } V_{in} < (V_{max}/2) \quad (4)$$

The Fig.6 shows the transfer curve of the comparator. The inverting terminal is given the voltage of 0.55V and the input of the non-inverting terminal is varied from 0 to 1V.

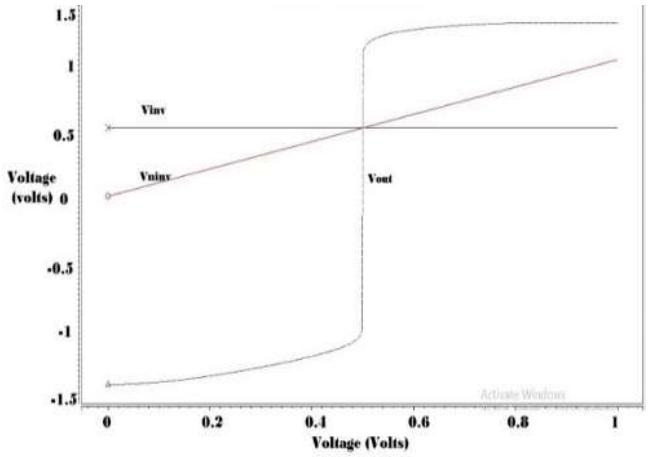


Fig. 6 Comparator transfer curve

3.3 SUBTRACTOR

The folded cascode Op Amp used in negative feedback configuration is used as shown in the Fig.7 to function as a subtractor. The values of resistances are chosen such that the output voltage is related to the input voltage with the equation,

$$V_{out} = V_{in\_1} - V_{in\_2} \quad (5)$$

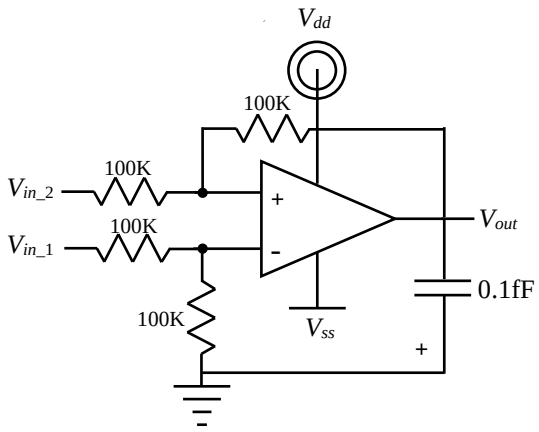


Fig.7. Subtractor

The Fig.8 shows the transient response of the subtractor for a 5GHz square wave with a 4ps rise time and 50% duty cycle and a 5GHz sine wave with a full scale amplitude. It can be seen that the settling time of the subtractor is 10ps for 5% of the final value.

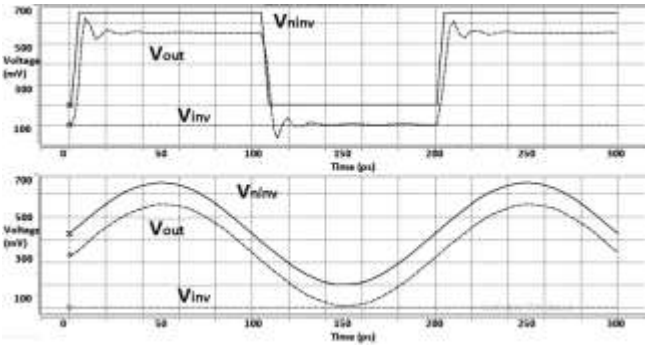


Fig.8. Transient response for subtractor

3.4 VOLTAGE AMPLIFIER OF GAIN TWO

The Fig.9 shows folded cascode amplifier used in negative feedback configuration to perform the voltage amplification of gain of two. The resistances are chosen such that output voltage and input voltage are related with following equation:

$$V_{out} = 2V_{inplus} \quad (6)$$

The Fig.10 shows the transient response for the voltage amplifier for a full scale square wave of 5GHz frequency with 50% duty cycle and 4ps rise time and for a sine wave of 5GHz frequency and full scale amplitude. It can be seen that the 5% settling time for the amplifier is around 10ps.

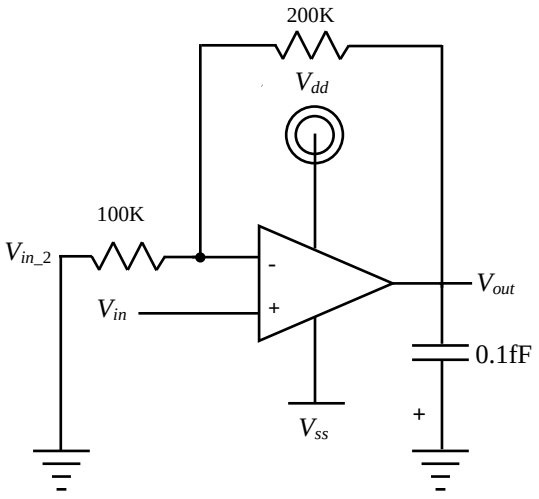


Fig.9. Voltage amplifier of gain of two

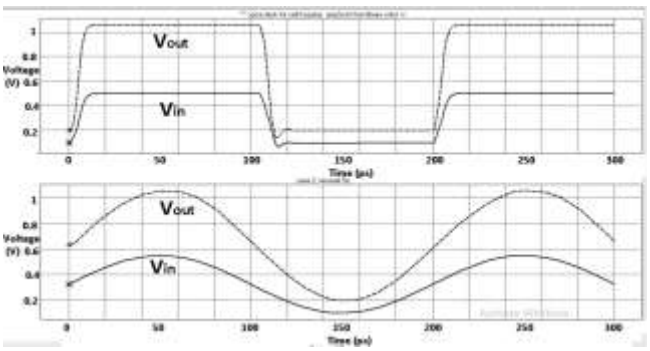


Fig.10. Transient response for amplifier

3.5 SELECTOR

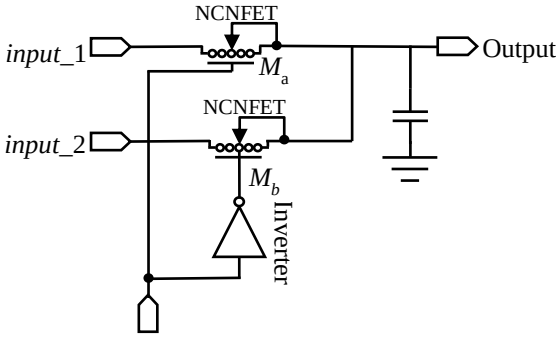


Fig.11. Selector

The selector circuit diagram is as shown in Fig.11. Depending upon the voltage at the '*Sel*' terminal, the signal *input*_1 or *input*_2 is chosen. The NCNFETs chosen are having nanotube diameter 1.5nm and 2 tubes each. A very negligible voltage appears across them so they work as ideal switches.

Table.4. Selector logic

Sel	***Ma***	***Mb***	***Vout***
Low	Off	On	V_{Input_1}
High	On	Off	V_{Input_2}

The Inverter which is used in the selector is constructed with CNFETs of two nanotubes each of diameter 1.5nm and its circuit is shown in Fig.12.

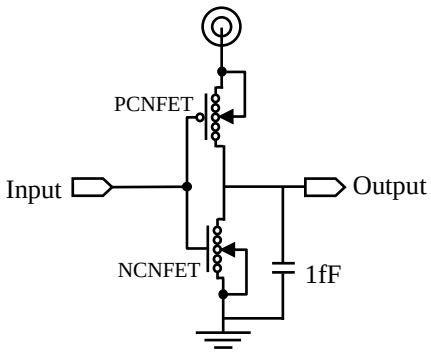


Fig.12. Inverter Circuit Diagram

3.6 POSITIVE EDGE TRIGGERED D FLIP/FLOP

The circuit diagram of positive edge triggered D flip/flop is shown in the Fig.13 [9]. The power, delay and PDP characteristics are given in Table.5 for the clock rate of 10GHz. This flip/flop is to be used in reading the comparator output.

Table.5. Power, delay and PDP for edge triggered D flip/flop

	Unloaded	***Cload* = 0.5fF**	***Cload* = 1fF**
Delay (pS)	3.38	8.791	13.406
Power (uW)	2.36	6.52	10.559
PDP (aJ)	7.8	57.352	141.553

The NAND gates are constructed using CNFETs with 2 nanotubes each of diameter 1.5nm. Their circuit description is shown in Fig.14.

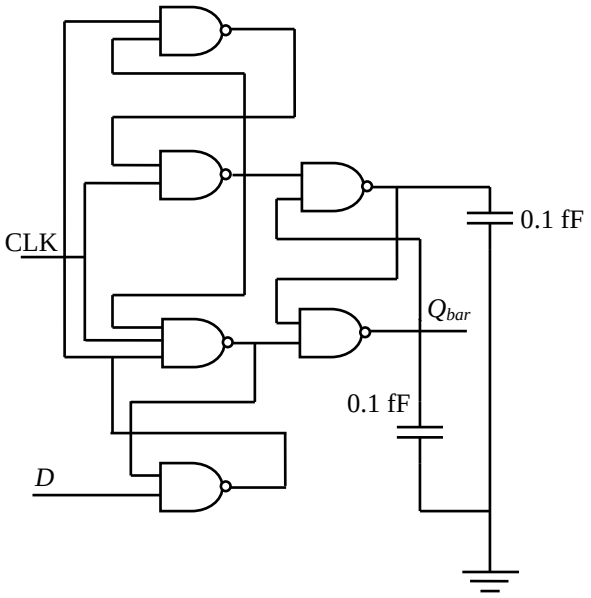


Fig.13. Circuit diagram and symbol of Positive Edge triggered D flip/flop

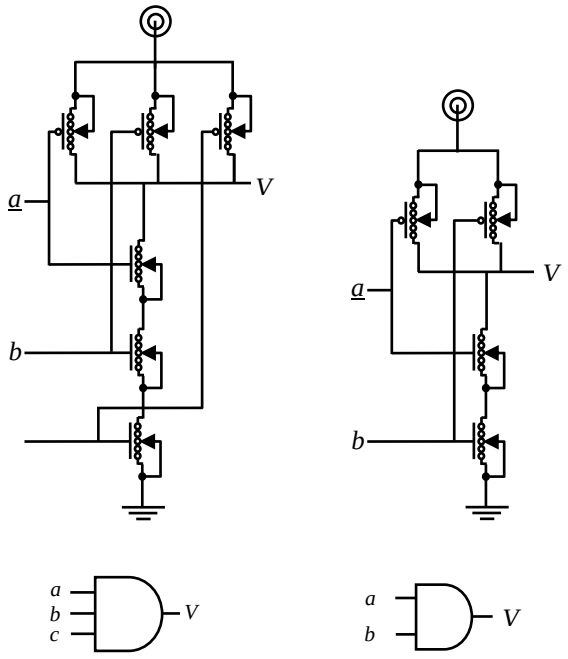


Fig.14. Three and two input NAND gates with CNFET

3.7 DOUBLE EDGE TRIGGERED D FLIP/FLOP

The circuit diagram of D flip/flop triggering on both the rising and falling edge (DET flip/flip) of the clock is shown in the Fig.15 [10]. This flip/flop is used for reading comparator outputs at the LSB transitions which results in reduction of Differential Non-linearity and Integral Non-linearity. The power, delay and PDP characteristics are given in Table.6 for the clock rate of 10GHz.

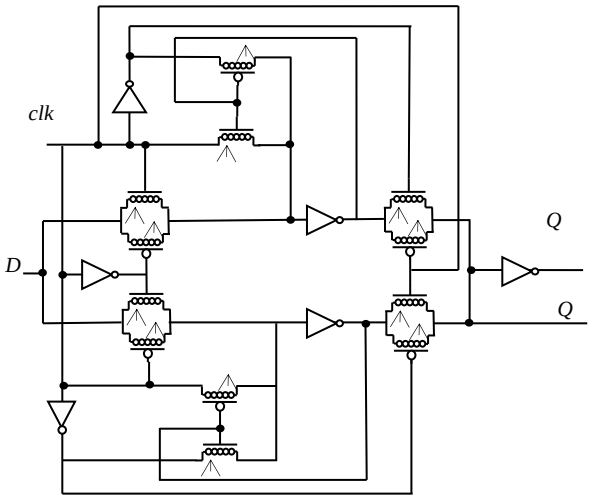
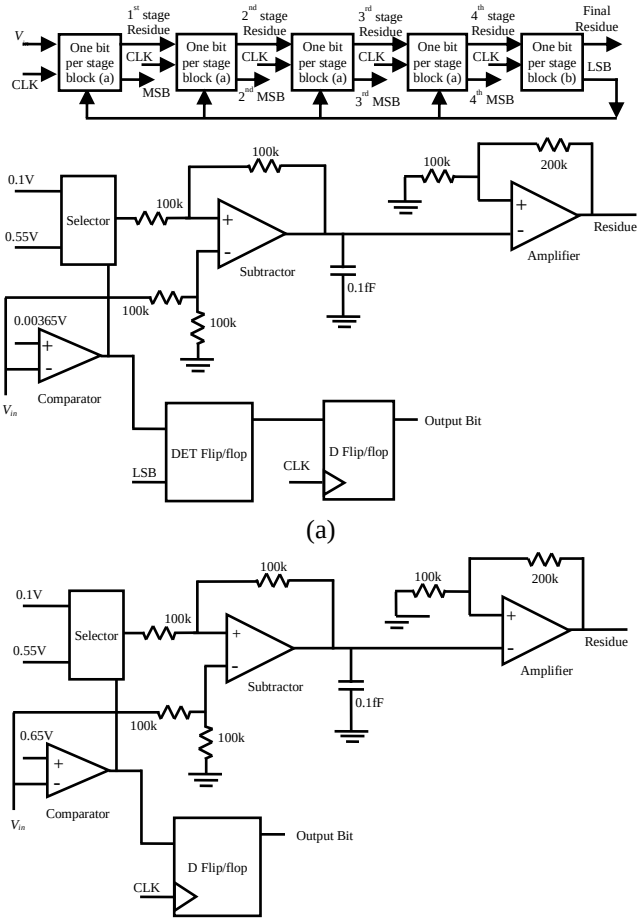


Fig.15. Circuit diagram and symbol of DET f/f

Table.6. Power, Delay and PDP for DET f/f

	Unloaded	**C_{load} = 0.5fF**	**C_{load} = 1fF**
Delay (pS)	2.016	18.37	33.37
Power (uW)	26.677	30.04	32.89
PDP (aJ)	53.78	551.834	1097.53



(a)

(b)

Fig.16. Five Bit ADC diagram

3.8 FIVE BIT ADC WITH ONE-BIT-PER-STAGE BLOCK

The Fig.16 shows the five bit ADC diagram with one-block-per-stage circuit for the stages.

- The range of analog input is selected to be 0.2V to 1.1V because the subtractor and the amplifier are most linear in this range. The first four stages are designed as shown in Fig.16.(a) with a DET flip/flop sensitive to the LSB transition sampling the decision of the comparator. The last stage which gives the decision of the LSB is built as shown in Fig.16(b) with the difference being no DET flip/flop present after comparator.
- Position of selector is shifted before the subtractor. Now subtractor output is:

$$V_{sub} = V_{in} - 0.1\text{V if } Sel = 0$$
$$V_{sub} = V_{in} - 0.55\text{V if } Sel = 1 \quad (7)$$

- The comparator threshold voltage now changed to 0.45V to 0.65V because $V_{max}/2 = 0.65$V after addition of offset. Hence the comparator output is related to input voltage as:

$$V_{out} = V_{dd} \text{ if } V_{in} > 0.65\text{V}$$
$$V_{out} = V_{ss} \text{ if } V_{in} < 0.65\text{V} \quad (8)$$

- The DET flip/flop is not used in the last stage which gives the LSB. For all the other stages i.e. one to four, the DET block is used with D input being the input from the comparator output voltage and clock input being the LSB output coming from last stage. Hence the comparator output is sampled at every transition of the LSB to synchronize the transitions with the LSB. This ensures a reduction in DNL and INL.

Next section describes the static and dynamic performance parameters along with average power consumption and figure of merit for the five bit ADC.

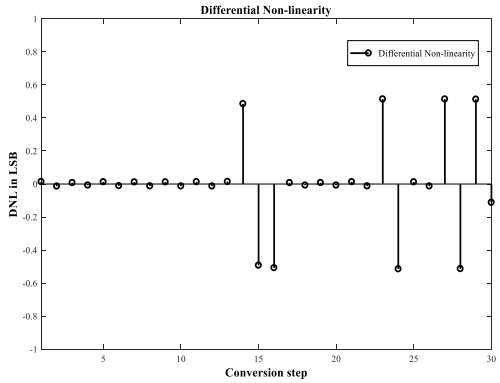
4. PERFORMANCE PARAMETERS

The static and dynamic performance of the ADC was analyzed with the help of Hspice simulations. The results are described in this section.

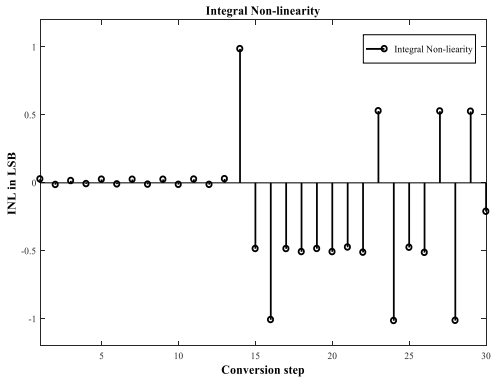
4.1 STATIC PERFORMANCE

To find the static performance parameters such as offset error, gain error, differential non-linearity (DNL) and integral non-linearity (INL), the 5 bit ADC was given a slow varying ramp input covering the full analog input voltage range of 0.2V to 1.1V.

The offset error was found out to be 0.2V and it was duly corrected. The gain error found was very negligibly small. The DNL and INL were calculated after offset correction. The DNL lied within +0.5LSB to -0.5LSB and the INL is within +1LSB to -1LSB as shown in the Fig.17.



(a)



(b)

Fig.17 (a) DNL and (b) INL

4.2 DYNAMIC ANALYSIS

The 5 bit ADC was given sinusoidal input of frequency 2GHz (oversampling) to 5GHz (Nyquist frequency) with an interval of 0.25GHz and the transient simulation was carried out in Hspice. The digital data obtained from Hspice was read in MATLAB and given to an ideal DAC to obtain back the analog input. The output thus obtained by the ideal DAC was filtered with the pass-band of 2 to 5GHz and the Signal-to-Distortion Noise (SND) ratio and Spurious-Free Dynamic Range (SFDR) is obtained. SFDR is slightly on the lesser side i.e. above 11dBc because of the harmonics generated due to not using sample-and-hold between stages of the pipeline and the average SND is ~30dB. It is shown in Fig.18.

Effective number of bits (ENOB) is calculated using formula:

$$ENOB(bits) = \frac{SNR - 1.76}{6.02} dB \quad (9)$$

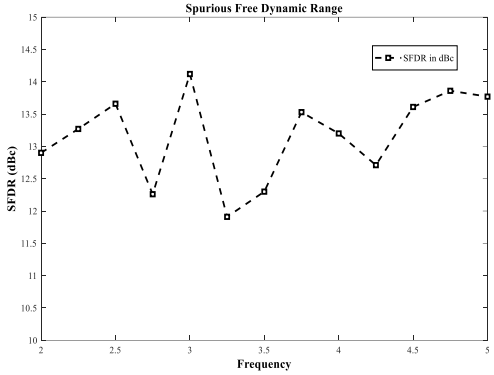
This gives average ENOB as 4.69 in the 2 to 5GHz band.

4.3 AVERAGE POWER AND FIGURE OF MERIT

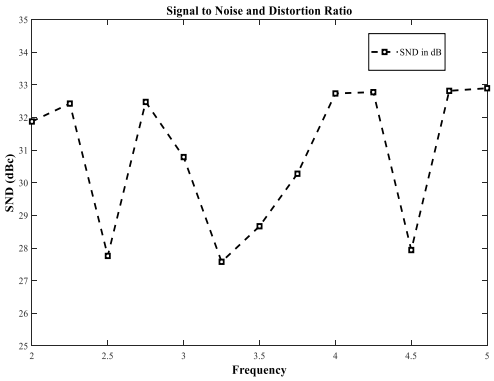
The average power consumed by the ADC is found to be 5.031mW. The Effective Resolution Bandwidth (ERBW) is 3GHz i.e. in the 2 to 5GHz band the ENOB is guaranteed to be above 4.6. The FoM is calculated using formula:

$$FoM = \frac{Power}{2^{ENOB} \min(f_s, 2ERBW)} \quad (10)$$

The FoM thus calculated is 25.38fJ/conversion step.



(a)



(b)

Fig.18 (a) SFDR (b) SND in the band of 2 to 5GHz

Table.7 Comparison of Various ADCs

	Proposed	**Xu et al. [2]**	**Chen et al. [3]**	**Oh et al. [4]**
Resolution (bits)	5	4	6	6
Technology	32nm CNFET	65nm CMOS	45nm CMOS	65nm CMOS
Architecture	Pipeline	Flash	Pipeline	Flash
Sampling rate (GSPS)	10	10	4	10
Power (mW)	5.032	104	38	63
ENOB (bits)	4.69	3.84	5.02	4.51
FoM (fJ/step)	25.38	790	570	277

5. DISCUSSION AND CONCLUSION

This work presented the design and simulation results of a 5 bit pipelined ADC with ENOB 4.69 working at 10 GSPS with average power consumption of 5.031mW. The drastic decrease seen in power consumption is due to the fact that CNFET requires 6 times less current than the CMOS counterparts for its working. Although it is generally advised to use sample and hold with a pipelined architecture, the ENOB performance without the use of sample-and-hold is still above 4.5 even at the Nyquist frequency. Because the sample and hold is not used between stages, there is additional harmonics generated which result in reducing the SFDR performance but the SFDR is still above 11dBc which can make the detection of the tone possible. The Table.7 compares this work with some state-of-the-art works. As the CNFET technology is very new and still in its early stages of developments, there is no foundry which commercially manufactures CNFET ICs on a large scale and hence the foundry files for layout and post-layout simulation are yet to be made available by them. Hence the layout and post layout simulation of the ADC circuit is not done but it can be carried out in near future when foundry files become available. With the ERBW of 3GHz from 2 to 5GHz, this can be very effectively utilized for high speed communication applications in the ISM band with very low power consumption in the ADC.

REFERENCES

[1] Shuang Zhu, Benwei Xu, Bo Wu, Kiran Soppimath and Yun Chiu, "A 0.073-mm^2 10-GS/s 6-Bit Time-Domain Folding ADC in 65-nm CMOS with Inherent DEM", *Proceedings IEEE Custom Integrated Circuits* Conference, pp. 1-4, 2015.

[2] Yongsheng Xu, Leonid Belostotski and James W. Haslett, "A 65-nm CMOS 10-GS/s 4-bit Background-Calibrated Noninterleaved Flash ADC for Radio Astronomy", *IEEE Transactions on Very Large Scale Integration Systems*, Vol. 22, No. 11, pp. 2316-2325, 2014.

[3] M.W. Chen, L.R. Carley and D.S. Ricketts, "A Process-Technology-Scaling-Tolerant Pipelined ADC Architecture Achieving 6-Bit and 4GS/s ADC in 45nm CMOS", *Proceedings of IEEE 14th Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems*, pp. 16-18, 2014.

[4] Dong-Ryeol Oh, Jong-In Kim, Min-Jae Seo, Jin-Gwang Kim and Seung-Tak Ryu, "A 6-bit 10-GS/s 63-mW 4xTI Time-Domain Interpolating Flash ADC in 65-nm CMOS", *Proceedings of 41st European Solid-State Circuits Conference*, pp. 323-326, 2015.

[5] Matt Straayer et al., "27.5 A 4GS/s Time-Interleaved RF ADC in 65nm CMOS with 4GHz Input Bandwidth", *Proceedings of IEEE International Solid-State Circuits Conference*, pp. 464-465, 2016.

[6] J. Deng and H.S. Philip Wong, "A Compact SPICE Model for Carbon-Nanotube Field-Effect Transistors Including Nonidealities and Its Application-Part I: Model of the Intrinsic Channel Region", *IEEE Transactions on Electron Devices*, Vol. 54, No. 12, pp. 3186-3194, 2007.

[7] J. Deng and H.S. Philip Wong, "A Compact SPICE Model for Carbon-Nanotube Field-Effect Transistors Including Nonidealities and Its Application-Part II: Full Device Model and Circuit Performance Benchmarking", *IEEE Transactions on Electron Devices*, Vol. 54, No. 12, pp. 3195-3205, 2007.

[8] P.A. Gowri Sankar and G. Sathiyabama, "A Novel CNFET Technology Based 3 Bit Flash ADC for Low-Voltage High Speed SoC Application", *International Journal of Engineering Research in Africa*, Vol. 19, pp. 19-36, 2016.

[9] P.E. Allen and Douglas R. Holberg, "*CMOS Analog Circuit Design*", 2nd Edition, Oxford University Press, 2002.

[10] R. Jacob Baker, "*CMOS Circuit Design Layout and Simulation*", Wiley IEEE Press, 1998.