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DESIGN AND SIMULATION OF CURRENT FEEDBACK OPERATIONAL AMPLIFIER IN 180nm AND 90nm CMOS PROCESSES

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Abstract

This paper proposes a Current Feedback Operational Trans-conductance Amplifier (CFB OTA) with a folded cascode op-amp as input stage cascaded with class AB buffer as output stage. This gives better results on parameters such as bandwidth, slew rate, settling time and input offset voltage compared to the conventional CFOA. Hence it carries significance in high frequency applications such as A/D converters and active filters where CMOS CFOA used as an active building block. CADENCE simulation results are obtained using 180nm CMOS process (supply voltage of ±2.5V, 100μA biasing current) and 90nm CMOS process (supply voltage of ±1.2V, 50μA biasing current). Some of the performance parameters obtained are DC gain of 60.2dB, open-loop gain bandwidth product(GBW) of 307 MHz, slew rate (SR+) of +30V/μS to +90V/μS and DC input offset voltage of −0.6nV.

Keywords:

CFOA, Class AB Buffer, Extended Bandwidth

1. INTRODUCTION

Design of analog circuit plays a pivotal role [1] in mixed signal applications, since interfacing digital systems to the analog counterpart in real time applications poses many tangible problems in terms of gain, bandwidth and noise figure. This is true in major application areas like industrial processes, signal conditioning, telecommunication and biomedical measurements. In analog systems, design and implementing analog filters carry significance, particularly in signal processing applications. In analog filters, which are active filters where operational amplifiers form the active element, design criteria are too critical for varying requirements and linearity plays a pivotal role in design [2]. The high gain amplifiers, as operational amplifiers are commonly attributed, it offers good bandwidth at the cost of temperature performance, power dissipation etc. A topology employing CFA-OTA as input stage cascaded with class AB cross coupled buffer as output stage in .35 μm is discussed in paper [1]. A Ka band linear power amplifier is implemented in 28 nm bulk technology in paper [2]. Also another CMOS CFOA design with 100 MHz bandwidth is presented in paper [11]. The paper given in [14] discusses the theoretical background of the current feedback operational transconductance amplifier

In high frequency and high speed applications, current mode op-amps are frequently used for better performance. One such op-amp is Current Feedback Operational trans-conductance Amplifier (CFOA) which is a four terminal device. The main advantage of the CFOA is that it can be easily designed from current op-amps, simply by using a circuit node which is normally connected to analog ground as an additional voltage input, without using additional transistors or stages. However, conventional CMOS CFOA design is still facing some challenges, such as fixed bandwidth, input offset voltage, noise, power consumption and circuit complexity [3-11].

The CFOAs are classified based on four terminal theory instead of conventional op-amps in two port theory [12-13] and so also it could be divided into more types unlike the classification based on two port theory [14], out of which the one of interest is CF-OTA with a voltage buffer. The main advantage of the current feedback OTA is that it can be easily designed from the design of current op-amps, simply by using a circuit node which is normally connected to analog ground as an additional voltage input, without using additional transistor stages. Improvising parameters like bandwidth, slew rate, settling time, input offset voltage and input impedance of CF-OTA has drawn wide attention from researchers. Here we report the design of a CFOA with better performance in terms of gain, bandwidth, slew rate and settling time in 180nm and 90nm. Also a comparison of performance is made between amplifiers with class AB output stage and source follower output stage.

The rest of the paper is organized as follows: Section 2 illustrates the circuit description and CMOS realization of the proposed CFOA. Section 3 discusses simulation results in two configuration with 90nm and 180nm technology. Finally concluding points are described in section 4.

2. METHODOLOGY

In four terminal theory, two input and output terminals of op-amp are not seen as one port, but it can be seen as four independent terminals that can have different impedance levels. CFOA is a hybrid input current output op-amp and the main advantage of designing CFOA is that it can be easily converted from current op-amps. The current op-amp has normally input stage with only one input and a current output stage. The current input stage of current op-amp is only a current buffer that transfers the input current to the high-impedance node. Converting current input stage into a hybrid input stage implies providing an additional voltage input through which the voltage at the current input can be set. The current output stage converts the voltage at high impedance node into two balanced currents.

2.1 PROPOSED CMOS CFOA

In this paper we present a CMOS Current Feedback Operational Amplifier (CFOA) with better bandwidth. In this approach folded cascode op-amp is used as input stage which is shown in Fig.1 and a preceding voltage buffer is implemented by using class AB buffer as shown in Fig.2(b). This output stage circuit helps to improve the current drive capability. The use of class AB buffer helps to decrease the output impedance

drastically. Also in this paper an observation is done by replacing the output stage with source follower circuit as in Fig.2(a) and it is found that only the slew rate is improved. The design parameters such as bias currents and the gate dimensions are given in Table.1.

The design of input stage starts by designing the folded cascode OTA using gm/Id technique in strong inversion region [15-16].

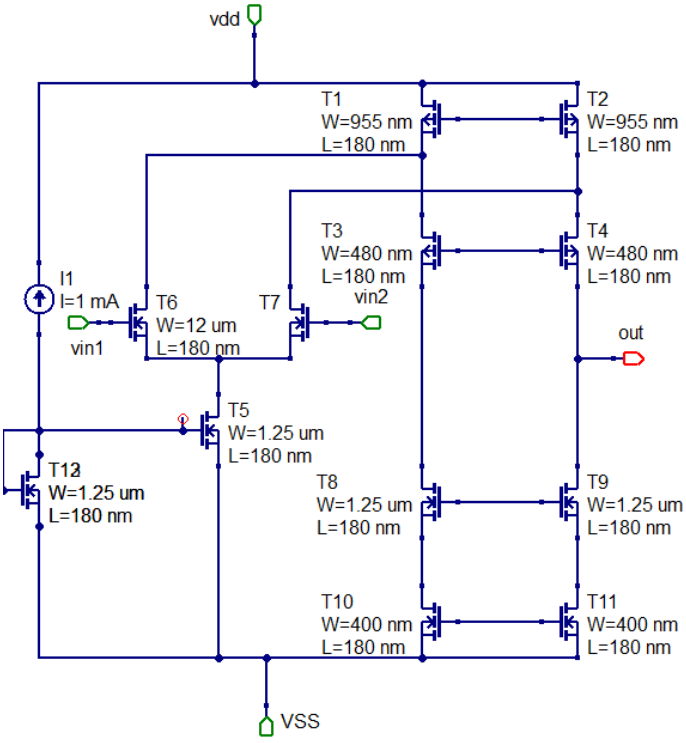
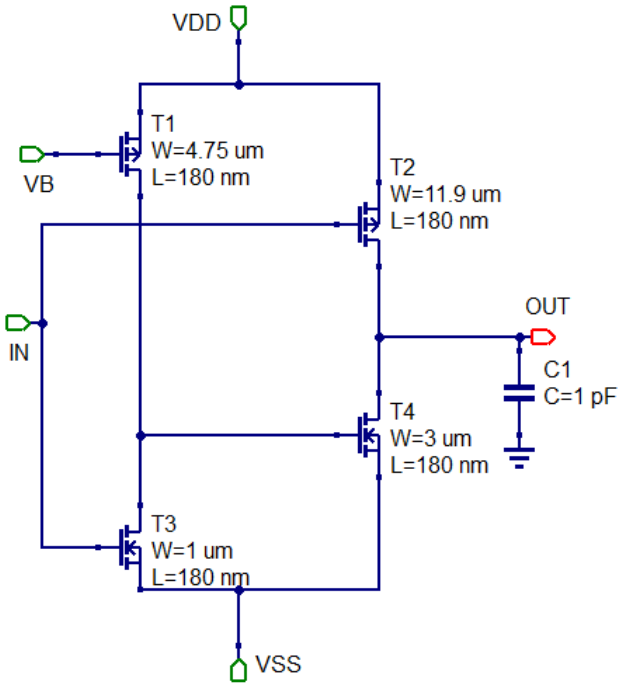
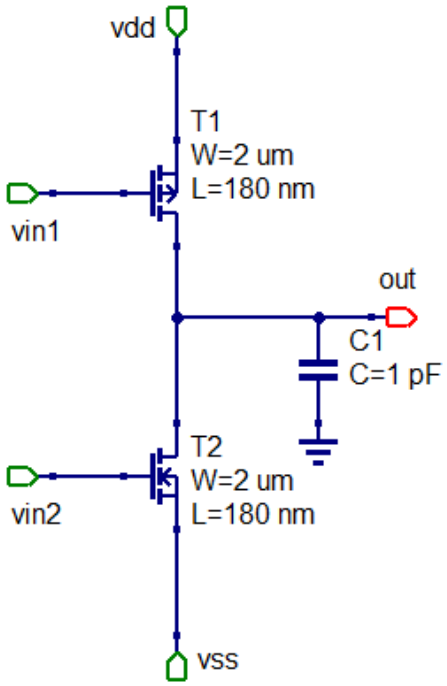


Fig.1. Schematic of CMOS CFOA input stage



(a) Source follower output



(b) Class AB output buffer

Fig.2. Schematic of CMOS CFOA output stages

In the G_m/I_d technique, the bias current strongly depends on transconductance of the OTA by the Eq.(1)

$$g_m = \frac{\{V_{in}(+) - V_{in}(-)\}}{I_d} \tag{1}$$

The folded cascod op-amps helps to achieve higher DC gain at the initial stage. The *GBW* of OTA is given by the Eq.(2)

$$GBW = \frac{g_m}{C_l} \tag{2}$$

The gate dimensions of the transistors M_1 and M_2 are related to the *GBW* of the OTA and it is given by the Eq.(3)

$$\left(\frac{W}{L}\right)_1 = \left(\frac{W}{L}\right)_2 = \frac{g_{m1}^2}{\mu_n Cox I_d} = \frac{GBW^2 C_l^2}{\mu_n Cox I_d} \tag{3}$$

where, g_m is the transconductance of the differential pair transistor, C_l is the load capacitance and $\mu_n\ Cox$ is the parameter which depends on the material constant.The current Id is related to the slew rate and load capacitance by the Eq.(4)

$$I_d = SR \times C_l \tag{4}$$

The bias currents in cascode is choosen such that 1.2 to 1.5 times greater than the I_d to avoid zero current in cascodes. The gate dimensions of the transistors M_4 to M_7 are related to the maximum output voltage of the OTA by the Eq.(5) and Eq.(6)

$$\left(\frac{W}{L}\right)_4 = \left(\frac{W}{L}\right)_5 = \frac{2I_5}{\mu_p Cox V_{DS5}^2} \tag{5}$$

$$\left(\frac{W}{L}\right)_6 = \left(\frac{W}{L}\right)_7 = \frac{2I_7}{\mu_p Cox V_{DS7}^2} \tag{6}$$

The gate dimensions of the transistors M_8 to M_{11} are related to the minimum output voltage of the OTA by the Eq.(7) and Eq.(8)

$$\left(\frac{W}{L}\right)_8 = \left(\frac{W}{L}\right)_9 = \frac{2I_9}{\mu_p Cox V_{DS9}^2} \quad (7)$$

$$\left(\frac{W}{L}\right)_{10} = \left(\frac{W}{L}\right)_{11} = \frac{2I_{11}}{\mu_p Cox V_{DS11}^2} \quad (8)$$

The minimum and maximum input common mode is set by Eq.(9) and Eq.(10)

$$\left(\frac{W}{L}\right)_3 = \frac{2I_3}{\mu_n Cox\left(V_{in_{\min}} - V_{ss} - \sqrt{\left(\frac{I_3}{\mu_n Cox}\right)} - V_t\right)^2} \quad (9)$$

$$\left(\frac{W}{L}\right)_4 = \frac{2I_3}{\mu_p Cox\left(V_{dd} - V_{in_{\max}} + V_t\right)^2} \quad (10)$$

Table.1. Gate dimensions and biasing currents in proposed CMOS CFOA

Transistors	Gate dimensions and biasing currents			
	L = 180nm		L = 90nm	
	Width	Current (μA)	Width	Current (μA)
M_1, M_2	12μm	50	30μm	25
M_3	1.25μm	100	500nm	50
M_{12}	1.25μm	100	690nm	50
M_4, M_5	955nm	100	445nm	50
M_6,M_7	480nm	50	300nm	25
M_8, M_9	1.25μm	50	1.75μm	25
M_{10}, M_{11}	400nm	50	1.75μm	25

3. RESULTS AND DISCUSSIONS

CFOA having high bandwidth with very low input offset voltage, low settling time, higher unity gain bandwidth product, -3dB bandwidth and improved slew rate is proposed in this paper. Simulation was carried out in 3 different ways.

- CFOA with class AB output buffer stage in 180nm technology
- CFOA with source follower output buffer stage in 180nm technology
- CFOA with class AB output buffer stage in 90nm technology (50μA)

From the simulation of CFOAs in 180nm CMOS process, excellent frequency responses in hundreds of MHz are obtained. The simulation of CFOA with class AB buffer gives DC gain of 61dB with a unity gain bandwidth of 714MHz is shown in Fig.3. The simulation of CFOA with source follower gives DC gain of 59.48dB with a unity gain bandwidth of 626MHz as shown in Fig.4. The existing feature of the CFOA with class AB buffer is that one can change the gain independent of the bandwidth (or shows less dependency).

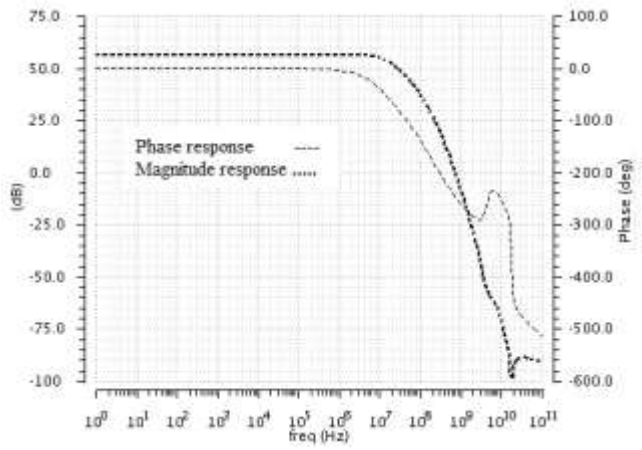


Fig.3. Open-loop frequency response of the proposed CMOS CFOA with class AB buffer

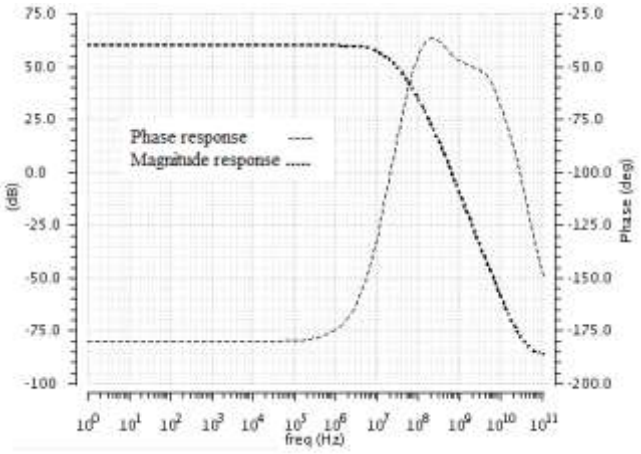


Fig.4. Open-loop frequency response of the proposed CMOS CFOA with source follower

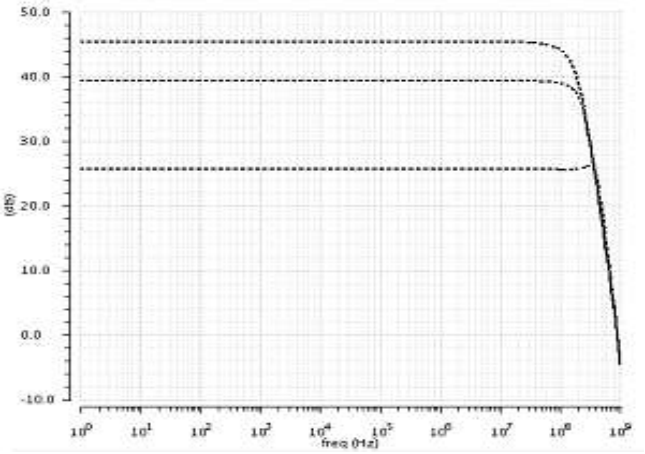


Fig.5. Closed-loop frequency response of the CFOA with class AB buffer for different gains

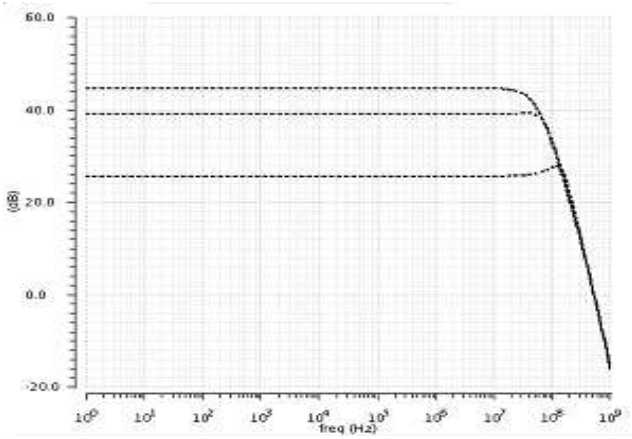


Fig.6. Closed-loop frequency response of the proposed CMOS CFOA with source follower for different gains

Table.2. Comparison between different configurations

Parameters	180nm		90nm
	CFOA (Class AB)	CFOA (Source follower)	CFOA (Class AB)
Supply V	2.5V	2.5V	1.2V
I bias	100μA	100μA	50μA
Bandwidth (MHz)	80.97	59.48	230
GBW in MHz	714	626	910
Settling time	40ns	80ns	70ns
Slew rate	30V/μs	110V/μs	90V/μs
Input V Range	-1 to 1	-1 to 1	-.8 to .9
Technology	180nm	180nm	90nm

By simulating the circuit with class AB buffer as the output stage, an improved closed loop response is obtained as in Fig.5. Then observed the simulated closed loop response obtained by replacing class AB buffer output stage with source follower as in Fig.6. From the simulation of CFOAs in 90nm CMOS process, a further improved frequency response is obtained. The DC gain of 32.13dB and unity gain bandwidth of 910MHz is obtained as shown in Fig.7. The closed loop response of the same for various gain and 3dB bandwidth is also given in Fig.8.

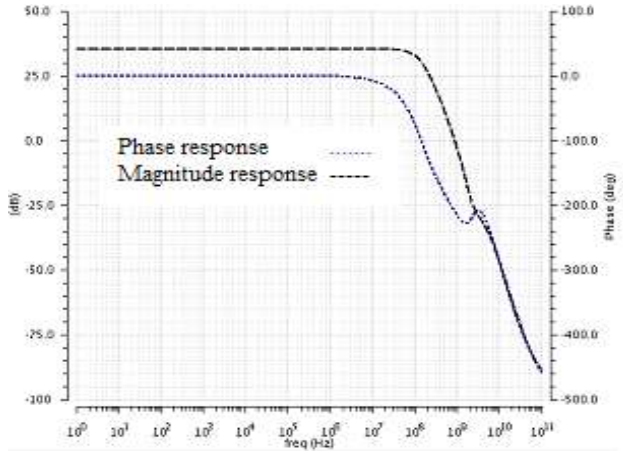


Fig.7. Open-loop frequency response of the proposed CMOS CFOA in 90nm process

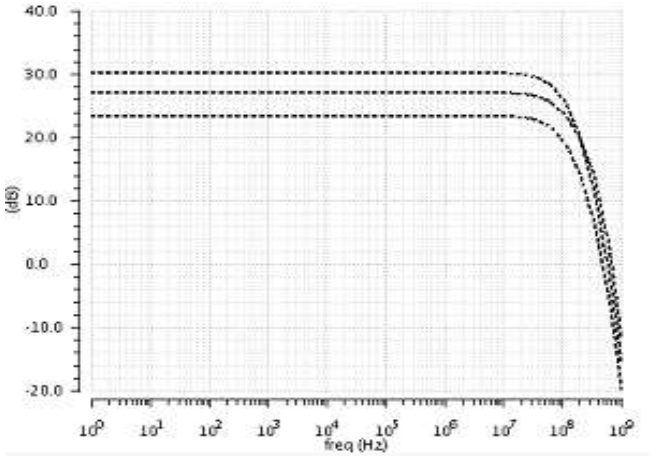


Fig.8. Closed-loop frequency response of the proposed CMOS CFOA with different gains

4. CONCLUSION

A CMOS CFOA having a better bandwidth is obtained and the design of proposed CFOA is carried out in both 90nm and 180nm CMOS process, and the output stages are implemented in Class AB cross coupled amplifier and source follower. The simulation results show improved gain, bandwidth, slew rate and settling time. It is obvious from the results that the CFOA with class AB output stage provides better frequency response and it can be effectively used in active filter design or high speed data converters.

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