

DESIGN OF ADIABATIC LOGIC BASED COMPARATOR FOR LOW POWER AND HIGH SPEED APPLICATIONS

T.S. Arun Samuel¹, S. Darwin² and N. Arumugam³

^{1,3}Department of Electronics and Communication Engineering, National Engineering College, Kovilpatti, India
²Department of Electronics and Communication Engineering, Dr. Sivanthi Aditanar College of Engineering, India

Abstract

This paper presents a novel modified comparator based on the combination of 2N-2N2P adiabatic logic and two phase adiabatic static clocked logic (2N-2N2P and 2PASCL), combination of efficient charge recovery adiabatic logic and two phase adiabatic static clocked logic (ECRL and 2PASCL). This new structure computes a decision making signal faster than the existing methods. The introduced logic based comparator demonstrates that the usage of high speed decision making signal allows high speed comparator, saving 60-80% of power in comparison with existing renowned conventional comparators. Adiabatic logic based circuit carry out less power consumption by constraining current flowing through devices with less voltage drop and by reusing the energy stored at output node instead of discharging it to ground. The design is simulated using Cadence Virtuoso Environment.

Keywords:

Adiabatic Logic, ECRL, 2PASCL, 2N-2N2P, Comparator

1. INTRODUCTION

Apart from operational amplifiers, comparators are most probably second most widely used electronic components in this world. Comparators are referred to as 1-bit analog-to-digital converter which is widely used in ADC circuitry. The speed of comparator is limited by the decision making time of the comparator [15]. The energy efficiency has become a critical concern in low power circuit design. Several techniques like voltage scaling, dynamic frequency scaling have been introduced to reduce a power consumption among which adiabatic logic become attractive solution. For low power applications, the comparator is designed based on the following block diagram [3].

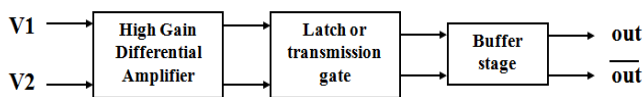


Fig.1. Functional block diagram for comparator

Decision making unit (latch) is used to ensure a correct transition from one logic state to another logic state. In this design a single stage differential amplifier is used. To improve the gain further, differential amplifier circuits can be cascaded with one or more stages. In certain design approach, the buffer stage is followed by a latch stage to handle large capacitive loads [7] [8].

This paper mainly focuses on a novel adiabatic logic which is based on the principle of energy recovery. Here the consumed energy is recovered back to the power supply instead of discharging it to ground which resourcefully reduce the overall power consumption [16] [17] [18]. The design helps to evaluate the performance of comparator using different combination of

adiabatic logic styles and their results were compared with the conventional CMOS design.

2. ADIABATIC LOGIC

An adiabatic logic is one that do not release energy when heat increase across the boundary of the device during its operation cycle [4]. The term is derived from thermo dynamic process. Adiabatic logic has several different logic styles which are used to reduce the power consumption of the circuit. Adiabatic logic families is generally categorized into two major groups as diode based and transistor based [9]. The research focus gets more attracted on transistor based adiabatic circuits compared to diode based. Transistor based adiabatic circuits are broadly classified into fully adiabatic logic family and partially adiabatic logic family.

Some of the fully adiabatic logic families are Pass transistor Adiabatic Logic (PAL) and Two Phase Adiabatic Static Clocked Logic (2PASCL). Some of the partially adiabatic logic families are Efficient Charge Recovery Logic (ECRL), Improved Efficient Charge Recovery Logic(IECRL), 2N-2N2P Adiabatic Logic and Positive Feedback Adiabatic Logic (PFAL) [6] [10]. This paper presents combination of 2N-2N2P Adiabatic Logic and Two Phase Adiabatic Static Clocked Logic (2PASCL). The combination is chosen to utilize the advantages of both adiabatic logics.

2.1 EFFICIENT CHARGE RECOVERY LOGIC (ECRL)

Efficient Charge Recovery Logic uses cross-coupled PMOS transistors. It has the structure similar to Cascode Voltage Switch Logic (CVSL) with differential signaling. The circuit uses differential logic, so each gate computes both a logic function and its complement, and each gate requires complimentary inputs [5] [11] [12]. The ECRL consists of two cross-coupled transistors M_1 and M_2 and two NMOS transistors which are shown in Fig.2. An AC power supply (PC) is used for ECRL gate to recover and reuse the supplied energy. Both out and out are generated to the power clock generator which drives a constant load capacitance independent of the input signal [1].

Full output swings is obtained because of the cross-coupled PMOS transistors in both pre-charge and recover phases. Cross-coupled P type MOS transistors in both pre-charge and recover phases has been used to obtain the full output swings. However due to the threshold voltage (V_{th}) of the P type MOS transistors, the circuits agonize from the non-adiabatic loss in the pre-charge and recover phases.

The CRL always pumps charge on the output with a full swing initially, input in is high and input in is low. When, since F is on

power clock (PC) rises from zero to V_{dd} , so output *out* remains ground level. Then, the Output *out* follows the PC as shown in Fig.2.

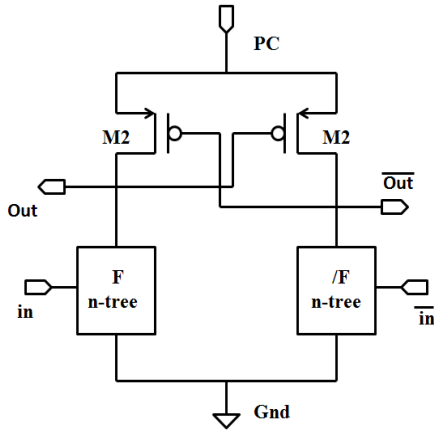


Fig.2. Basic structure of Efficient Charge Recovery Logic

2.2 2N-2N2P ADIABATIC LOGIC

This adiabatic logic family is obtained from Efficient Charge Recovery Logic (ECRL) in order to achieve state retention. A 2N-2N2P family has a similar structure to ECRL and the only difference is that 2N-2N2P has a pair of cross-coupled NMOS transistors in addition to the cross-coupled PMOS transistors in Efficient Charge Recovery Logic. Cross-coupled full inverters has used in 2N-2N2P which is similar to a standard SRAM cell. The key advantage of 2N-2N-2P above ECRL is that the cross-coupled *N* type MOS switches result in non-floating outputs for huge portion of the recovery phase. The basic structure is shown in Fig.3.

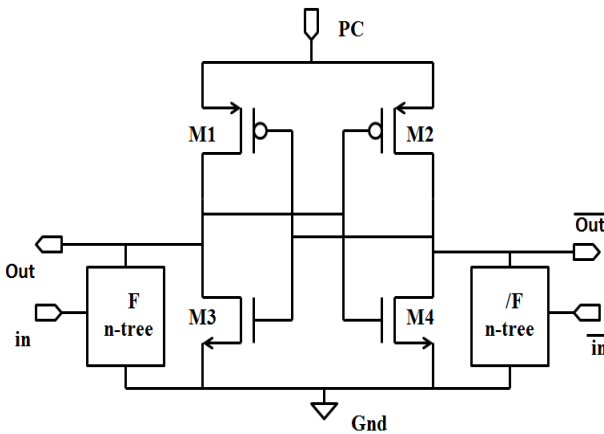


Fig.3. Basic structure of 2N-2N2P adiabatic logic

2.3 TWO PHASE ADIABATIC STATIC CLOCKED LOGIC

The Two Phase Adiabatic Static Clocked Logic (2PASCL) contains two phase clocking split level sinusoidal power supply where one clock is in phase while the other is out of phase. This logic is also referred to as Split Rail Charge Recovery Logic [2]. In its construction, the circuit has two diodes where one diode is placed between the output node and power clock, and another diode connected between one of the terminals of NMOS and power source. The two diodes are used to reuse energy at the

output node and also to improve internal signal nodes discharging speed [13] [14]. The basic structure of Two Phase Adiabatic Static Clocked Logic is shown in Fig.4. The circuit operation is divided into two phases *hold phase* and *evaluation phase*. During the evaluation phase, the power clock swings up. During the hold phase, power clock swings down.

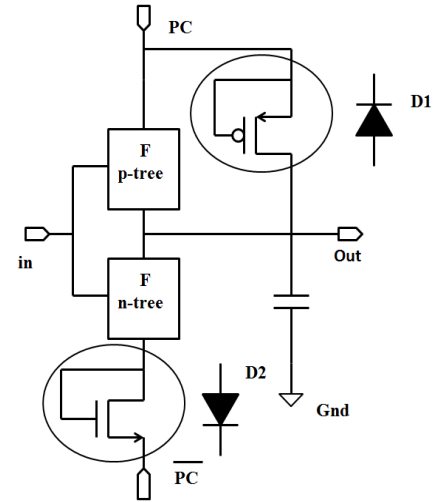


Fig.4. Basic structure of Efficient Charge Recovery Logic

3. PROPOSED SYSTEM

3.1 COMBINATION OF ECRL AND 2PASCL BASED COMPARATOR

The Fig.5 shows the circuit diagram for combination of ECRL and 2PASCL based comparator. When *a* is logic 1 and *b* is logic 0, transistor M_3 and M_4 are in active state and M_5 and M_6 are in cutoff state. This will change M_2 into active state and M_1 cutoff state. The output *agb* is high (V_{dd}). The opposite operation will take place when *a* is logic 0 and *b* is logic 1. When both inputs are same means it retains the previous state value.

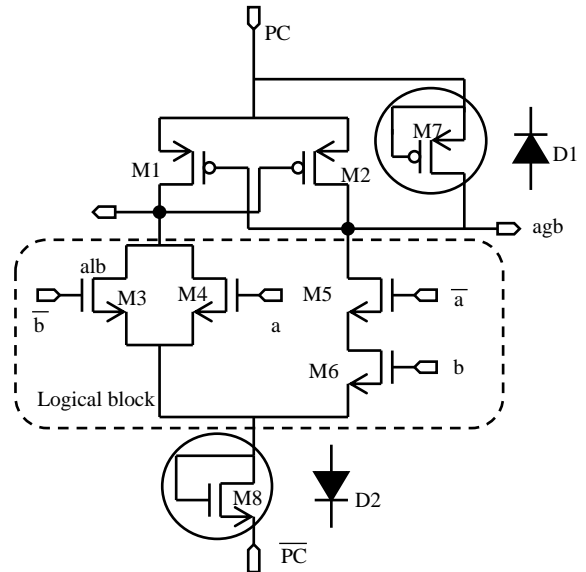


Fig.5. Circuit diagram for combination of ECRL and 2PASCL based comparator

3.2 COMBINATION OF 2N-2N2P AND 2PASCL BASED COMPARATOR

The combination of 2N-2N2P and 2PASCL logic is realized as a combination of both 2N-2N2P and 2PASCL. Its structure is similar to 2PASCL except that the core part of 2PASCL is replaced by 2N-2N2P logic circuit. It has two power clock signals operated in two different modes. The major advantage of this technique is it has less power dissipation compared to ECRL and it also gives the true function and complementary function of a given circuit. Using 2N-2N2P and 2PASCL, the comparator circuit can be constructed. The general 2N-2N2P gate consists of a two cross coupled inverters and two functional blocks F and F' (complement of F) driven by normal and complemented inputs which realizes both normal and complemented outputs. A variant of the ECRL logic family is 2N-2N2P family, the only difference is that 2N-2N2P has a pair of cross-coupled NMOS transistors in addition to the cross-coupled PMOS transistors. This combined logic provides non-floating outputs for large part of the recovery phase and also improve the discharging speed of internal signal nodes.

The Fig.6 shows the circuit diagram for combination of 2N-2N2P and 2PASCL based comparator. When a is logic 1 and b is logic 0, transistor M_5 and M_6 are active state and M_7 and M_8 are cut off state. This will turn on the transistor M_2 and M_3 and also will turn off the transistor M_3 and M_1 . The output agb is high (V_{dd}) and output alb is low. The opposite operation will take place when a is logic 0 and b is logic 1. When both inputs are same means it retains the previous state value. During charging phase of power supply M_{10} will turn on and M_9 will turn on during discharging phase of power supply.

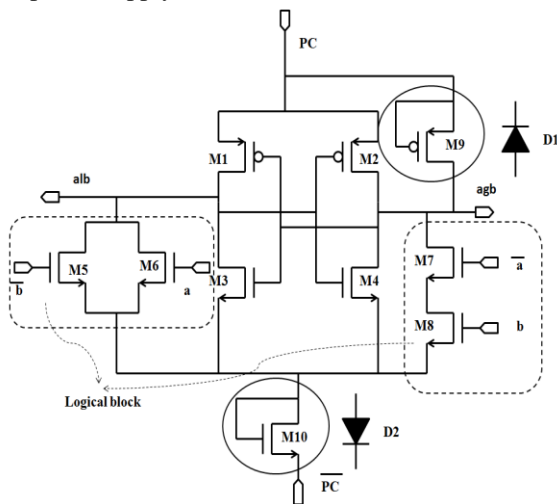


Fig.6. Circuit diagram for combination of 2N-2N2P and 2PASCL based comparator

4. RESULT AND DISCUSSIONS

4.1 COMBINATION OF ECRL AND 2PASCL BASED COMPARATOR

Combination of efficient charge recovery adiabatic logic (ECRL) and two-phase adiabatic static CMOS logic (2PASCL) based comparator is designed.

The Fig.7 gives the schematic diagram for combination of ECRL and 2PASCL based comparator. 2PASCL uses two split level complementary sinusoidal signals which operate in different modes like normal and recovery phase. It also has two diodes in its structure while comparing to ECRL. The core part is designed on the basis of ECRL which rapidly generate decision making signals. The designed comparator circuit has two input nodes, where the signals to be compared are given as input. These two inputs are designated as a and b . Depending on the input signals, the circuit has two output states low or high. If signal a is greater than signal b , one output node will charge to V_{dd} , and that node is designated as agb and another output node is alb . This decision is rapidly obtained by a transmission gate which separate power supply and functional block

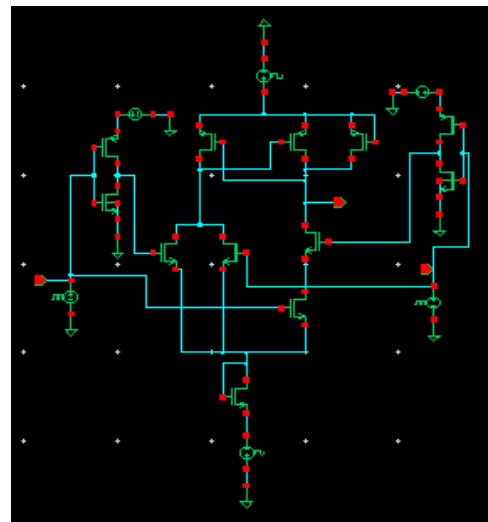


Fig.7. Schematic diagram for combination of ECRL and 2PASCL based comparator

The circuit consists of two phases of operation that is evaluation phase and recovery phase. During evaluation phase, normal comparison operation will take place only when power supply voltage swings up from 0 to V_{dd} . The recovery phase occurs when the power supply voltage swings down from V_{dd} . In this operation, the combination of ECRL and 2PASCL based comparator recover 50% of power discharged to ground. The transient analysis of ECRL and 2PASCL based comparator is shown in the Fig.8.

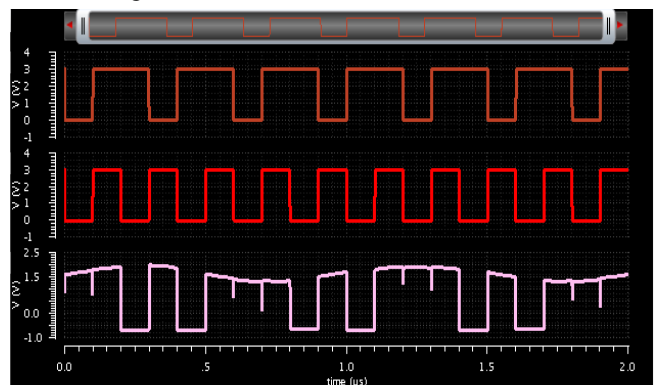


Fig.8. Transient analysis of ECRL and 2PASCL based comparator

The sinusoidal waveform represents the driving power supply voltage. This analysis infers that the normal operation takes place above the threshold voltage of rising and falling edge of the supply. After that, recovery phase starts to reuse the energy. Because of that only the device can operate when the supply voltage swings down.

The average power consumption of combination of ECRL and 2PASCL based comparator is shown in the Fig.9. It consumes power of 21.3287W for sinusoidal power supply of 3V with operating frequency 1MHz.

$$\text{Average power consumption} = 428.4 \times 10^{-3} \text{ W} = 21.3287 \text{ W}$$

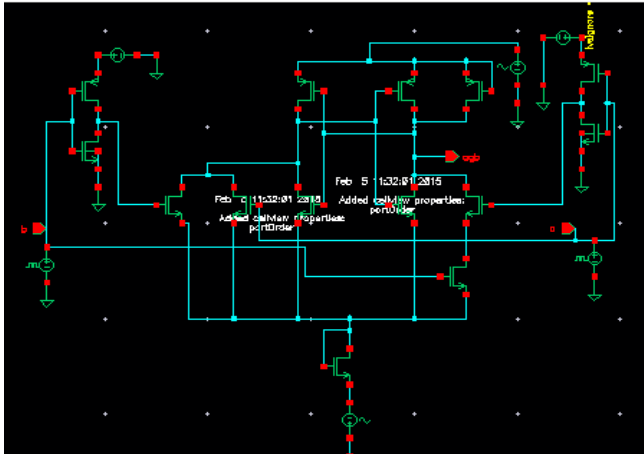


Fig.9. Schematic diagram for combination of 2N-2N2P and 2PASCL based comparator

4.2 RESULT OF COMBINATION OF 2N-2N2P AND 2PASCL BASED COMPARATOR

The schematic diagram for combination of ECRL and 2PASCL based comparator is demonstrated in Fig.9. The core part is designed on the basis of 2N-2N2P adiabatic logic in order to achieve state retention at the output node. The designed circuit has two input node where two signals to be compared is given. These two inputs are designated as *a* and *b*. Depending on the input signals, the circuit has two output states. If signal *a* is greater than signal *b*, one output node will charge to V_{dd} that node is designated to *agb* and another output node is *alb*. This decision is rapidly obtained by a transmission gate which separate power supply and functional block.

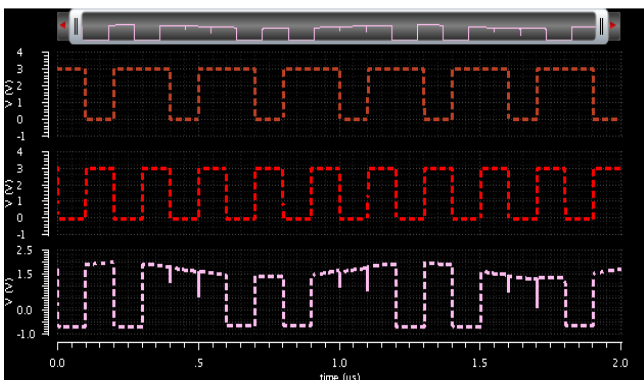


Fig.10. Transient analysis of 2N-2N2P and 2PASCL based comparator

It consists of two phases of operation that is evaluation phase and recovery phase. During evaluation phase, normal comparison operation will take place only after rising and falling edge threshold voltage of the power supply. During recovery phase occur below the threshold value of rising and falling edge. It reuses the energy stored in output node that is recovered back to the power supply. The transient analysis of combination of 2N-2N2P and 2PASCL based comparator is shown in the Fig.10.

This analysis shows that the operation similar to combination of ECRL and 2PASCL based comparator. But it has an advantage of state retention at the output node. It consumes power of 16.96743W for sinusoidal power supply of 3V with operating frequency 1MHz.

$$\text{Average power consumption} = 340.8 \times 10^{-3} \text{ W} = 16.96743 \text{ W}$$

Table.1. Comparative analysis of comparator circuit

Circuit	Average Power Consumption (W)	Power savings (%)
Double tail comparator	31.48534	--
ECRL and 2PASCL based comparator	21.3287	32.5
2N-2N2P and 2PASCL based comparator	16.96743	46

5. CONCLUSION

A simple modification is proposed that reduce the power dissipation during transistor switching. In this paper, sinusoidal power supply offers the effective utilization of power by providing the way to recycle energy at output node instead of discharged to the ground. This offers the great advantage in the reduction of the total power. Combination of different adiabatic logic families is applied to the comparator circuit which yields maximum power reduction compared to the previously available comparator. The proposed design is simulated using Cadence Virtuoso Environment. The simulation results clearly show that the proposed design has much less power compared to the conventional comparator.

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