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PARAMETRIC ANALYSIS OF DFAL BASED DYNAMIC COMPARATOR

Heena Parveen and Vishal Moyal

Department of Electronics and Telecommunication Engineering, Shri Shankaracharya Technical Campus, India

Abstract

In Complementary Metal Oxide Semiconductor (CMOS) technology, the advancement in manufacturing of semiconductor processing has changed the designing challenges for the researchers. The challenges that are now being vital are high speed and low power computing devices. This paper presents a novel dynamic comparator with DFAL (Diode Free Adiabatic Logic) inverter that employs the principle of adiabatic logic. As compared to the conventional CMOS technique, the adiabatic logic technique shows more promising results. The proposed Dynamic Comparator, not only provides low power consumption and reduces the delay, but also improves the energy efficiency in comparison to the conventional Dynamic Comparator. The design has been simulated using Cadence Virtuoso Spectre simulator in gdpk 90nm Technology.

Keywords:

Conventional Dynamic Comparator, Adiabatic Logic, DFAL Inverter, Low Power

1. INTRODUCTION

Comparators are known to be the most essential building block in Analog-to-Digital Converters (ADCs) as they act as decision making circuits throughout the transition of analog signals into digital signals. Basically, Comparators compare one input voltage signal against another voltage signal and a binary output signal is produced as per the comparison. Dynamic Comparators which fall under the classification of regenerative comparators have a wide use in high speed Analog-to-Digital Converters [1] due to their lesser power dissipation, high speed, and no static power consumption. However, certain device mismatch [2] such as parasitic node capacitance, current factor β, and threshold voltage limits the accuracy of such comparators. Also, they cause random offset voltage in comparators which degrade their performance. Using offset cancellation or calibration techniques [3-5] while implementing comparator is also an effective methodology to improve this issue. Furthermore, reduction in the offset voltage can be done by means of a preamplifier in the design of comparator, thereby requiring more consumption of power and more complex design.

As the power that has been consumed in conventional CMOS circuits is directly proportional to the circuit load capacitance and the square of the supply voltage [6], most of the researchers are focussing on supply voltage scaling and reducing the circuit load capacitance so that the power consumption can be reduced. For supply voltage scaling, the threshold voltage (V_t) of transistor should be proportionally scaled down, but sub-threshold leakage current increases with reduction in threshold voltage (V_t). The circuit load capacitance could be further minimized by a reduction in the device sizes but this will somehow affect the driving capability and speed of the circuit. Due to these limitations, in the present scenario, adiabatic logic circuits [7] are being considered for reducing the power consumption. These circuits are based on energy recovery principle, i.e. reusing the energy which is stored in the circuit load capacitance instead of following the usual means of discharging the circuit load capacitance to the ground and wasting the energy. Also, they provide better results than conventional CMOS circuits. So far, several adiabatic circuits have been presented [8]-[10] but these circuits suffer from large delay, complex circuitry, and degradation of output amplitude. To overcome the drawbacks related to diode based adiabatic circuits, 2PASCL [11] circuits were introduced which does not include diodes in its path of charging. Moreover, instead of sinusoidal or ramp power clocks, they use split level sinusoidal power clocks which charges and discharges the circuit capacitance relatively slower than other adiabatic power clocks. Although 2PASCL has an advantage of providing low power dissipation, minute current leakage exists in the circuit as gates are slowly switched ON. Also, 2PASCL circuits suffer from the problem of floating output node because of alternating hold mode in its functioning. DFAL (Diode Free Adiabatic Logic) [12] based circuits not only eliminates the problem of diode based circuits but also reduces the problem of 2PASCL circuits and thus have gained the attraction of many researchers as they offer more promising results.

This paper presents a novel dynamic comparator with DFAL inverter that not only utilizes low power [13] but also has less delay. The primary aim is to amend the overall performance in comparison to the conventional dynamic comparator without making the circuitry complex. The paper describes the structure and functioning of the Conventional Dynamic Comparator in section 2 and includes the operation of DFAL based Proposed Dynamic Comparator in section 3. Simulation results and analysis are addressed in section 4 and are followed by conclusion in section 5.

2. DYNAMIC COMPARATORS

Dynamic Comparators are often described as Clocked comparators. Regenerative feedback is generally used in Dynamic Comparators and hardly ever in non-clocked comparators. The conventional dynamic comparator which has a wide use in analog-to-digital converters is shown in Fig.1. Its working procedure is explained as follows: Dynamic Comparators have two modes of operation- reset and evaluation phase. These operating modes operate according to the clock input that is provided to the circuit.

When clock input is LOW in reset phase, transistor Mtail will be in OFF state. The reset transistors (M_5 and M_6) will become ON and will pull both the output nodes (i.e. Out_n and Out_p) to voltage V_{dd} for initiating the starting condition. During the evaluation phase, when the clock input becomes HIGH, transistors M_5 and M_6 will become OFF and simultaneously M_{tail} will be ON due to which Out_n and Out_p which were at V_{dd} will start falling with different rates of discharging.

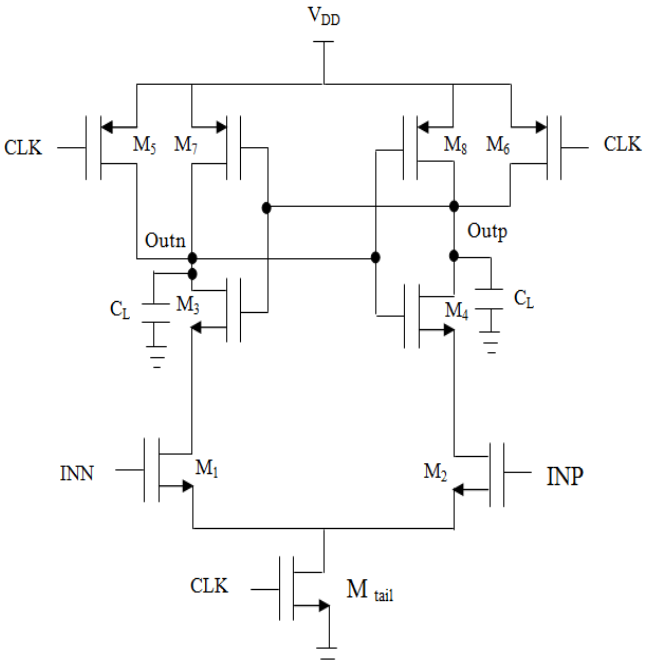

Fig.1. Conventional Dynamic Comparator

The case when V_{INP} is found to be greater than V_{INN}, here the voltage at Out_p will discharge faster than that of Out_n. Since the voltage at the node Out_p is discharged by the drain current of transistor M_2, the voltage will fall down to $V_{dd}-|V_{thp}|$ before the voltage at node Out_n is discharged by the drain current of M_1, as a result of which transistor M_7 will be ON. Consequently, the back-to-back inverters will begin the latch generation and the voltage at node Out_n will become V_{dd} and the voltage at node Out_p will fall down to the ground. The case when V_{INN} is found to be greater than V_{INP}, the circuit will work in a vice versa manner.

3. PROPOSED DYNAMIC COMPARATOR

The structure of the proposed dynamic comparator with DFAL inverter is shown in Fig.2. The primary motive of the project is reducing the consumption of power and delay of the conventional dynamic comparator by a certain level, by replacing its back-to-back inverter with a DFAL inverter that shows lower power consumption and less delay than the CMOS inverter.

3.1 CIRCUIT OPERATION

The proposed dynamic comparator consists of two split level sinusoidal power clock supply voltages V_1 as well as V_2 where one of the clocks will be in phase whereas the other one will be inverted. The voltage level of V_1 exceeds V_2 by $V_{1/2}$, which will minimize the voltage difference between the electrodes and this will result in the reduction of power dissipation. The power clocks described in the operation of the proposed comparator are composed of DC as well as sinusoidal components and can be expressed as shown in Eq.(1) and Eq.(2) respectively.

$$V_1 = \frac{V_{dd}}{4}\sin(\omega t + \phi) + \frac{3}{4}V_{dd} \quad (1)$$

$$V_2 = \frac{V_{dd}}{4}\sin(\omega t + \phi) + \frac{1}{4}V_{dd} \quad (2)$$

The proposed comparator operates in two modes evaluation and hold. In the evaluation mode, V_1 will go high and V_2 will go low, whereas in the hold mode, V_1 will go low and V_2 will go high.

During the evaluation mode, when the voltage given to the circuit is LOW, transistor M_{11} will be in OFF state while the transistors M_7 and M_8 will be in ON state. The transistors M_7 and M_8 are responsible for driving the DFAL inverters. When M_7 and M_8 are turned ON, M_9 and M_{10} also turns ON and thus will charge the load capacitances C_L resulting in a HIGH state at the output nodes (i.e. Out_n and Out_p). Conversely, when the applied voltage is HIGH, transistor M_{11} will become ON and transistors M_7 and M_8 will become OFF which in turn will turn OFF the pMOS transistors (M_9 and M_{10}) and turns ON the nMOS transistors (M_3, M_4, M_5 and M_6). Thus, the discharging process and the charges to be recycled to the power clock (V_2) will occur through nMOS transistors (M_3, M_4, M_5 and M_6) resulting in a LOW state at the output nodes (i.e. Out_n and Out_p).

In the hold mode, when the voltage given to the circuit is LOW and nMOS transistors (M_3, M_4, M_5 and M_6) turns ON, no transition will occur at the output, i.e. the output will remain low. The same process happens when the applied voltage to the circuit is HIGH and pMOS transistors (M_9 and M_{10}) turn ON. Because of the hold mode, dynamic switching reduces and hence energy dissipation can also be reduced.

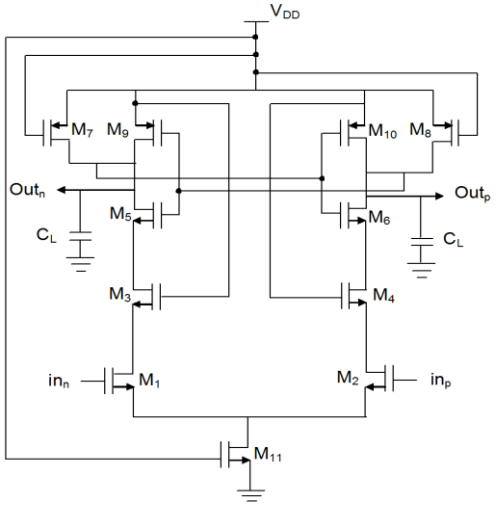

Fig.2. Proposed Dynamic Comparator

Table.1. Specifications for simulation

Technology	Cadence gdpk 90nm CMOS
Simulator	Cadence Virtuoso Spectre
MOS Dimensions	W=120nm/L=100nm for all circuits
Supply Voltage	3V
Clock Frequency	Two times the input frequency

4. SIMULATION RESULTS AND DISCUSSION

The Proposed Dynamic Comparator and Conventional dynamic comparator are designed and simulated using Cadence Virtuoso Spectre simulator in gdpk 90nm Technology at a supply voltage of 3V. The simulated waveform verifying the working of the proposed comparator with DFAL inverter is shown in Fig.3.

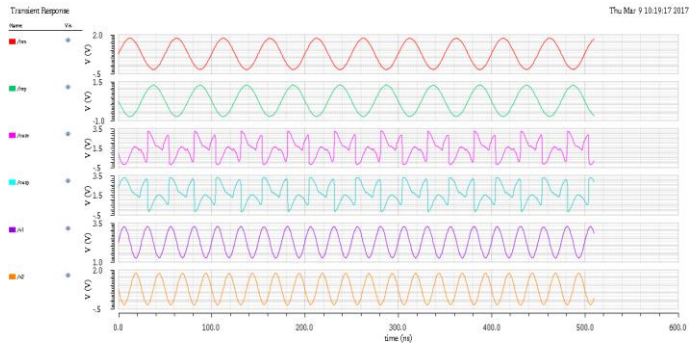

Fig.3. Simulation results of Proposed Dynamic Comparator

4.1 POWER EFFICIENCY AND DELAY BY VARYING THE FREQUENCY

In order to verify the functioning of the proposed circuit, simulation of both proposed dynamic comparator and the conventional dynamic comparator has been done and their delay and power are measured and compared with varying frequency.

The input frequency and clock frequency are varied at the same time from 1MHZ to 100MHz and the load capacitance has been set to 5fF. The clock frequency has been taken two times the input frequency and the power dissipation and delay are calculated for 10 clock cycles of charging and discharging and are shown in Fig.4 and Fig.5 respectively.

It may be observed that with the increase in frequency, the power dissipation of both the comparators (dynamic and the proposed one) increases, whereas the proposed dynamic comparator (with DFAL inverter) has a lesser power dissipation in each of the frequency as compared to the conventional dynamic comparator although a continuous reduction in delay has been observed for both the comparators with varying frequency. So, from the above analysis, it is clear that with the improvement in power and speed of the proposed comparator, the overall PDP (Power Delay Product) has also been improved in comparison to the conventional dynamic comparator. This indicates that the proposed dynamic comparator with DFAL inverter can be utilized for a wide frequency range with an improved performance than the dynamic comparator with CMOS inverter.

4.2 POWER EFFICIENCY AND DELAY BY VARYING THE LOAD CAPACITANCE

In order to verify the driving capability of the proposed comparator against the conventional dynamic comparator, extra load capacitance has been added one by one at the output node from 2fF to 20fF. The input frequency and clock frequency are kept constant at 40MHz and 80MHz respectively. Then, the power and delay are calculated for 10 clock cycles of charging and discharging and are shown in Fig.6 and Fig.7 respectively. When the capacitive load is increased gradually from 2fF to 20fF, the power dissipation of the proposed, as well as dynamic comparator, increases correspondingly and it can be clearly noticed that at each stage of varying load capacitance, the proposed comparator has better efficiency than the conventional dynamic comparator.

While the load capacitance increases, it can be noticed that the delay at the output of each comparator also increases and thus a significant enhancement can be observed in the overall PDP (Power Delay Product) for the proposed dynamic comparator against the conventional dynamic comparator.

The power, delay, energy saving percentage and adiabatic gain with respect to load capacitance and frequency of proposed and conventional dynamic comparator based on DFAL and CMOS inverters respectively has been estimated and are shown in Table.2 and Table.3 respectively.

As a comparison parameter, we have used adiabatic gain which can be illustrated as the ratio of the energy dissipated per operation of a conventional CMOS circuit and its corresponding adiabatic circuit. It can be noticed that the proposed dynamic comparator offers an energy saving of almost 90% and adiabatic gain of around 10.5 at all observed load capacitances and frequencies.

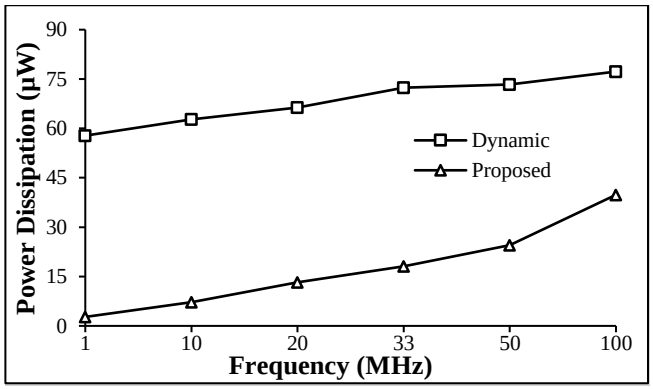

Fig.4. Power Dissipation of the Comparators with frequency

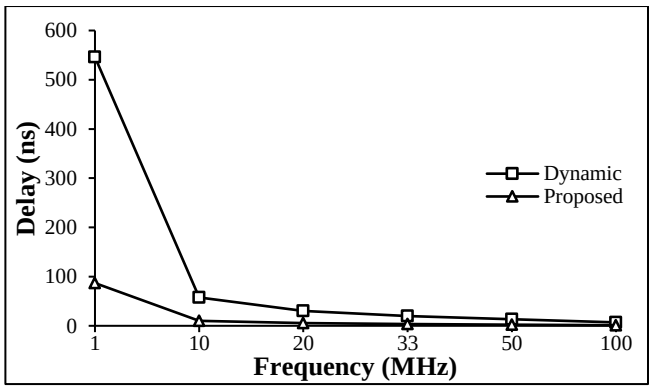

Fig.5. Delay of the Comparators with frequency

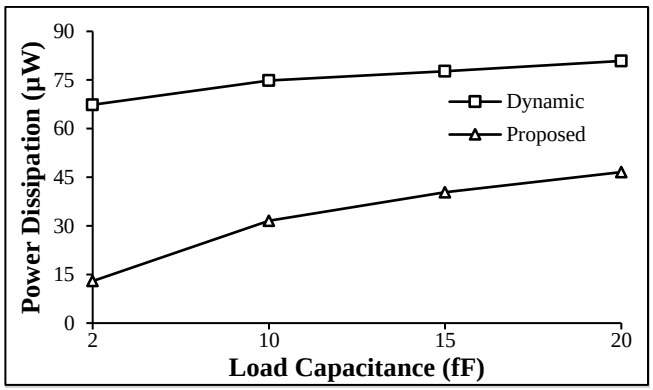

Fig.6. Power Dissipation of the Comparators with Load Capacitance

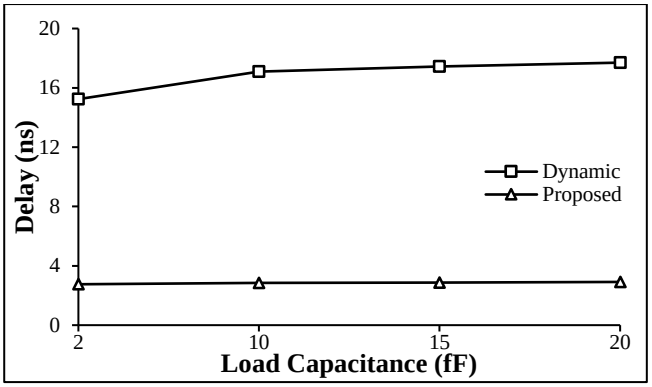

Fig.7. Delay of the Comparators with Load Capacitance

Table.2. Comparison of Power Dissipation, Delay and Power Delay Product (PDP) with varying load capacitance at input frequency= 40MHz and clock frequency = 80MHz in 10 clock cycles of charging and discharging

Comparators	**2fF**	**10fF**	**15fF**	**20fF**
Power Dissipation (µW)				
Dynamic	67.36	74.81	77.72	80.87
Proposed	12.96	31.58	40.36	46.58
Delay (ns)				
Dynamic	15.24	17.09	17.43	17.70
Proposed	2.756	2.848	2.88	2.914
PDP (pJ)				
Dynamic	1.028	1.279	1.355	1.431
Proposed	0.036	0.090	0.116	0.136
Energy Saving (%)				
	96.50	92.96	91.44	90.50
Adiabatic Gain				
	28.56	14.21	11.68	10.52

Table.3. Comparison of Power Dissipation, Delay and Power Delay Product (PDP) with varying frequency at 5fF in 10 clock cycles of charging and discharging

Comparators	1 MHz	10 MHz	20 MHz	33 MHz	50 MHz	100 MHz
Power Dissipation (µW)						
Dynamic	57.81	62.72	66.32	72.33	73.37	77.27
Proposed	2.719	7.226	13.21	18.11	24.47	39.83
Delay (ns)						
Dynamic	545.924	57.887	30.406	19.564	13.453	6.962
Proposed	86.855	9.966	5.279	3.342	2.279	1.179
PDP (pJ)						
Dynamic	31.56	3.63	2.02	1.42	0.99	0.54
Proposed	0.236	0.072	0.070	0.061	0.056	0.047
Energy Saving (%)						
	99.25	98.02	96.55	95.74	94.34	91.30
Adiabatic Gain						
	133.73	50.42	28.98	23.47	17.68	11.49

5. CONCLUSION

A novel DFAL based Dynamic Comparator has been presented. The main intention behind this proposed theory is to present a low-power energy efficient and high performance dynamic comparator with a DFAL based inverter. The conventional and proposed design of dynamic comparator has been simulated and analyzed. The design has been simulated using Cadence Virtuoso Spectre Simulator in gdpk 90nm technology at 3V supply voltage. The results of simulation and evaluation of performance comparison show that the proposed dynamic comparator is more power efficient than the conventional dynamic comparator. Also, the delay and PDP (Power Delay Product) of the proposed dynamic comparator are considerably lower as compared to the conventional dynamic comparator. Thus, an energy saving of almost 90% and adiabatic gain of around 10.5 at all observed load capacitances and frequencies has been offered by the proposed dynamic comparator. In high speed ADCs and other VLSI applications, the Proposed Dynamic Comparator would be very effective.

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