ISSN: 2395-1680 (ONLINE)
DOI: 10.21917/ijme.2026.0386

HIGH-SPEED, LOW-POWER, TRANSMISSION-GATE BASED CHARGE PUMP IN 90NM CMOS FOR PLLS IN RF/MICROWAVE SYSTEMS

Parul Trivedi, Onkesh, Madhu Dwivedi and Deepa Prajapati
Department of Electronics and Communication Engineering, Veer Bahadur Singh Purvanchal University, India

Abstract

This paper presents a detailed performance analysis of a CMOS charge pump (CP) designed for phase-locked loop (PLL) applications in RF and microwave systems, specifically targeting the S-band and C-band frequency ranges. Implemented in 90 nm CMOS technology, the proposed CP employs two complementary transmission gates to effectively suppress charge sharing and clock feed through, thereby enhancing accuracy and stability. Operating from a 1.0 V supply, the design achieves a total power consumption of 223 µW. The circuit delivers an output current of 291 µA in charging mode and 267 µA in discharging mode, maintaining a linear output voltage range from 0 V to 1 V. Designed to operate at 5 GHz, the CP demonstrates high-speed operation with low power dissipation, making it well-suited for modern high-frequency PLL architectures. Comprehensive simulation results highlight the proposed CP's capability to meet the stringent performance requirements of low-power, high-speed RF applications.

Keywords:

CP for PLL, RF/Microwave System, High Operating Frequency CP

1. INTRODUCTION

Phase-locked loops (PLLs) have become indispensable components in modern communication systems and integrated circuit design, facilitating signal synchronization, clock generation, and frequency synthesis[1] - [4]. They are widely used in applications such as audio and video synchronization, wireless communications, and high-speed data systems, where stability, low jitter, and power efficiency are critical[5]. A typical PLL architecture, as shown in Fig.1, consists of a phase frequency detector (PFD), charge pump (CP), loop filter (LF), and voltage-controlled oscillator (VCO) [5] - [9].

Among these blocks, the charge pump plays a pivotal role in driving the loop's stability, synchronization, and overall performance. A CP generates a control signal by transferring charge and shifting the VCO frequency to match the phase and frequency of the reference input from the PFD.

The CP output current charges or discharges the loop filter capacitor, generating a control voltage for the VCO. CMOS-based charge pumps, implemented via switched-capacitor circuitry in standard CMOS processes, offer several compelling advantages: notably, low power consumption, ease of digital integration, high scalability, and excellent efficiency—attributes particularly valued for modern SoC and nanoscale designs [10] [11]. In contrast, conventional charge pump architectures that rely on large transistor switches and complex current-mirror circuits often face challenges in advanced CMOS nodes. These include elevated static power dissipation, the need for matched current sources, bulky device sizing, and amplifier extensions that exacerbate process sensitivity and limit scalability [12] [13].

Charge pumps are generally classified into two main types. The first is the analog charge pump [5], which relies on diodes and capacitors for voltage conversion.

It offers simplicity and compact design but suffers from limited output current capability and higher voltage drops. The second is the digital charge pump [5], which employs transistors and switches to achieve higher output current and lower voltage drop, making it more suitable for modern integrated PLLs.

Several researchers have proposed different CP design strategies to improve performance. Sivasakthi and Radhika [14] developed a two-stage MOS current mode logic (MCML) based CP capable of 10GHz operation in 45nm CMOS, emphasizing high-speed and low-power operation without incorporating elaborate current-mismatch correction. Qiu et al. [15] presented a 1 V, 9.6 GHz CP-PLL optimized for low power and low jitter, demonstrating multi-GHz operation without heavy mismatch-compensation circuitry. A CP design using a Miller operational amplifier has been reported [16] to reduce reference spur by precisely matching charge and discharge currents; however, this improvement in linearity comes at the cost of reduced operating frequency. Similarly, a feedback-loop-based CP [17]achieved low power consumption by reducing charge/discharge currents, but its frequency range was limited. In contrast, An inverter based CP is introduced in [3]. In this paper the charge sharing concept of capacitor is used for charging and discharging of load capacitor. This paper presents a high frequency operation of charge pump.

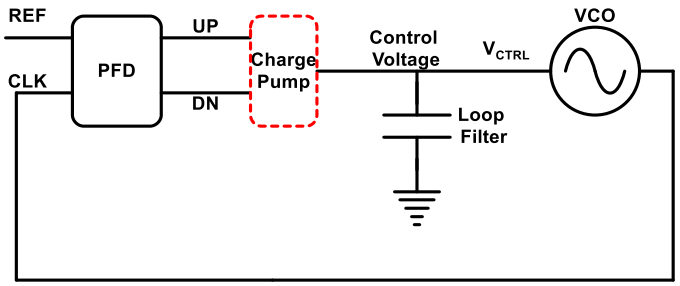

Fig.1. Typical block diagram of PLL

While these approaches have contributed to advancing CP design, a gap remains for charge pumps that can operate in the multi-GHz range with low power consumption, without incurring the complexity or speed degradation associated with heavy mismatch-correction schemes. This work addresses that gap by presenting a CMOS CP implemented in 90nm technology, optimized for 5 GHz PLL applications in RF/Microwave systems. The proposed design employs two complementary transmission gates to suppress charge sharing and clock feedthrough, achieving a very small mismatch between charging and discharging current in the output. The presented work demonstrate that the low voltage, high operating frequency, CPs can be both power efficient and practically useful in modern RF PLLs without

relying on complex mismatch compensation circuitry. The remaining part of this paper is organized as: Section 2 introduces the proposed charge pump architecture along with the design methodology. Section 3 outlines the simulation setup employed for validating the circuit performance. Section 4 discusses the operation and results of the proposed design, including idle mode, charging mode, discharging mode, power consumption analysis, and output current analysis. Section 5 provides a comparative evaluation of the proposed charge pump against recent state-of-the-art designs. Finally, Section 6 concludes the paper.

2. PROPOSED CHARGE PUMP

In the PLL design, the CP is an analog block. The traditional CP designs dissipate a significant amount of power in the milliwatt range [3]. Another issue also arises with charge leakage, which impacts the charging and discharging of the LF-capacitor, as a result the control voltage is not obtained properly [18]. Many sources have low operating frequency, which impacts the speed of the charge pump performance, and the proposed charge pump contained inverters, transmission gates (pass transistors), in which the transmission gates are helping to reduce the charge leakage [12].

A complementary transmission gate—where an NMOS and a PMOS are placed in parallel (as shown in Fig.2) offers several advantages for precision charge pump applications. First, it minimizes off-state leakage because when one device's V_{GS} approaches zero, the other remains firmly in cutoff, thereby reducing total leakage across the full voltage swing. Second, during switching, the charge injected by the NMOS channel carriers on the rising edge is effectively counteracted by the opposite-polarity charge injected from the PMOS on the falling edge.

This complementary cancellation strongly suppresses net charge transfer to the internal node, thereby reducing both charge sharing errors and clock feedthrough effects. As a result, the transmission gate provides more stable voltage transfer characteristics compared to single-MOS implementations. Finally, since the effective on-resistance (R_{on}) of the TG is the parallel combination of the NMOS and PMOS resistances, it remains low and relatively constant over the full input range. This results in a reduced RC time constant, enabling operation at multi-GHz frequencies. Similar suppression of charge injection and feedthrough effects in CMOS transmission gates has also been reported in analog switch studies[19].

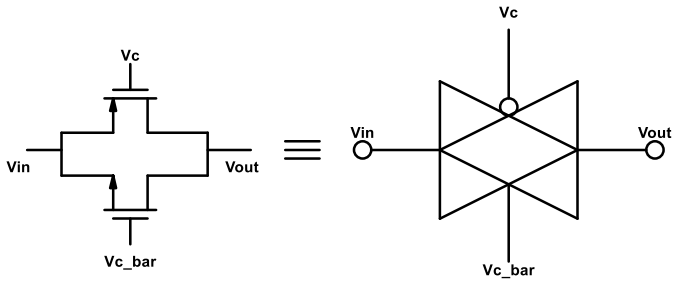

Fig.2. Representation of Transmission Gate

The proposed charge pump circuit is given in the Fig.3(a) and Fig.3(b) in which two transmission gates TG1 and TG2 are used. Transistors, MN1 & MP2 together form TG1 and MN2 & MP3 combine to form TG2. The PMOS MP1 & NMOS MN3 are used as switches to charge or discharge the output capacitor. Inverters INV1 and INV2 are CMOS based inverters and they are used to produce UP_bar and DN_bar signals respectively.

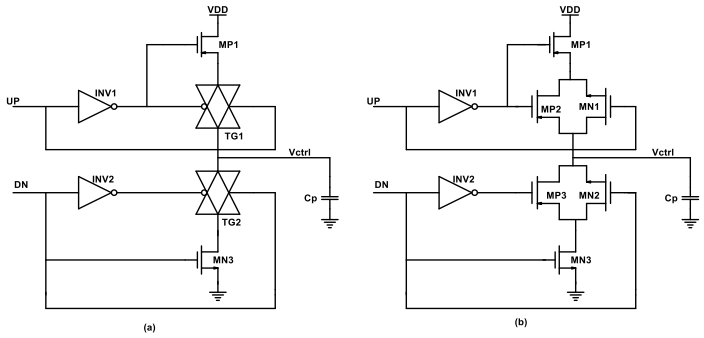

Fig.3. Proposed Transmission gate based charge pump

3. SIMULATION SETUP

The charge pump for the phase-locked loop (PLL) is designed and simulated using GPDK 90nm CMOS technology in cadence virtuoso under a 1.0V power supply. The schematic is captured using the virtuoso schematic editor, and the functional verification of the design is performed using the SPECTRE simulator. Transient analysis is carried out to evaluate the dynamic behavior of the charge pump, and power analysis is conducted to estimate its power consumption during operation.

4. OPERATION AND RESULTS

The CP is driven by the PFD's UP and DOWN pulses, which also produce the charging and discharging current. When the phase or frequency of reference signal is equal to the feedback signal, it generates no output pulses in the form of up and down signal. When the reference signal lead the feedback signal then the PFD generate UP signal and when the feedback signal lead the reference signal then PFD generate DOWN signal. The circuit is operating in three modes idle mode, pump up mode and pump down mode[3].

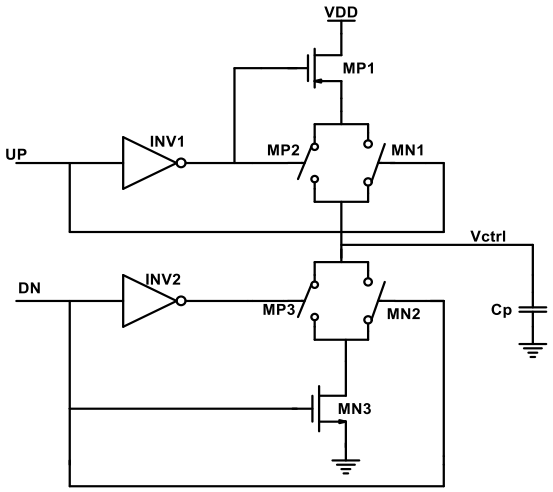

Fig.4. Switching Diagram for idle Mode of proposed Charge Pump

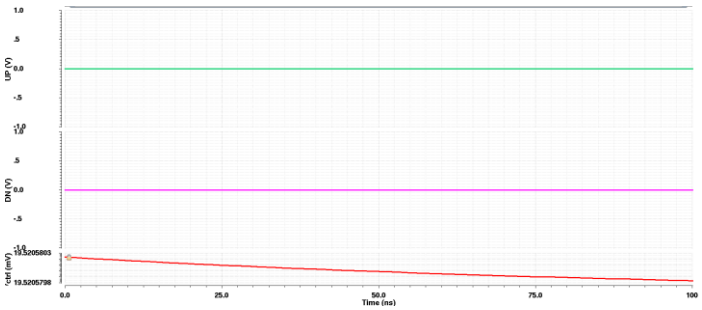

Fig.5 Transient waveform of proposed charge pump in idle mode

4.1 IDLE MODE

When both UP and DN both signals are at logic low level the charge is set to operate in idle mode. As can be seen from Fig.4 that, in this mode all the transistors and transmission Gates in the charging and discharging path are off. So in this case there is no effect on the LF-capacitor. As a result the control voltage (as shown in Fig.5) will remain at its previous state, causing the V_{ctrl} at the output to remain constant.

4.2 CHARGING MODE

If up signal is at logic high and down signal is at logic zero then the charge pump will be said to work in the charging mode. As shown in Fig.6, in charging mode transistor MP1 and transmission gate TG1 will be on and operate at their full capacity. This creates a charging path from power supply to output LF-Capacitor. While transistors MP1and transmission gate TG2 will be off so no discharge operation will be performed. As it is clear from Fig.7, that in charging mode of operation the control voltage increasing during every up pulse. The zoomed-in transient waveform shown in Fig.8 clearly shows that V_{ctrl} moves up one step after each pulse.

4.3 DISCHARGING MODE

If up pulse is at logic low and down pulse is at logic high the charge pump will be said to work in the discharge mode. As shown in Fig.9, during discharge mode transistor MN1 and transmission gate TG2 will be on, and work in its full capacity. This creates a discharging path from output LF-capacitor to ground. While transistors MP1 and TG1 of transmission gate will be off. So no charging operation will be performed in this mode. Fig.10 clearly shows the control voltage decreasing during every down pulse. The zoomed-in transient waveform, shown in Fig.11 clearly expresses that, V_{ctrl} moves one step down after every pulse.

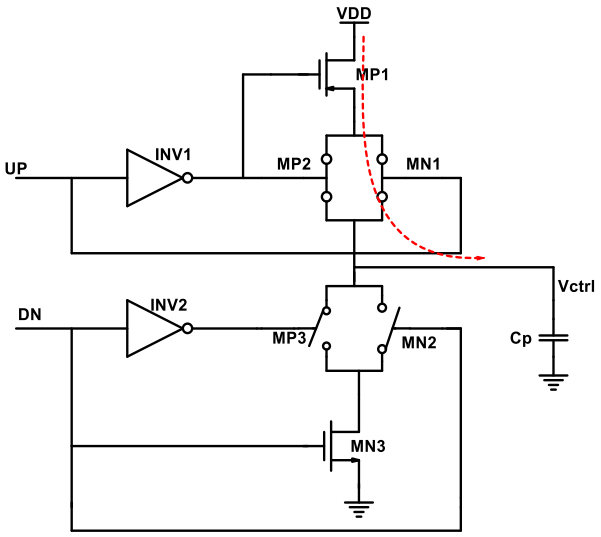

Fig.6. Switching Diagram for charging Mode of proposed Charge Pump

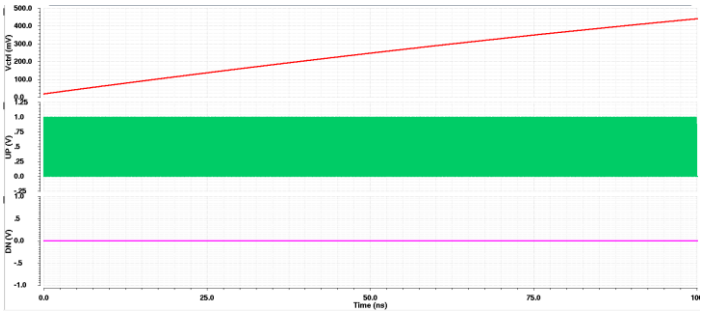

Fig.7. Transient waveform of proposed charge pump in charging mode

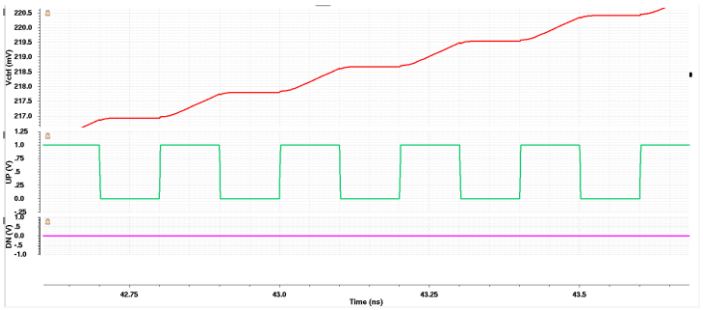

Fig.8. Zoomed-in transient waveform of the proposed charge pump in charging mode (corresponding to Fig.7).

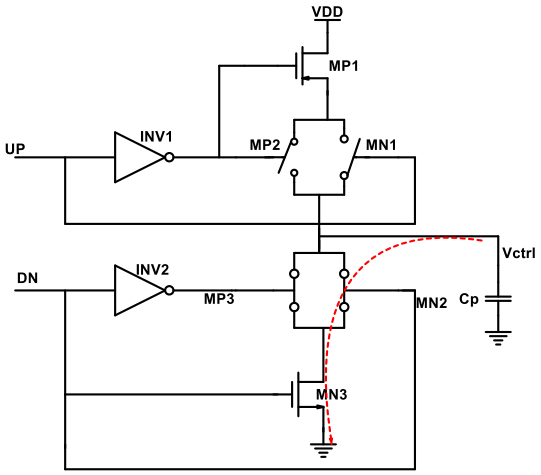

Fig.9. Switching Diagram for discharging mode of proposed Charge Pump

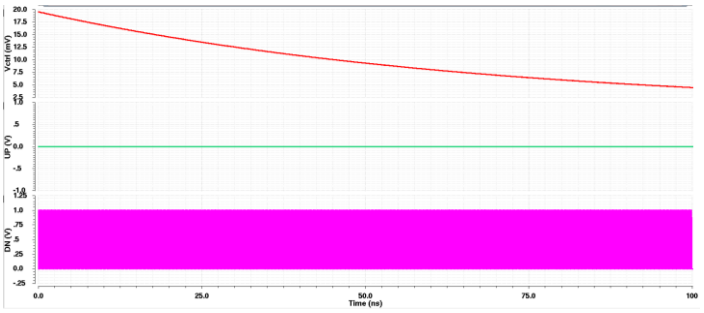

Fig.10. Transient waveform of proposed charge pump in discharging mode

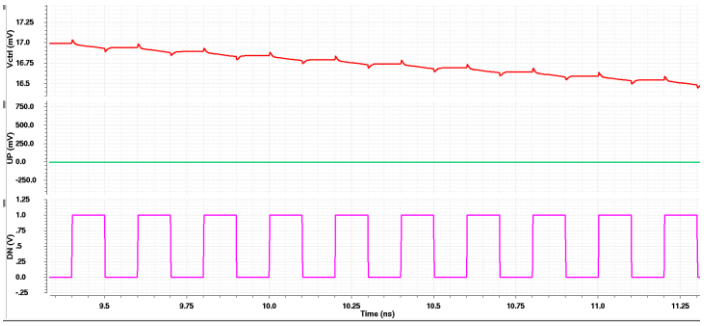

Fig.11. Zoomed-in transient waveform of the proposed charge pump in charging mode (corresponding to Fig.10)

4.4 POWER CONSUMPTION ANALYSIS

The power efficiency of the proposed Phase Frequency Detector (PFD) was evaluated through power consumption analysis at a supply voltage of 1.0 V. The design employs two transmission gates (TGs) as key switching elements, which contribute to reduced short-circuit current and minimal dynamic power dissipation due to their low on-resistance and complementary switching behavior.

The proposed PFD consume remarkably low power of 223 µW stems directly from its use of two complementary transmission gates (Fig.2). In each gate, an NMOS and a PMOS are placed in parallel so that when one device's VGS approaches zero the other is firmly cut off, minimizing off-state leakage across the full voltage swing . During switching, charge injected by the NMOS on rising edges is counteracted by the PMOS's opposite injection on falling edges, suppressing net charge transfer—and thus dynamic charge-sharing losses—at internal nodes . Finally, because each transistor's on-resistance falls when its gate is driven strongly, the combined Ron remains low and nearly constant over the entire input range, yielding a small RC time constant and supporting high frequency operation with minimal dynamic power dissipation. The charge pump's power evaluation is shown in Fig.12.

4.5 OUTPUT CURRENT ANALYSIS:

The proposed charge pump exhibits stable current performance across its operating range. Simulation results show an output current of 291 µA (Fig.13) during the charging phase and 267 µA (Fig.14) during the discharging phase at an operating frequency of 1 GHz. The difference between charging and discharging currents ensures minimal mismatch, thereby reducing static phase error in PLL applications. This balanced current operation also minimizes ripple at the output and improves overall loop stability of PLL

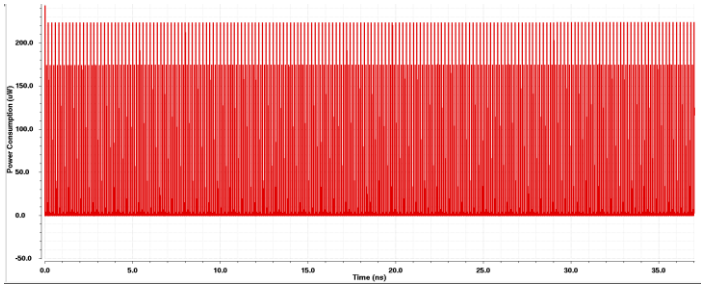

Fig.12. Simulated power consumption characteristics of the proposed charge pump

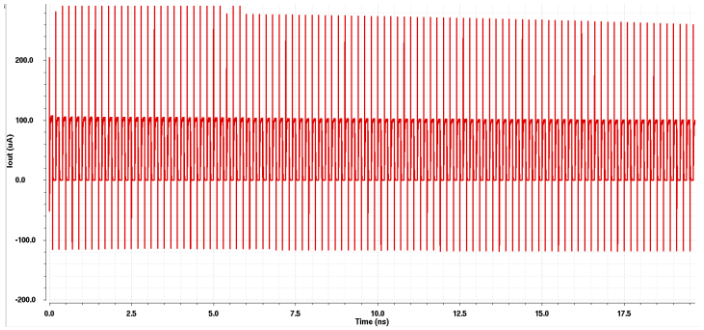

Fig.13. Output current of the proposed charge pump in charging mode (≈ 291 µA)

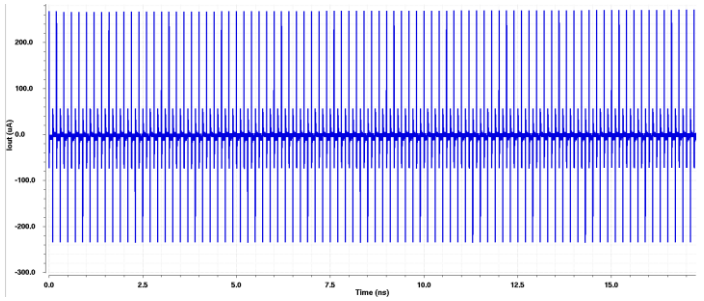

Fig.14. Output current of the proposed charge pump in discharging mode (≈ 267 µA)

Table.1. Comparison with Proposed Charge Pump with Previous Designs

Ref	Supply (V)	Technology	Power consumption	Operating Frequency	Output Current
[1]	_	0.15um Win GaAs pHEMT	56 mW	3.584-4.021 GHz	5 mA
[2]	1.2	65 nm CMOS	176 µW	1 GHz	100 µA
[3]	1.8	180 nm CMOS	0.35mW	1.6GHz	200µA
[4]	1.8	180nm CMOS	274µW	4 GHz	----
[17]	1.8	180 nm CMOS	410-740µW	50-800 MHz	19.9µA
[20]	1.8	180 nm CMOS	0.56 mW		100 µA
[21]	1.3	130 nm CMOS	10.7 mW	2.2-2.4 GHz	100 µA
This work	1.0	90 nm CMOS	223 µW	5 GHz	291 µA Charging
					267 µA Discharging

5. COMPARATIVE ANALYSIS OF PROPOSED CHARGE PUMP

The Table.1 summarizes the comparison with a few of the current works, showing how our proposed design outperforms them in terms of power consumption and operational frequency. The Table.1 presents a comparison of the proposed PFD with prior works in terms of supply voltage, technology node, power consumption, operating frequency, and output current. While earlier CMOS and GaAs implementations demonstrate either high current drive at the cost of power or low power with limited frequency. The Table.1 shows that the proposed CP ensuring robust performance for RF/microwave phase-locked loop applications

6. CONCLUSION

A CMOS charge pump optimized for high-frequency PLL applications for RF/Microwave has been presented. Implemented in 90 nm CMOS technology, the design utilizes complementary transmission gates to effectively mitigate charge sharing and clock feedthrough, thereby ensuring improved output accuracy and stability. Operating from a low supply voltage of 1.0 V, the proposed CP achieves an output current of 291 µA in charging mode and 267 µA in discharging mode. With a total power consumption of only 223 µW at 5 GHz, the circuit demonstrates the capability to support low-power and high-speed operation. These results confirm that the proposed architecture meets the stringent requirements of modern RF PLLs, offering a robust solution for integration in next-generation wireless communication systems.

REFERENCES

[1] R. Zhao, Y. Zhang, H. Lv and Y. Wu, “Design and Implementation of Charge Pump Phase-Locked Loop Frequency Source Based on GaAs pHEMT Process”, *Sensors*, Vol. 22, No. 2, pp. 504-521, 2022.

[2] H. Lad Kirankumar, S. Rekha and T. Laxminidhi, “Low Mismatch High-Speed Charge Pump for High Bandwidth Phase Locked Loops”, *Microelectronics Journal*, Vol. 114, pp. 105156-105167, 2021.

[3] J.K. Sahani, A. Singh and A. Agarwal, “A Wide Frequency Range Low Jitter Integer PLL with Switch and Inverter Based CP in 0.18 µm CMOS Technology”, *Journal of Circuits, Systems and Computers*, Vol. 29, No. 9, pp. 2050142-2050153, 2020.

[4] Vaishali and R.K. Sharma, “An Improved Dynamic Range Charge Pump with Reduced Current Mismatch for PLL Applications”, *Proceedings of International Conference on Intelligent Computing and Control Systems*, pp. 1-19-1022, 2018.

[5] S.M. Schober and J. Choma, “A Charge Transfer-Based High Performance, Ultra-Low Power CMOS Charge Pump for PLLs”, *Analog Integrated Circuits and Signal Processing*, Vol. 89, No. 3, pp. 561-573, 2016.

[6] P. Trivedi and B.B. Tiwari, “Low Phase Noise, Low Power 4-Stage Ring VCO for OFDM Systems”, *Journal of Circuits, Systems and Computers*, Vol. 32, No. 1, pp. 1-25, 2023.

[7] P. Trivedi and B.B. Tiwari, “Supply Less Sensitive Ring Voltage-Controlled Oscillator for Microwave L-Band Frequencies”, *Circuit World*, Vol. 34, No. 1, pp. 1-13, 2022.

[8] P. Trivedi and B.B. Tiwari, “High Operating Frequency, Low-Power PFD for PLL Applications”, *Proceedings of International Conference on Computing Communication and Networking Technologies*, pp. 1-5, 2023.

[9] P. Trivedi and B.B. Tiwari, “Wide Tuning Range 4-Stage Ring VCO for Phase Locked Loop”, *Proceedings of International Conference on Microwave, Antenna and Communication*, pp. 1-4, 2023.

[10] S. Golestan, J.M. Guerrero and J.C. Vasquez, “Three-Phase PLLs: A Review of Recent Advances”, *IEEE Transactions on Power Electronics*, Vol. 32, No. 3, pp. 1894-1907, 2017.

[11] L.F. Rahman, M. Marufuzzaman, L. Alam and M. Bin Mokhtar, “Design Topologies of a CMOS Charge Pump Circuit for Low Power Applications”, *Electronics*, Vol. 10, No. 6, pp. 676-687, 2021.

[12] U. Nanda, D.P. Acharya and S.K. Patra, “A New Transmission Gate Cascode Current Mirror Charge Pump for Fast Locking Low Noise PLL”, *Circuits, Systems, and Signal Processing*, Vol. 33, No. 9, pp. 2709-2718, 2014.

[13] M. Guo, L. Wang, S. Wang, J. Lu and M. Cui, "A Low Mismatch Current Charge Pump Applied to Phase-Locked Loops", *Micromachines*, Vol. 15, No. 7, pp. 913-926, 2024.

[14] M. Sivasakthi and P. Radhika, "A High-Speed MCML Charge Pump Design at 10 GHz Frequency in 45 nm CMOS Technology for PLL Application", *Analog Integrated Circuits and Signal Processing*, Vol. 118, No. 1, pp. 49-66, 2024.

[15] D. Qiu, X. Kong, M. Jian, J. Zheng and C. Guo, "A 1-V 9.6-GHz Charge-Pump PLL with Low RMS-Integrated Jitter", *Microelectronics Journal*, Vol. 142, pp. 106006-106017, 2023.

[16] A.M. Suraj Kumar Saw, Payali Das and Madhusudan Maiti, "A 90nm Design of Charge Pump Circuit for Perfect Current Matching", *Proceedings of International Conference on Microwave and Communication*, pp. 128-132, 2017.

[17] M. Estebsari, M. Gholami and M.J. Ghahramanpour, "A Novel Charge Pump with Low Current for Low-Power Delay-Locked Loops", *Circuits, Systems, and Signal Processing*, Vol. 36, No. 9, pp. 3514-3526, 2017.

[18] B. Razavi, "*Design of Integrated Circuits for Optical Communications*", McGraw-Hil, 2002.

[19] W.M.C. Sansen, "*Analog Design Essentials*", Springer, 2006.

[20] O. Lozada and G. Espinosa, "A Charge Pump with a 0.32% of Current Mismatch for a High Speed PLL", *Analog Integrated Circuits and Signal Processing*, Vol. 86, No. 2, pp. 321-326, 2016.

[21] R.R. Manikandan and B. Amrutur, "A Zero Charge-Pump Mismatch Current Tracking Loop for Reference Spur Reduction in PLLs", *Microelectronics Journal*, Vol. 46, No. 6, pp. 422-430, 2015.