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LOW QUANTUM-COST REVERSIBLE LOGIC APPROXIMATE MULTIPLIERS

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Abstract

The reversible logic (RL) is emerging as a one of the promising techniques for design and development of computationally intensive arithmetic applications such as artificial intelligence (AI), machine-learning (ML), Robotics, etc. As the benefits of CMOS scaling is gradually diminishing and quest to achieve low power and high-performance has made the researchers to look into alternate logic styles and computation techniques to implement circuits. In recent years, the RL has emerged as a low power technique to design the circuits using emerging nanotechnologies such as quantum cellular automata (QCA), Spintronics, etc. On the other side, `approximate-computing' technique has emerging as a most promising technique to design an energy-efficient circuits for error-tolerant applications such as image and video processing. The multiplier being critical element of image or video processing application plays an important role in the contribution of overall performance of the system under consideration. In this paper we present design and analysis of four novel approximate multipliers using approximate reversible logic gates that are reported in the recent literature. The proposed multipliers have been analyzed in terms of image-quality and circuit design metrics. From the analysis, it is found that the proposed multipliers are found to be superior in terms of quantum-cost, power, area, and image quality metrics.

Keywords:

Reversible Logic, Low Power, Full Adder, Quantum Gates, Quantum Cost

1. INTRODUCTION

Modern computationally intensive battery-operated "Internet-of-Things" (IoT) devices demand energy-efficient multimedia processors. The critical block in this processor is "Multiply-accumulate" (MAC) and is an important and most expensive operation in many AI and ML applications. Apart from these applications, the MAC operations are extensively used in many other applications including tensor processing units (TPUs), audio, speech, video, object detection, neural network (NN), convolution, filtering, [1-3] etc. The MAC has: a multiplier, an adder, and an accumulator [4-6].

Energy dissipation is inevitable in conventional irreversible logic gates [7]. The energy dissipation occurs mainly due to loss of information. The amount of heat generated per bit of information lost is $kT\log 2$ Joules [8], where k is Boltzmann's constant and T is the absolute temperature at which operation is performed. The problem of information loss can be mitigated by using reversible logic, where the inputs and outputs have one-to-one mapping. And also, every input vector can be uniquely recovered from the output vectors and vice-versa [7].

The full-adder cell (FAC) is being a leaf or primitive cell of any MAC has a direct influence on overall performance of the multimedia processor. Thus, FAC has become the center of attraction for most of the researchers to design energy efficient DSP systems. The various alternate techniques for low power circuit design based on approximate computing have been discussed in the current literature. The reduction in power dissipation can be achieved at various levels of design abstraction: Algorithmic level, Architecture level, Gate level, and Transistor level. The low power is achieved at the algorithmic level, by significant driven computation (SDC), the computations at this level are classified as significant and non-significant. The significant and non-significant computations are implemented using exact and approximate circuits respectively [9]. The enhancement in power efficiency at architectural level, can be achieved through the voltage over scaling (VOS) [10]. To achieve low power using VOS, the supply voltage is scaled down below its lower bound. The power reduction at gate level, using VOS was also discussed in [11-12]. The voltage scaling allows to use different supply voltages for various logic gates of the same circuit. Many other works reported have extensively discussed on power reduction at transistor circuit level [13-14]. Power reduction at circuit level is achieved using mixed logic styles, where circuit under consideration is designed using more than one type of logic. For example, pass transistor logic style is used along with the static CMOS logic. With an emergence of reversible logic (RL), the RL gates have gained more popularity in the design of energy-efficient arithmetic circuits. Thus, reversibility has become most promising and an indispensable paradigm in future low power circuit design. Many approximate FC (AFC) realizations using reversible logic gates have been proposed and discussed in the state-of-the-art literature.

Some of the main issues associated with the current state-of-the-art techniques in developing multipliers using reversible logic and approximation include high quantum costs, large garbage outputs, high constant inputs, inadequate error control measures, and failure to consider scalability. The high quantum cost associated with the majority of the conventional designs in implementing a multi-digit multiplier based on reversible logic is accompanied by the generation of too much garbage and high constant inputs. Approximate computing techniques focus primarily on reducing the consumption of power while paying little attention to the issue of managing error propagation, resulting in poor performance in critical applications. Another important aspect regarding the development of approximate logic-based designs is the failure of existing solutions to provide a unified approach that addresses approximation and reversibility simultaneously. Finally, there is a lack of emphasis in some of the existing solutions on application-specific performance criteria such as PSNR and SSIM.

Innovatively, the design of low quantum-cost approximate multipliers through reversible logic with energy consumption and accuracy optimization in parallel is the main novelty in this paper. This work differs from other existing approaches where approximation and reversibility are considered independently because a family of new Reversible Logic Approximate Full Adder Cells (RAFC3a–RAFC3d) with minimum quantum cost, garbage, and hardware utilization is proposed. The suggested adder units are embedded into the Wallace-tree-based multiplier structure to enable a proper balance between accurate and approximate calculations in most significant bits (MSBs) and least significant bits (LSBs), respectively. An innovative contribution in the current study is the analysis of the suggested designs using both circuit level metrics (power, delay, power-delay-product (PDP), area) and application level metrics (PSNR and SSIM) of image quality. The experimental results show that RAFC3a and RAFC3b have higher hardware and computational efficiency than other approaches.

Rest of this paper is organized as follows. The next section presents the existing and proposed RL approximate adders and their quantum metrics. Section 3 presents the design of approximate multiplier based on our proposed approximate adders. The section 4 presents the design results and discussion. Finally, section-5 concludes the paper.

2. RL BASED APPROXIMATE ADDERS AND THEIR QUANTUM METRICS

This section presents existing and proposed RL based AFCs and their important features. The conventional reversible logic gates that are used to design reversible circuits are:

2.1 EXISTING APPROXIMATE FULL-ADDER CELLS

The existing approximate full adder cells that were reported in current literature [15, 16] are shown in Fig.1(a), Fig.1(b), and Fig.1(c). The salient features of these adders in terms of their quantum design metrics such as quantum-cost (QC), number of garbage-outputs (GOs), number of constant inputs (CIs), etc. are presented as follows.

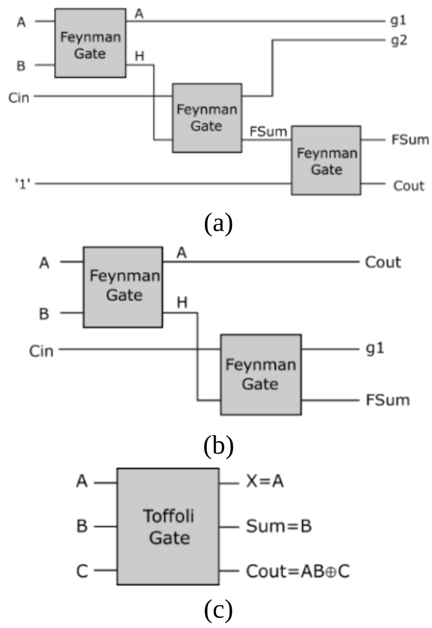

Fig.1. Existing RL based Approximate Adders

The Fig.1(a) is referred to as RAFC1a, has been designed using three Feynman gates with a total QC=3, two-garbage outputs, and one-constant input. The Fig.1(b) (RAFC1b) uses two Feynman gates with a total QC=2, one-garbage output, no constant inputs. The Fig.1(c) (RAFC2) uses one Toffoli gate, with a QC=5, one-garbage output, no constant inputs.

2.2 PROPOSED APPROXIMATE FA CELLS

The proposed approximate adders that were reported in our earlier publication in [17] are listed in Fig.2. The main motivation to derive the following approximate adders is to achieve low quantum cost with an objective to trade-off between error metrics and image quality metrics for image processing applications.

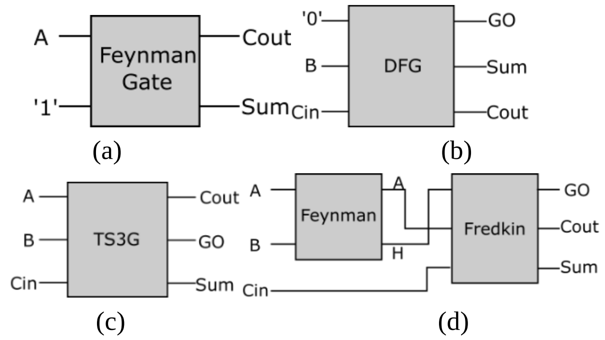

Fig.2. Proposed RL based Approximate Adders

The following are the salient features of the proposed approximate adder cells:

- The Fig.2(a) is a proposed approximate adder cell herein referred to as RAFC3a, having $Sum = \bar{A}$, $Cout = A$. The quantum metrics are *QC*=1, *GO*s=0, and *CI*s=1.
- The Fig.2(b) is a proposed approximate adder cell herein referred to as RAFC3b, having Sum=*B*, Cout=*Cin*. The quantum metrics are *QC*=2, *GO*s=1, and *CI*s=1.
- The Fig.2(c) is a proposed approximate adder cell herein referred to as RAFC3c, having *Sum*=*A*⊕*B*⊕*Cin*, *Cout*=*A*. The quantum metrics are *QC*=2, *GO*s=1, and *CI*s=0.
- The Fig.2(d) is a proposed approximate adder cell herein referred to as RAFC3d, having $\mathrm{Sum} = HA \oplus \bar{H}\, C_{in}$, $C_{out} = \bar{H}A \oplus H\, C_{in}$, where *H*=*A*⊕*B*. The quantum metrics are *QC*=6, *GO*s=1, and *CI*s=0.

3. PROPOSED APPROXIMATE MULTIPLIER ARCHITECTURE

The proposed methodology involves the design and analysis of low quantum cost approximate multipliers with the help of reversible computing concepts. At first, some efficient RAFC (Reversible Approximate Full Adder Cells), namely, RAFC3a, RAFC3b, RAFC3c, and RAFC3d are designed based on minimal quantum cost, garbage outputs, and constant inputs. Then these adders are used within the structure of a Wallace tree multiplier, in which RAFCs are used for LSB (Least Significant Bit) computation in order to obtain lower power and area requirements, whereas MSBs (Most Significant Bits) are calculated using EXACT ADDERS to retain accuracy. All designs are simulated using Verilog HDL language and synthesized using the 90nm standard cell library in order to analyze parameters such as power consumption, delay, PDP (Power Delay Product), and area. Simultaneously, simulations have been performed using MATLAB software by analyzing parameters including PSNR (Peak Signal to Noise Ratio) and SSIM (Structural Similarity Index).

To assess the performance of the proposed approximate adder and compare their merits over the existing adders, we have proposed the following approximate multiplier derived based Wallace-tree based multiplier architecture.

The Fig.3 is an 8×8 approximate multiplier dot diagram used to illustrate design and method of partial products compression. The partial products that are generated in the first stage are gradually compressed into the final two rows using both exact and approximate compressors.

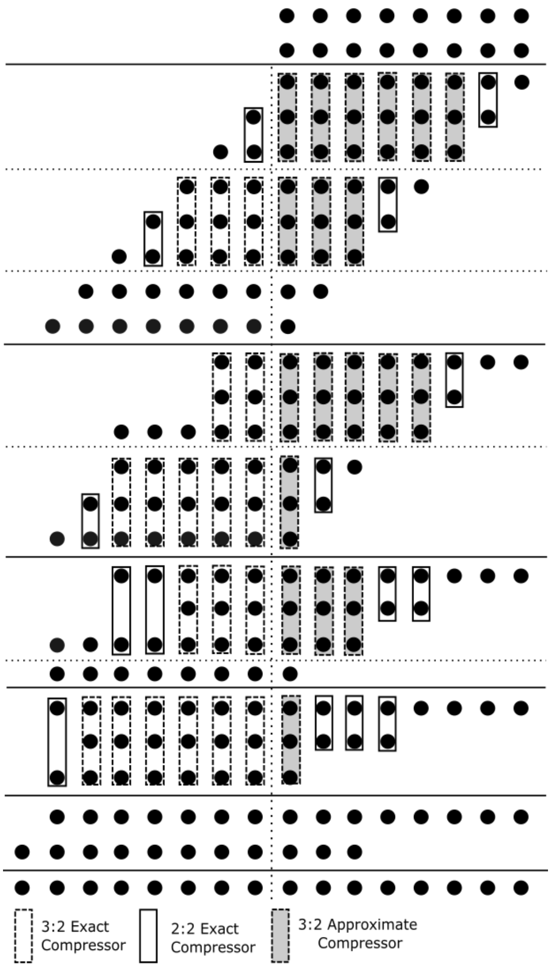

Fig.3: Dot diagram of proposed approximate multiplier architecture

The proposed multiplier architecture has divided into two parts namely MSB and LSB. The MSB is designed using compressors (exact full adder and exact half adder cells). The LSB is designed using compressors (approximate full adder and exact half adder cells). Depending on the type of approximate adder cell used, we have proposed a total 7- approximate multipliers. All these multipliers are designed and simulated using Verilog-HDL and MATLAB simulations. Based on the simulations the performance metrics that are extracted are tabulated in Table.1 and Table.2.

Table.1. Circuit design metrics of proposed multipliers

Multiplier Design	Power (μW)	Delay (nS)	PDP (fJ)	Area (μm^2)
RAFC1a	87	1.8	156	1403
RAFC1b	77	1.7	131	1360
RAFC2	50	1.6	80	1245
RAFC3a	**40**	**1.5**	**60**	**910**
RAFC3b	**40**	**1.5**	**60**	**958**
RAFC3c	52	1.6	83	1245
RAFC3d	57	1.7	97	1461

Table.2. Image quality metrics of proposed multipliers

Multiplier Design	PSNR (dB)	SSIM
RAFC1a	43	0.95
RAFC1b	44	0.98
RAFC2	45	0.99
RAFC3a	**46**	**0.99**
RAFC3b	**47**	**0.99**
RAFC3c	44	0.98
RAFC3d	50	0.99

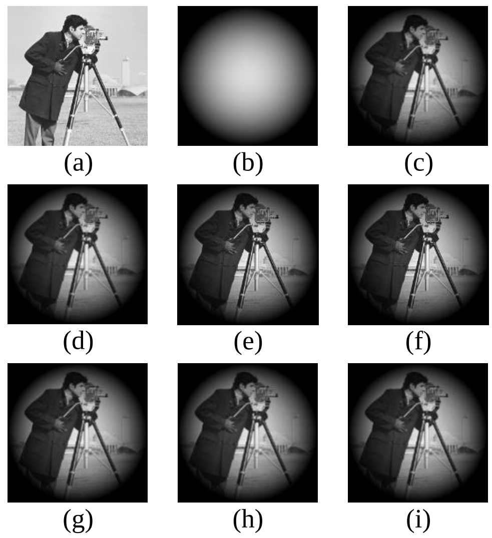

Fig.4. Image multiplication outputs of proposed multipliers

To extract the circuit design metrics the proposed multipliers under consideration are designed using Verilog-HDL and synthesized using Cadences' generic 90nm standard cell library. To extract image-quality metrics, the multipliers are designed to process image multiplication using MATLAB with two images as an input. The image multiplication results are also shown in the Fig.4.

The Fig.4(a) and Fig.4(b) represent the test images to be multiplied using the proposed multipliers designed based on existing and proposed approximate multipliers. The Fig.4(c) (RAFC1a), Fig.4(d) ((RAFC1b), and Fig.4(e) (RAFC2) represent the image multiplication output of proposed multipliers designed using reported approximated adders. The Fig.4(f) (RAFC3a),

Fig.4(g) ((RAFC3b), Fig.4(h) ((RAFC3c), and Fig.4(i) (RAFC3d) represent the image multiplication output of proposed multipliers designed using proposed approximated adders.

4. MULTIPLIER DESIGN RESULTS AND DISCUSSION

Based on the extracted results from the circuit design metrics and image quality metrics from image multiplication results the following are the observation: From Table.1, the proposed multipliers RAFA3a and RAFC3b using proposed adders are found to be low power and area efficient. From Table.2, the proposed multipliers RAFA3a and RAFC3b are found to be more efficient in terms of PSNR and SSIM. Further the quantum cost of the proposed multipliers RAFA3a and RAFC3b are also same and equal to one. Which is quite low as compared to the existing approximate adders based on reversible logic.

Thus, considering aforementioned observations, among the proposed multiplier designs the two approximate multiplier designs RAFC3a and RAFC3b are found to be efficient designs in terms of both circuit design and image quality metrics and hence they are found to be an ideal choice for image processing applications.

5. CONCLUSION

In this paper, a total seven approximate multipliers have proposed using existing and proposed reversible approximate adders. All the proposed approximate multipliers are designed, simulated and synthesized using Verilog-HDL using Cadences 90nm standard cell library. Further, the efficacy of these multiplier designs has been studied through image multiplication applications using MATLAB codes. Based on the comparison results, among proposed multiplier designs, two multiplier designs are found to be low-power, area- efficient, and also having low quantum cost with high PSNR and SSIM values, indicating their suitability for image processing applications. Some possible directions for future work on the reversible logic approximate multipliers proposed in this thesis include exploring the scalability of the designs towards more sophisticated and larger design approaches. For example, one possibility would be to explore the use of larger multipliers and hierarchical architecture for the evaluation of scalability for complicated AI and signal processing systems. Optimization of these designs can also be done through adaptation, whereby the level of approximation varies depending on user-defined requirements. Furthermore, implementation of the designs in emerging technologies like QCA and spintronic device implementations can give an idea about the real-time efficiency of the multipliers. Another potential extension includes designing methods for error resilience and tolerance. Real-world applicability of the multipliers can also be evaluated for scenarios like deep neural network applications, image compression, and edge computing systems. Lastly, another possibility includes using reversible logic together with machine learning algorithms for optimal exploration of the design space.

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