DOI: 10.21917/ijme.2026.0375

SUB-THRESHOLD CMOS SENSOR INTERFACE FOR ULTRA–LOW-ENERGY WEARABLE HEALTH MONITORS

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Abstract

Wearable health monitors have required continuous physiological signal acquisition under severe energy constraints. Conventional sensor interfaces have consumed significant power due to super-threshold biasing and frequent data conversion. Sub-threshold CMOS operation has emerged as a viable alternative for achieving ultra–low-energy sensing while maintaining acceptable signal fidelity. Prior studies have highlighted feasibility, yet practical interface stability and noise robustness have remained limited. Existing wearable sensor interfaces have suffered from excessive energy consumption, reduced battery lifetime, and poor performance under low-voltage operation. Process variations, thermal noise, and leakage effects have degraded accuracy when circuits have operated in the sub-threshold region. These challenges have restricted long-term deployment in body-worn healthcare systems. This work has proposed a sub-threshold CMOS sensor interface that has targeted ultra–low-energy wearable applications. The interface architecture has included a low-noise transconductance amplifier, an adaptive bias generator that has regulated operating points, and an energy-efficient analog-to-digital conversion stage. A calibration mechanism that has compensated process variations has been integrated. Circuit blocks that which operate below threshold voltage have been optimized for robustness. The design has been validated using standard CMOS technology through post-layout simulations and measured prototypes. The proposed sub-threshold CMOS sensor interface demonstrates an average power consumption of 41 nW at a 0.4 V supply after 200 iterations, which represents a reduction of approximately 53% compared with event-driven sub-threshold designs. Input-referred noise remains below 4.6 µVrms, while the signal-to-noise ratio exceeds 58 dB. The energy per conversion reaches 16 pJ, and gain drift is limited to 3.0% under process and temperature variations. These results confirm that the interface supports stable and ultra–low-energy wearable health monitoring.

Keywords:

Sub-Threshold CMOS, Wearable Health Monitors, Ultra-Low Energy Circuits, Sensor Interface, Low-Power Biomedical Electronics

1. INTRODUCTION

Wearable health monitoring systems have transformed continuous medical observation by enabling non-invasive and real-time physiological data acquisition. These systems have relied heavily on integrated sensor interfaces that operate under tight energy budgets due to small battery capacities and long-term usage requirements. Prior research has established that CMOS-based sensor interfaces have dominated wearable platforms because of their scalability and compatibility with standard fabrication processes [1–3]. Sub-threshold CMOS operation, where transistors operate below the threshold voltage, is presently recognized as a promising approach for achieving ultra–low-energy consumption. This operating regime has allowed circuits to mimic weak-inversion behavior that which significantly reduces dynamic and static power dissipation. As a result, sub-threshold designs have been increasingly explored for biomedical sensing applications. Despite these advantages, several challenges have persisted in sub-threshold sensor interface design. Circuits that have operated in this region have exhibited high sensitivity to process, voltage, and temperature variations, which have degraded reliability and repeatability [4]. Noise susceptibility, particularly thermal and flicker noise, has also increased due to reduced signal swings. Additionally, leakage currents and mismatch effects have complicated bias stability, which has limited deployment in real-world wearable environments [5]. These issues have constrained the adoption of sub-threshold interfaces in safety-critical health monitoring systems. The core problem has remained the development of a sensor interface that has sustained ultra–low-energy operation while preserving signal integrity, robustness, and long-term stability. Existing solutions have either reduced power at the cost of accuracy or improved performance with increased energy consumption [6]. This trade-off has restricted continuous monitoring in wearable health devices. The primary objective of this work has been to design a sub-threshold CMOS sensor interface that has minimized energy consumption without compromising noise performance and stability. Secondary objectives have included enhancing tolerance to process variations, reducing long-term drift, and maintaining compatibility with standard CMOS technology.

The novelty of this research has resided in the integration of an adaptive biasing mechanism with a calibrated sub-threshold front-end architecture. Unlike prior designs, the proposed approach has dynamically stabilized operating points under varying conditions, which has improved robustness during prolonged operation. The main contributions of this work have been twofold. First, a low-noise sub-threshold sensor interface that has achieved nanowatt-level power consumption has been designed and validated. Second, a variation-aware calibration strategy that has improved stability and repeatability in wearable health monitoring scenarios has been demonstrated.

2. RELATED WORKS

Early studies on low-power wearable sensor interfaces have primarily focused on super-threshold CMOS designs that have optimized duty cycling and power gating techniques [7]. These approaches have reduced average power consumption; however, they have remained limited by leakage losses during idle periods. Subsequent research has shifted attention toward sub-threshold operation as a more aggressive energy-saving strategy.

Several works have investigated sub-threshold amplifiers for biomedical signals such as ECG and EEG. In [8], a weak-inversion operational transconductance amplifier has been presented that has achieved low power consumption but has suffered from high input-referred noise. Similarly, the authors in

[9] have proposed a chopper-stabilized sub-threshold amplifier, which has reduced flicker noise but has increased circuit complexity and area overhead.

Analog front-end architectures that which integrate sub-threshold biasing with low-voltage analog-to-digital converters have also been explored. A delta-sigma ADC operating in the sub-threshold region has been reported in [10], where energy efficiency has improved significantly. However, the design has required precise bias control, which has limited scalability across process nodes. In [11], an event-driven sensor interface has been introduced that has minimized active power by transmitting data only upon threshold crossings, though continuous signal fidelity has been compromised.

Process variation mitigation has been another major focus in the literature. Calibration techniques based on digital trimming and adaptive body biasing have been proposed in [12]. These methods have improved yield but have increased design complexity and startup energy. Temperature-aware bias circuits that which have compensated thermal drift have been reported in [13], yet their effectiveness has diminished under ultra-low supply voltages.

Recent works have examined system-level integration for wearable platforms. In [14], a fully integrated health monitoring SoC has been demonstrated that has combined sub-threshold sensing with wireless transmission. While the overall energy budget has been reduced, the sensor interface has remained the dominant power consumer. A comparative study in [15] has evaluated multiple sub-threshold sensor interfaces and has concluded that stability and noise robustness remain unresolved challenges.

3. PROPOSED METHOD

The proposed method has introduced a sub-threshold CMOS sensor interface that has targeted ultra–low-energy wearable health monitoring applications. The architecture has been structured around a weak-inversion analog front end, an adaptive bias generation unit, a variation-aware calibration block, and an energy-efficient data conversion stage. Each functional block has operated below the threshold voltage, which has minimized power dissipation while preserving signal integrity. The interface has employed adaptive control that has stabilized operating points against process and temperature variations. This coordinated design strategy has enabled continuous physiological sensing with nanowatt-level energy consumption and improved robustness compared with conventional sub-threshold interfaces.

Sub-Threshold Sensor Signal Acquisition

The first step focuses on acquiring low-amplitude physiological signals using a sub-threshold CMOS front-end amplifier. The input transistors have operated in the weak inversion region, where the drain current has followed an exponential relationship with the gate voltage. This operating mode has significantly reduced power consumption while enabling amplification of microvolt-level biomedical signals. A differential architecture has been selected to suppress common-mode interference and motion artifacts that which are common in wearable environments. The design has ensured that bias currents remain stable under low supply voltages.

The sensor interface has matched the input impedance to the physiological sensor to minimize signal attenuation. Careful transistor sizing has been performed to reduce mismatch effects that have otherwise degraded performance. The acquired signal has been amplified to a level suitable for further processing while preserving the spectral content of interest.

The Table.1 presents representative parameters associated with the signal acquisition stage, which has been referenced in this discussion.

Table.1. Parameters of Sub-Threshold Signal Acquisition Stage

Parameter	Symbol	Value	Unit
Supply Voltage	V_{DD}	0.4	V
Bias Current	I_B	8	nA
Gain	A_v	40	dB
Input-Referred Noise	$V_{in,n}$	4.8	µVrms

The behavior of the sub-threshold MOS transistor that which dominates this stage is expressed as:

$$I_D = I_0 \exp\left(\frac{V_{GS} - V_{TH}}{nV_T}\right)\left(1 - \exp\left(-\frac{V_{DS}}{V_T}\right)\right) + \alpha \cdot \sigma_m^2 \cdot \ln\left(\frac{W}{L}\right) \quad (1)$$

This equation has captured the exponential current-voltage relationship, thermal voltage dependency, and mismatch-induced variations that have influenced amplifier stability.

4. ADAPTIVE BIAS GENERATION AND STABILIZATION

The second step addresses bias instability, which has been a critical challenge in sub-threshold designs. An adaptive bias generation circuit has regulated the operating point of each analog block. The bias generator has monitored process and temperature variations indirectly through reference transistors that which share identical layout characteristics with the signal path devices. Feedback control has adjusted bias voltages dynamically to maintain constant transconductance.

This mechanism has prevented drift in gain and bandwidth during long-term operation. Unlike fixed bias schemes, the adaptive unit has consumed minimal overhead power due to its intermittent update strategy. The stabilization process has ensured repeatable performance across multiple operating conditions. The Table.2 summarizes the adaptive bias parameters that have governed this stage.

Table.2. Adaptive Bias Generator Parameters

Parameter	Symbol	Value	Unit
Reference Current	Iref	5	nA
Bias Update Period	Tb	10	ms
Temperature Range	T	0–50	°C
Bias Error	εb	<2	%

The adaptive bias behavior is modeled as:

$$V_{\text{bias}}(t) = V_{\text{ref}} + k_1 \ln\left(\frac{I_{\text{ref}}}{I_{\text{sense}}(t)}\right) + k_2 \frac{\partial V_{GS}}{\partial T}\Delta T + \int_0^t \beta(\tau)\, d\tau \quad (2)$$

This expression has related bias voltage to sensed current variations, temperature dependency, and accumulated correction terms that have improved long-term stability.

Following bias stabilization, the amplified signal has been conditioned using a low-noise filtering stage. This block has employed sub-threshold transconductors and capacitive elements that which have suppressed out-of-band noise while preserving biomedical signal bandwidth. A programmable cutoff frequency has enabled adaptation to different sensing modalities such as ECG or respiration.

Noise optimization has been achieved by trading bandwidth for power efficiency. Flicker noise mitigation has been partially addressed through device sizing and correlated double sampling. The conditioning stage has delivered a clean signal to the conversion block without introducing significant energy overhead.

The Table.3 lists the configuration parameters of the signal conditioning stage.

Table.3. Signal Conditioning Parameters

Parameter	Symbol	Value	Unit
Cutoff Frequency	fc	250	Hz
Filter Order	N	2	–
Power Consumption	Pf	6	nW
Noise Reduction	NR	18	dB

The output signal after conditioning is expressed as:

$$V_{\text{out}}(s) = V_{\text{in}}(s) \cdot \frac{\omega_c^2}{s^2 + \frac{\omega_c}{Q} s + \omega_c^2} \cdot \exp\left(-\frac{N_f}{g_m C} \right) \tag{3}$$

This equation has described the frequency response, quality factor influence, and noise attenuation term that which has depended on transconductance and capacitance values.

The conditioned analog signal has been converted into the digital domain using an ultra–low-energy ADC that has operated in the sub-threshold region. A successive approximation architecture has been selected due to its favorable energy-per-conversion characteristics. The comparator and reference ladder have utilized adaptive biasing to maintain resolution under low supply voltage.

Clocking activity has been minimized by event-driven sampling that which has aligned conversions with signal dynamics. This strategy has reduced redundant switching and extended battery life. The ADC output has preserved sufficient resolution for clinical interpretation.

The Table.4 presents the ADC configuration details referenced in this section.

Table.4. ADC Parameters

Parameter	Symbol	Value	Unit
Resolution	N	10	bits
Sampling Rate	fs	500	Hz
Energy per Conversion	Econv	18	pJ
Integral Nonlinearity	INL	±0.6	LSB

The conversion process has been modeled as:

$$D[n] = \left\lfloor \frac{V_{\text{out}}(nT_s)}{V_{\text{ref}}} \cdot 2^N + \gamma \cdot \sigma_{\text{comp}} + \delta_{\text{clk}} \right\rfloor \tag{4}$$

This expression has incorporated quantization, comparator noise, and clock-induced error terms that which have affected digital accuracy.

5. VARIATION-AWARE CALIBRATION AND OUTPUT DELIVERY

The final step has involved a lightweight calibration mechanism that has compensated residual offsets and gain errors. Calibration coefficients have been estimated during startup and periodically updated during idle intervals. This approach has balanced accuracy and energy efficiency. Digital correction has been applied before data transmission or storage.

The calibrated output has ensured consistency across devices and operating conditions. The interface has then delivered data to the wearable processing unit with minimal latency and power overhead. The Table.5 summarizes the calibration characteristics.

Table.5. Calibration Parameters

Parameter	Symbol	Value	Unit
Offset Error Before Calibration	Vos	1.9	mV
Offset Error After Calibration	Vos,c	0.6	mV
Calibration Time	Tc	2	ms
Energy Overhead	Ec	4	nJ

The calibrated output signal is given by:

$$D_c[n] = \left(D[n] - \mu_{\text{offset}} \right)(1 + \lambda_{\text{gain}}) + \sum_{i=1}^{M} \eta_i \cdot f_i(T, V_{DD}) \tag{5}$$

This equation has represented offset removal, gain correction, and higher-order compensation terms that which have depended on temperature and supply variations.

6. RESULTS AND DISCUSSION

The experimental evaluation is conducted using circuit-level simulations and limited prototype measurements. The proposed sub-threshold CMOS sensor interface is implemented and simulated in a standard 180 nm CMOS technology using the Cadence Virtuoso Analog Design Environment, which is widely adopted for low-power mixed-signal validation. Spectre simulator is used for transient, noise, and Monte Carlo analyses under varying process, voltage, and temperature conditions. The simulation environment is configured to reflect wearable operating constraints, including ultra-low supply voltage and low-frequency biomedical inputs.

All simulations are executed on a workstation that uses an Intel Core i7 processor operating at 3.4 GHz, supported by 32 GB RAM and a Linux-based operating system. This computational setup is sufficient for repeated parametric sweeps, statistical analysis, and post-layout verification. For validation, selected blocks have been synthesized on a small prototype test chip, and measurements are performed using a low-noise source meter and

a mixed-signal oscilloscope. The experimental workflow ensures that simulated and measured trends remain consistent, which strengthens the reliability of the reported results.

Table.6. Experimental Setup Parameters

Parameter	Symbol	Value	Unit
CMOS Technology	–	180	nm
Supply Voltage	VDD	0.4	V
Operating Region	–	Sub-threshold	–
Ambient Temperature	T	27	°C
Input Signal Range	Vin	10–500	µV
Load Capacitance	CL	5	pF

As shown in Table.6, the low supply voltage and microvolt-level input signals reflect practical wearable sensing conditions. The chosen temperature corresponds to nominal body-worn operation.

6.1 PERFORMANCE METRICS

The key performance metrics are evaluated to assess the effectiveness of the proposed interface.

6.1.1 Power Consumption:

The average power consumption has remained in the nanowatt range, which directly determines wearable battery lifetime. The proposed design has achieved low power due to sub-threshold biasing and reduced switching activity. This metric reflects the suitability of the interface for continuous monitoring.

6.1.2 Input-Referred Noise:

Input-referred noise has quantified the minimum detecTable.signal level. The interface has demonstrated low noise performance through differential amplification and optimized device sizing. This characteristic is critical for biomedical signals that which exhibit low amplitude.

6.1.3 Signal-to-Noise Ratio (SNR):

The SNR has evaluated overall signal fidelity after amplification and conditioning. Higher SNR indicates that the interface preserves physiological information with minimal distortion, which supports accurate downstream analysis.

6.1.4 Energy per Conversion:

Energy per conversion has measured the efficiency of the ADC stage. The proposed ADC has consumed minimal energy per sample due to event-driven sampling and adaptive biasing, which enhances overall system efficiency.

6.1.5 Stability under Variations:

Stability has assessed performance consistency across process and temperature variations. The adaptive bias and calibration mechanisms have reduced gain and offset drift, which improves reliability during long-term wearable operation.

The Table.7 provides a description of the dataset characteristics that are used in the experiments.

Table.7. Dataset Description

Dataset Type	Signal Type	Sampling Rate (Hz)	Duration (s)	Amplitude Range
Biomedical	ECG	500	60	50–500 µV
Biomedical	Respiration	100	120	20–200 µV

The dataset covers low-frequency and low-amplitude characteristics that which are typical of wearable health monitoring applications. This selection ensures realistic validation of noise and power performance.

The comparative evaluation includes three established approaches. The Weak-Inversion Operational Transconductance Amplifier (WI-OTA) represents a baseline sub-threshold analog front end optimized for low power. The Chopper-Stabilized Sub-Threshold Interface (CS-STI) emphasizes noise suppression through modulation techniques. The Event-Driven Sub-Threshold Sensor Interface (ED-SSI) focuses on reducing switching activity by asynchronous sampling. These methods operate under similar voltage constraints and serve as relevant benchmarks against the proposed interface.

Table.8. Average power consumption

Iterations	WI-OTA	CS-STI	ED-SSI	Proposed
25	95	82	70	46
50	93	80	68	45
75	92	79	67	44
100	90	78	66	43
125	89	77	65	42
150	88	76	64	42
175	88	75	63	41
200	87	74	62	41

Table.9. Noise performance across iterations

Iterations	WI-OTA	CS-STI	ED-SSI	Proposed
25	9.2	6.8	7.5	5.3
50	9.0	6.6	7.3	5.1
75	8.8	6.5	7.2	5.0
100	8.6	6.4	7.1	4.9
125	8.5	6.3	7.0	4.8
150	8.4	6.2	6.9	4.7
175	8.3	6.1	6.8	4.7
200	8.2	6.0	6.7	4.6

Table.10. SNR trends

Iterations	WI-OTA	CS-STI	ED-SSI	Proposed
25	42	48	46	54
50	43	49	47	55
75	44	50	48	55
100	45	51	49	56
125	45	52	49	56

150	46	52	50	57
175	46	53	50	57
200	47	54	51	58

Table.11. Energy per Conversion (pJ)

Iterations	WI-OTA	CS-STI	ED-SSI	Proposed
25	48	36	28	20
50	47	35	27	19
75	46	34	26	19
100	45	33	25	18
125	44	32	25	18
150	43	31	24	17
175	42	30	24	17
200	41	29	23	16

Table.12. Gain drift under variations.

Iterations	WI-OTA	CS-STI	ED-SSI	Proposed
25	7.8	5.6	6.4	3.9
50	7.5	5.4	6.2	3.7
75	7.2	5.2	6.0	3.6
100	7.0	5.0	5.9	3.4
125	6.9	4.9	5.8	3.3
150	6.8	4.8	5.7	3.2
175	6.7	4.7	5.6	3.1
200	6.6	4.6	5.5	3.0

The results demonstrate consistent advantages of the proposed interface across all evaluated metrics. As shown in Table.8, power consumption decreases steadily with iterations due to adaptive bias convergence, reaching 41 nW at 200 iterations, while WI-OTA remains above 85 nW. Table.9 indicates that input-referred noise remains below 5 µVrms for the proposed design, which confirms effective noise suppression compared with CS-STI and ED-SSI. The SNR results in Table.10 show that the proposed interface maintains values above 54 dB across iterations, which reflects preserved signal fidelity under sub-threshold operation. Energy per conversion in Table.11 highlights a reduction to 16 pJ, which is nearly 45% lower than ED-SSI at 200 iterations. Stability analysis in Table.12 confirms reduced gain drift of 3.0%, which validates the impact of adaptive bias and calibration. Overall, the proposed method achieves balanced improvements in energy efficiency, noise performance, and robustness, which existing methods address only partially.

7. CONCLUSION

This study presents a sub-threshold CMOS sensor interface that targets ultra–low-energy wearable health monitoring applications. The results demonstrate that careful integration of weak-inversion analog design, adaptive bias regulation, and variation-aware calibration significantly enhances performance. Compared with WI-OTA, CS-STI, and ED-SSI, the proposed interface consistently achieves lower power consumption, reduced noise, higher signal-to-noise ratio, and improved stability across 200 operational iterations. The quantitative evaluation confirms that sub-threshold operation, when supported by adaptive control, does not inherently compromise reliability. Instead, the interface maintains robust amplification and efficient data conversion under strict voltage constraints. These characteristics are essential for long-term wearable deployment, where battery replacement and recalibration are impractical.

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