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FPGA-ACCELERATED LTE-M FRAMEWORK FOR LOW-LATENCY OPTIMIZATION IN 5G PHYSICAL CHANNEL COMBINATION WITH 4G LTE NETWORKS

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Abstract

The growing demand for high-speed, low-latency communication in next-generation wireless systems has driven the convergence of 4G LTE and 5G technologies. However, integrating 5G physical channels with existing LTE infrastructures presents a significant challenge due to inherent latency and bandwidth limitations in conventional baseband processing architectures. This study addresses these limitations by developing a Field-Programmable Gate Array (FPGA)-based LTE-M (LTE for Machines) acceleration framework that optimizes latency and enhances signal processing efficiency in hybrid 4G–5G networks. The proposed architecture leverages parallelized hardware design and reconfigurable logic to execute key baseband functions including modulation, demodulation, and channel coding at significantly higher throughput compared to traditional DSP or CPU-based systems. The design incorporates adaptive pipelining and low-complexity scheduling techniques to minimize processing delays in the physical layer, ensuring seamless support for Machine-Type Communication (MTC) and IoT-based applications over LTE-M channels. Experimental validation of the FPGA-based LTE-M framework showed a 37% reduction in end-to-end latency and a 42% improvement in throughput, with BER decreasing by 50% compared to conventional methods. In addition, FPGA resource utilization was optimized by 10–15%, and power consumption decreased by 30%, which shows both high performance and energy efficiency for hybrid 4G–5G network combination.

Keywords:

FPGA Acceleration, LTE-M, 5G Physical Channel, Latency Reduction, Hybrid 4G–5G Combination

1. INTRODUCTION

The evolution of wireless communication technologies has seen a significant shift from 4G LTE to 5G, driven by the need for higher data rates, reduced latency, and increased connectivity. In this context, LTE-M (Machine Type Communication) has emerged as a pivotal technology, bridging the gap between 4G and 5G networks, particularly for IoT applications. However, the combination of 5G physical channels into existing 4G LTE infrastructures presents challenges that need to be addressed to realize the full potential of 5G technologies.

One of the primary challenges in this combination is the inherent latency present in the 4G LTE physical layer, which can hinder the performance of 5G applications that demand ultra-reliable low-latency communication (URLLC). Traditional software-based processing units struggle to meet the stringent latency requirements of 5G systems, necessitating the exploration of hardware-based solutions. Field-Programmable Gate Arrays (FPGAs) have been identified as a promising solution due to their parallel processing capabilities and reconfigurability, allowing for the acceleration of baseband processing tasks and the reduction of latency in the physical layer.

Despite the advancements in FPGA technology, the combination of FPGA-based LTE-M frameworks for latency reduction in 5G physical channels within 4G LTE networks remains underexplored. Existing studies have primarily focused on individual aspects of this combination, such as modulation schemes or synchronization processes, without providing a comprehensive solution that addresses the end-to-end latency reduction in the physical layer.

The primary objectives of this research are:

- To design and implement an FPGA-based LTE-M framework that facilitates the combination of 5G physical channels into 4G LTE networks.
- To optimize the latency in the physical layer by leveraging FPGA's parallel processing capabilities.

This research introduces a novel approach by integrating FPGA-based LTE-M frameworks to address the latency challenges in the physical layer when incorporating 5G physical channels into 4G LTE networks. The novelty lies in the comprehensive design that encompasses modulation, demodulation, channel coding, and synchronization processes, all optimized for low-latency performance.

Contributions

- The development of a comprehensive FPGA-based framework that integrates LTE-M functionalities with 5G physical channels, facilitating seamless communication between 4G and 5G networks.
- The implementation of advanced latency reduction techniques, including parallel processing and pipelining, to enhance the performance of the physical layer in hybrid 4G–5G networks.

2. METHODS

The proposed framework integrates FPGA-based acceleration into LTE-M networks to reduce latency in 5G physical channels while maintaining compatibility with 4G LTE networks. The methodology is divided into several key functional blocks, each optimized for low-latency operation.

2.1 FPGA-BASED MODULATION AND DEMODULATION

The first step in the proposed system involves the modulation and demodulation of the LTE-M signals on the FPGA. The system leverages hardware parallelism to process multiple modulation

symbols simultaneously, thereby reducing the processing time compared to conventional CPU-based processing.

The modulation process maps input binary data into complex symbols, following M-QAM or QPSK schemes depending on channel requirements. The FPGA implementation performs this mapping in a parallelized pipeline, allowing multiple symbols to be processed concurrently.

The demodulation process involves detecting the transmitted symbols from the received waveform. Here, FPGA resources are used to implement maximum likelihood or minimum mean square error (MMSE) estimators efficiently. Symbol Mapping (Modulation):

$$s_k = \sum_{n=0}^{N-1} x_n e^{-j2\pi kn/N}, \quad k = 0,1,\ldots,N-1 \tag{1}$$

where s_k represents the modulated symbol, x_n is the input bit stream, and N is the modulation order.

Table.1. FPGA Resource Allocation for Modulation/Demodulation

Resource Type	Utilization (%)	Latency (ns)	Throughput (Mbps)
LUTs	72	12	980
DSP Slices	65	15	1020
BRAM	50	10	950

The Table.1 illustrates the FPGA resource allocation and achieved throughput for modulation and demodulation tasks.

2.2 CHANNEL CODING AND DECODING

Channel coding ensures data integrity over noisy channels, which is critical in LTE-M and 5G systems. In the proposed framework, Turbo codes and LDPC codes are implemented on the FPGA to provide robust error correction. Hardware pipelining allows encoding and decoding operations to execute concurrently, further minimizing latency.

The FPGA architecture enables multiple decoding cores to run in parallel, each handling a subset of the incoming data stream. This ensures that throughput remains high while reducing the Thus end-to-end processing delay.

Turbo Code Decoding (Log-MAP Algorithm):

$$L(u_k) = \ln \frac{P(u_k = 1 \mid y)}{P(u_k = 0 \mid y)} = \max_{s',s} \left[\alpha_{k-1}(s') + \gamma_k(s',s) + \beta_k(s) \right] \tag{2}$$

where, $L(u_k)$ is the log-likelihood ratio of the k^{th} bit, α and β represent forward and backward state metrics, and γ_k is the branch metric computed using received symbols y.

Table.2. Latency and Throughput for Channel Coding

Coding Scheme	FPGA Core Count	Latency (ns)	Bit Error Rate (BER)
Turbo Code	4	18	1e-5
LDPC Code	6	22	8e-6

The Table.2 summarizes the latency and error performance for different coding schemes implemented on FPGA.

2.3 PHYSICAL LAYER SYNCHRONIZATION

Accurate synchronization between transmitter and receiver is essential for LTE-M and 5G combination. The proposed system employs FPGA-based timing recovery and frequency offset correction to align incoming data streams with minimal delay.

The FPGA implementation utilizes parallel correlators for pilot symbol detection and timing alignment. Frequency offset estimation is performed using a hardware-accelerated FFT, which reduces the time needed for phase correction.

Timing and Frequency Offset Correction:

$$y[n] = x[n]e^{j(2\pi \Delta f n T_s + \phi)} + w[n] \tag{3}$$

where $y[n]$ is the received signal, $x[n]$ is the transmitted symbol, Δf is the frequency offset, T_s is the sampling interval, ϕ is the phase offset, and $w[n]$ is additive noise.

Table.3. Synchronization Performance

Metric	Value	Improvement (%)
Timing Error (ns)	3.5	42
Frequency Offset (Hz)	12	35
Latency (ns)	15	37

The Table.3 presents the synchronization accuracy and latency improvements achieved using FPGA.

3. ADAPTIVE PIPELINING AND SCHEDULING

The proposed framework incorporates adaptive pipelining to overlap different processing stages and low-complexity scheduling for efficient resource utilization. This ensures continuous data flow without stalling, which is critical for low-latency applications.

The FPGA schedules multiple tasks dynamically, adjusting pipeline stages based on input load and processing conditions. This reduces idle cycles and maximizes throughput.

Pipeline Throughput Estimation:

$$T_{eff} = \frac{N}{\sum_{i=1}^{M} \left(\frac{1}{f_i} + t_{comm,i} \right)} \tag{4}$$

where, T_{eff} is the effective throughput, Nis the number of processed symbols, M is the number of pipeline stages, f_i is the processing frequency of stage i, and $t_{comm,i}$ is the communication latency between stages.

Table.4. Pipeline Stage Performance

Stage	Frequency (MHz)	Latency (ns)	Utilization (%)
Modulation	300	12	70
Channel Coding	250	18	65
Synchronization	200	15	60
Scheduling	150	10	50

The Table.4 shows the frequency, latency, and utilization of different FPGA pipeline stages. Finally, the system performance is evaluated using a hardware-in-the-loop testbed that integrates all the aforementioned modules. FPGA resource usage, latency, throughput, and power consumption are measured and compared with conventional software-based systems.

The framework shows significant reductions in end-to-end latency, while improving throughput and power efficiency. By integrating modulation, channel coding, synchronization, and adaptive scheduling into a unified FPGA platform, the system achieves consistent low-latency operation suitable for LTE-M and 5G physical layer combination.

End-to-End Latency Calculation:

$$L_{total} = \sum_{i=1}^{N_m} (L_i + t_{queue,i}) \quad (5)$$

where L_i is the latency of module i and $t_{queue,i}$ is the queuing delay between modules.

Table.5. System Performance

Metric	FPGA-Based System	Software-Based System	Improvement (%)
End-to-End Latency (ns)	60	95	37
Throughput (Mbps)	1020	720	42
Power Consumption (W)	18	26	30

The Table.5 compares the Thus system performance between FPGA-based and conventional implementations.

4. RESULTS AND DISCUSSION

The proposed FPGA-based LTE-M framework was evaluated through a combination of simulation and hardware-in-the-loop experiments. The MATLAB/Simulink 5G Toolbox was primarily used to model and simulate the 5G physical layer over LTE-M channels, including modulation, coding, and synchronization modules. FPGA-specific implementation and acceleration were tested using Xilinx Vivado 2023.1 on a Zynq UltraScale+ MPSoC development board, providing reconfigurable hardware to measure latency, throughput, and resource utilization.

During simulations, realistic LTE-M traffic and channel models were generated, including AWGN and multipath fading scenarios, to emulate practical wireless environments. All experiments were executed on a high-performance workstation equipped with an Intel Core i9-13900K CPU, 64 GB RAM, and a NVIDIA RTX 4090 GPU, enabling efficient MATLAB simulations and verification of FPGA synthesis results.

Table.6. Experimental Parameters

Parameter	Value / Setting	Description
Carrier Frequency	2.4 GHz	LTE-M/5G channel frequency
Bandwidth	1.4 MHz (LTE-M)	Channel bandwidth
Modulation Scheme	QPSK, 16-QAM	Symbol mapping scheme
Coding Scheme	Turbo, LDPC	Channel coding technique
FFT Size	128	Number of points for OFDM
FPGA Board	Zynq UltraScale+ MPSoC	Hardware platform for implementation
Clock Frequency	300 MHz	FPGA operating frequency
Number of Pipeline Stages	4	Modulation, coding, synchronization, scheduling
Simulation Tool	MATLAB/Simulink 5G Toolbox	Software simulation environment
Channel Model	AWGN + Rayleigh Fading	Wireless channel model

The Table.6 summarizes the experimental parameters used in both simulation and FPGA-based evaluation of the proposed LTE-M framework.

4.1 PERFORMANCE METRICS

To quantify the performance of the proposed system, five key metrics were evaluated:

- **End-to-End Latency**: This metric measures the total delay from transmission to reception of a packet, including processing, synchronization, and queuing delays. FPGA acceleration significantly reduced latency compared to software-based processing.
- **Throughput**: Defined as the number of bits successfully transmitted per second, throughput was measured across different modulation and coding schemes. Parallel processing on FPGA led to higher throughput and better resource utilization.
- **Bit Error Rate (BER)**: BER evaluates the reliability of data transmission by calculating the fraction of erroneous bits. LDPC and Turbo coding on FPGA reduced BER under AWGN and multipath fading conditions.
- **Resource Utilization**: This metric monitors the usage of FPGA resources such as LUTs, DSP slices, and BRAM, which determines the efficiency of hardware implementation. Efficient pipelining and adaptive scheduling optimized utilization.
- **Power Consumption**: Power efficiency was measured in Watts for the FPGA board under full load conditions. The hardware-accelerated framework consumed less power compared to equivalent software-based systems while achieving latency and throughput improvements.

4.2 PERFORMANCE OVER VARIOUS SCHEMES

The performance of the proposed FPGA-based LTE-M framework was evaluated against three existing methods: FPGA-based baseband modulator, SmartNIC FPGA architecture for 5G DU Low-PHY, and Physical layer latency management in 5G NR

systems. Each metric was measured over QPSK and 16-QAM modulation schemes.

Table.7. End-to-End Latency Comparison (ns)

Method / Scheme	QPSK	16-QAM
FPGA-based baseband modulator	92	105
SmartNIC FPGA architecture for 5G DU Low-PHY	88	102
Physical layer latency management in 5G NR	95	110
Proposed Method	60	70

The Table.7 shows that the proposed method reduces latency by 30–40% compared to existing methods across both QPSK and 16-QAM.

Table.8. Throughput Comparison (Mbps)

Method / Scheme	QPSK	16-QAM
FPGA-based baseband modulator	720	800
SmartNIC FPGA architecture for 5G DU Low-PHY	750	820
Physical layer latency management in 5G NR	710	790
Proposed Method	1020	980

The Table.8 illustrates that FPGA-based acceleration significantly improves throughput for both modulation schemes.

Table.9. BER Comparison

Method / Scheme	QPSK	16-QAM
FPGA-based baseband modulator	2e-5	4e-5
SmartNIC FPGA architecture for 5G DU Low-PHY	1.8e-5	3.8e-5
Physical layer latency management in 5G NR	2.2e-5	4.2e-5
Proposed Method	1e-5	2e-5

The Table.9 shows that the proposed framework achieves lower BER, reflecting higher reliability under both QPSK and 16-QAM.

Table.10. FPGA Resource Utilization (%)

Method / Scheme	LUTs	DSP Slices	BRAM
FPGA-based baseband modulator	75	68	55
SmartNIC FPGA architecture for 5G DU Low-PHY	72	65	52
Physical layer latency management in 5G NR	78	70	58
Proposed Method	70	65	50

The Table.10 indicates that the proposed method uses FPGA resources more efficiently while improving performance.

Table.11. Power Consumption Comparison (W)

Method / Scheme	QPSK	16-QAM
FPGA-based baseband modulator	25	27
SmartNIC FPGA architecture for 5G DU Low-PHY	24	26
Physical layer latency management in 5G NR	26	28
Proposed Method	18	20

The Table.11 shows that the proposed FPGA-based framework consumes significantly lower power than existing methods.

The results indicate that the proposed FPGA-based LTE-M framework outperforms existing methods across all metrics. End-to-end latency is reduced by 30–40% (Table.7), while throughput is increased by 25–30% (Table.8), showing the benefit of hardware acceleration. BER is reduced nearly 50% (Table.9), reflecting enhanced reliability under QPSK and 16-QAM schemes. FPGA resource utilization is optimized (Table.10), ensuring hardware efficiency, and power consumption is lowered by 20–30% (Table.11), supporting energy-efficient deployment.

4.3 PERFORMANCE OVER CHANNEL MODELS

The system performance was evaluated under three channel conditions: AWGN, Rayleigh Fading, and AWGN + Rayleigh Fading, and compared with FPGA-based baseband modulator, SmartNIC FPGA architecture for 5G DU Low-PHY, and Physical layer latency management in 5G NR systems.

Table.12. End-to-End Latency Comparison (ns)

Method / Channel Model	AWGN	Rayleigh Fading	AWGN + Rayleigh
FPGA-based baseband modulator	90	105	112
SmartNIC FPGA architecture for 5G DU Low-PHY	88	102	110
Physical layer latency management in 5G NR	95	108	115
Proposed Method	60	70	75

The Table.12 shows that the proposed method achieves 30–40% lower latency compared to existing methods across all channel types.

Table.13. Throughput Comparison (Mbps)

Method / Channel Model	AWGN	Rayleigh Fading	AWGN + Rayleigh
FPGA-based baseband modulator	730	680	650
SmartNIC FPGA architecture for 5G DU Low-PHY	750	700	670
Physical layer latency management in 5G NR	710	660	640
Proposed Method	1020	980	940

The Table.13 shows that the proposed FPGA framework maintains higher throughput under all channel conditions.

Table.14. BER Comparison

Method / Channel Model	AWGN	Rayleigh Fading	AWGN + Rayleigh
FPGA-based baseband modulator	1.8e-5	3.2e-5	3.5e-5
SmartNIC FPGA for 5G DU Low-PHY	1.5e-5	3e-5	3.3e-5
Physical layer latency management in 5G NR	2e-5	3.5e-5	3.8e-5
Proposed Method	1e-5	2e-5	2.2e-5

The Table.14 indicates that the proposed method significantly reduces BER, especially under combined AWGN + Rayleigh fading conditions.

Table.15. FPGA Resource Utilization (%)

Method / Channel Model	LUTs	DSP Slices	BRAM
FPGA-based baseband modulator	75	68	55
SmartNIC FPGA for 5G DU Low-PHY	72	65	52
Physical layer latency management in 5G NR	78	70	58
Proposed Method	70	65	50

The Table.15 shows the proposed method uses lower FPGA resources while supporting reliable performance across all channel types.

Table.16. Power Consumption Comparison (W)

Method / Channel Model	AWGN	Rayleigh Fading	AWGN + Rayleigh
FPGA-based baseband modulator	25	27	28
SmartNIC FPGA for 5G DU Low-PHY	24	26	27
Physical layer latency management in 5G NR	26	28	29
Proposed Method	18	20	21

The Table.16 shows the energy efficiency of the proposed framework under various channel conditions.

The results demonstrate that the proposed FPGA-based LTE-M framework consistently outperforms existing methods across all channel conditions. End-to-end latency decreases by 30–40% (Table.12), while throughput improves by 25–35% (Table.13). BER is reduced nearly 40–50% under Rayleigh and combined AWGN + Rayleigh fading (Table.14), indicating enhanced reliability. FPGA resource usage remains lower (Table.15), ensuring efficient hardware utilization, and power consumption is reduced by 20–30% (Table.16), supporting energy-efficient deployment.

4.4 PERFORMANCE OVER CODING SCHEMES

The system performance was evaluated under two channel coding schemes: Turbo and LDPC, and compared with FPGA-based baseband modulator, SmartNIC FPGA architecture for 5G DU Low-PHY, and Physical layer latency management in 5G NR systems.

Table.17. End-to-End Latency Comparison (ns)

Method / Coding Scheme	Turbo	LDPC
FPGA-based baseband modulator	92	100
SmartNIC FPGA for 5G DU Low-PHY	88	97
Physical layer latency management in 5G NR	95	105
Proposed Method	60	68

The Table.17 shows that the proposed framework reduces latency by approximately 30–35% for both Turbo and LDPC coding schemes.

Table.18. Throughput Comparison (Mbps)

Method / Coding Scheme	Turbo	LDPC
FPGA-based baseband modulator	720	750
SmartNIC FPGA for 5G DU Low-PHY	750	780
Physical layer latency management in 5G NR	710	740
Proposed Method	1020	980

The Table.18 shows that the proposed FPGA-based framework maintains higher throughput across both coding schemes.

Table.19. BER Comparison

Method / Coding Scheme	Turbo	LDPC
FPGA-based baseband modulator	2e-5	1.5e-5
SmartNIC FPGA for 5G DU Low-PHY	1.8e-5	1.3e-5
Physical layer latency management in 5G NR	2.2e-5	1.6e-5
Proposed Method	1e-5	8e-6

The Table.19 indicates that the proposed method significantly reduces BER, with LDPC coding showing the highest reliability improvement.

Table.20. FPGA Resource Utilization (%)

Method / Coding Scheme	LUTs	DSP Slices	BRAM
FPGA-based baseband modulator	75	68	55
SmartNIC FPGA	72	65	52

for 5G DU Low-PHY			
Physical layer latency management in 5G NR	78	70	58
Proposed Method	70	65	50

The Table.20 shows that the proposed framework uses lower FPGA resources while maintaining high-performance coding capabilities.

Table.21. Power Consumption Comparison (W)

Method / Coding Scheme	**Turbo**	**LDPC**
FPGA-based baseband modulator	25	27
SmartNIC FPGA for 5G DU Low-PHY	24	26
Physical layer latency management in 5G NR	26	28
Proposed Method	18	20

The Table.21 shows that the proposed FPGA-based framework reduces power consumption by 20–30%, making it energy efficient.

The results confirm that the proposed FPGA-based LTE-M framework outperforms existing methods across both Turbo and LDPC coding schemes. End-to-end latency decreases by 30–35% (Table.17), and throughput increases by 25–35% (Table.18). BER is reduced nearly 50–60% for LDPC and 45–50% for Turbo coding (Table.19), reflecting superior reliability. FPGA resource utilization remains optimized (Table.20), and power consumption is lowered by 20–30% (Table.21).

5. CONCLUSION

This study presents an FPGA-based LTE-M framework designed to reduce latency and enhance performance in 5G physical channel combination with existing 4G LTE networks. The proposed framework leverages parallelized hardware acceleration for modulation, demodulation, channel coding, synchronization, and adaptive pipelining, resulting in a comprehensive low-latency architecture. Experimental evaluations under various modulation schemes (QPSK, 16-QAM), coding schemes (Turbo, LDPC), and channel models (AWGN, Rayleigh Fading, AWGN + Rayleigh) demonstrate significant improvements over existing methods. Specifically, the framework achieved a 37% reduction in end-to-end latency, a 42% increase in throughput, and a 50% decrease in BER, while maintaining efficient FPGA resource utilization and reducing power consumption by 30%. Comparative analysis with Lopes Ferreira et al., Borromeo et al., and Marinšek et al. validates the superior performance of the proposed design across all tested conditions. These results highlight the framework's capability to support ultra-reliable low-latency communication and IoT-based applications in hybrid 4G–5G networks. Thus, the study provides a scalable, energy-efficient, and high-performance solution that bridges the gap between 4G LTE infrastructures and emerging 5G deployments, offering a practical pathway for future wireless communication systems.

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