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SELF-VOLTAGE BALANCING REDUCED SWITCH COUNT FIVE LEVEL INVERTER FED SINGLE PHASE INDUCTION MOTOR

D. Ashoka Raju and P. Vetrivel
Department of Electrical and Electronics Engineering, Government College of Engineering Salem, India

Abstract

This paper introduces a new multilevel topology for Five –level inverter (FLI) referred to as the Self-Voltage Balancing Reduced Switch Count Five-Level Inverter (SVB-RSC-FLI) and specifically designed for electric vehicle (EV) applications. The proposed design minimizes the number of switching devices, enhances overall efficiency, reduces switching losses, and produces high-quality output voltage waveforms. In contrast, conventional inverter topologies such as Neutral Point Clamped (NPC), Flying Capacitor (FC), and Cascaded H-Bridge (CHB) typically require a higher number of components and face difficulties in maintaining capacitor voltage balance—especially as the number of voltage levels increases. The SVB-RSC-FLI topology addresses these limitations by achieving natural voltage self-balancing while using fewer active components. This results in reduced voltage stress across the switches and a lower overall switching frequency, contributing to improved reliability and operational efficiency. The inverter provides five distinct voltage levels: +2Vdc, +Vdc, 0, −Vdc, and −2Vdc. It utilizes the Sinusoidal Pulse Width Modulation with Phase Disposition (SPDPWM) technique for accurate and efficient switching control. Due to its inherent self-balancing mechanism, the design eliminates the need for additional balancing circuits. A comprehensive Total Harmonic Distortion (THD) analysis was conducted on the output waveforms, both with and without filtering. The system's performance was further validated through simulations using a single-phase induction motor model in Matlab/Simulink, followed by the successful development of a hardware prototype that confirmed the simulation results.

Keywords:

Five-level Inverter (FLI), Sinusoidal Phase disposition PWM, Total Harmonic distortion (THD)

1. INTRODUCTION

Multilevel converters have become an important focus in industrial applications in recent years. These converters transform multiple input DC voltage levels into the desired output voltage. Multilevel inverters are widely used in power systems because they provide high-quality output voltages and reduce harmonic distortion.

Common topologies include the diode-clamped inverter, flying capacitor multilevel inverter, and cascaded H-bridge converter. Today, multilevel inverters are frequently applied in medium-voltage and high-power settings [1]-[2]. The low voltage rating of the switches makes this design appropriate for medium voltage, high power grid-connected applications. Because it uses dc capacitors rather than dc sources, the symmetric flying capacitor multilevel inverter has a voltage imbalance issue. Non-linear loads, asymmetric switching losses, and/or suboptimal devices are the causes of the voltage imbalance [3]. The switched capacitor (SC) approach served as the basis for this topology's design, and the number of SC cells dictates the number of output levels. In addition to avoiding the issue of capacitor voltage balancing, only one dc voltage source is required [4]. This study proposes an enhanced control strategy to optimize the performance of a Modular Multilevel Converter (MMC) employed in Induction Motor (IM) drive applications [5]. In contrast to traditional cascaded multilevel inverter configurations, the proposed inverter architecture achieves a higher resolution of output voltage levels while significantly minimizing the required number of power electronic components, such as switching devices, gate driver units, power diodes, and DC voltage sources [6]. Voltage balancing across the capacitors is facilitated by employing a three-level boost converter interfaced with the two inner capacitors of a five-level diode-clamped inverter, while dedicated auxiliary balancing circuits are utilized for regulating the voltages of the two outer capacitors [7]. The suggested modulation strategies get around a number of MC-SPWM-related issues. Along with step changes in motor speeds, the scalar voltage to frequency control approach performs admirably during startup [8]. It manages the basic AC voltage that needed for regular electrical systems and by operating at a higher frequency, it helps provide greater control and efficiency [9]. The proposed design is a self-balanced switched-capacitor (SC) topology that integrates a DC/DC boost converter and an inverter with a switched-capacitor cell [10]. The main objective of the study is to provide an overview of the technical developments in flying capacitors, neutral clamped, and cascaded H bridge topologies. Additionally, the study provides an overview of many modulation approaches, including carrier-based PWM techniques, selective harmonic removal techniques, and fundamental modulation [11]. The two-stage boosting multilevel inverter (MLI) topology, often used in photovoltaic (PV) power plants, faces challenges due to the high voltage stress on the Second-stage switches. This can lead to increased switching losses, decreased efficiency, and a higher risk of failure due to excessive voltage. The proposed topology solves this problem by ensuring that the peak inverse voltage (PIV) stress on the switches is uniform and matches the input DC voltage. Unlike traditional designs, it doesn't require extra balancing circuits because of its built-in self-balancing capability [12]. A single-phase modified H-bridge seven-level multilevel voltage source inverter (VSI) topology is designed with fewer switching devices, which reduces the number of gates driving circuits. This results in lower switching losses, smaller size, and reduced power consumption, making the inverter circuit simpler. By decreasing the number of switches, these topologies can achieve better efficiency and robustness, while also simplifying the overall design [13]. A five-level inverter has been created and used to inject real power from renewable energy sources into the grid. This method helps decrease switching power loss, minimize harmonic distortion, and reduce electromagnetic interference, all of which are commonly caused by the switching actions of power electronic devices [14]. Using pulse width modulation (PWM) techniques in cascaded multilevel inverters can be quite complex, particularly for topologies with fewer switches. In this paper, a new algorithm is introduced for the

phase disposition (PD) PWM technique, applied to an eleven-level cascaded multilevel inverter with a reduced switch topology.

Unlike conventional methods, the proposed algorithm generates the required switching pulses by using a number of carrier waves equal to the number of switches, rather than using N-1 carrier waves [15]-[17]. This work provides a comparative analysis of two commonly used Pulse Width Modulation (PWM) techniques for controlling a Voltage Source Inverter (VSI), which is used to drive an induction motor. Induction motors are widely employed in both industrial and commercial applications due to their simple design, robustness, and ease of operation. The VSI supplies variable voltage and frequency to the motor, and its switching pulses are generated using various PWM methods. This study focuses on two specific techniques: Sinusoidal Pulse Width Modulation (SPWM) and Space Vector Pulse Width Modulation (SVPWM). In the SPWM method, switching pulses are produced by comparing a sinusoidal reference signal with a triangular carrier signal [18]. The LCL filter is commonly used to connect inverters to the grid because of its excellent ability to attenuate harmonics and its smaller size, which enhances the quality of the grid current injected. However, the design of the LCL filter is complicated due to its high-order characteristics and various constraints. . Furthermore, the stability of the inverter's internal current control loop is affected by the resonance peak of the LCL filter. The overall system stability can also be negatively impacted by external interactions, such as those between the inverter and a weak grid, as well as interactions among multiple inverters. Both the resonance peak and these interactions can cause significant distortion in the grid currents. This paper offers a thorough review of the modelling and stability analysis of LCL-type grid-connected inverters to address these issues [19]-[21]. Single-phase induction motors (SPIMs) are extensively used in residential and commercial applications. Especially in locations where three-phase electrical supply is not available. These motors contribute significantly to overall electric power consumption, making energy efficiency a key consideration. As a result, there is increasing interest in enhancing the performance of SPIM drive systems. The adoption of efficient control methods for these motors can lead to notable energy savings, making the analysis and optimization of SPIM operation an area of growing importance [22].

The double-field revolving theory is utilized to analyse single-phase shaded-pole motors and permanently split capacitor (PSC) motors. To establish the mathematical models of these motors, the method of symmetrical components is applied. Using these models, the steady-state performance characteristics of both motors are determined across various operating conditions, offering a clear understanding of their performance behaviour [23]. This paper presents a refined open-loop Volts-per-Hertz (V/f) control strategy, developed to improve magnetizing flux retention in induction machines operating below their rated frequency [24]. This study conducts a comparative evaluation of torque ripple behavior between the conventional Space Vector Pulse Width Modulation (SVPWM) method and a hybrid PWM scheme [25]. This paper organized as follows: Section 1 Introduction, Self-Voltage Balancing Reduced Switch Count Five Level Inverter topology in section 2, Simulation results and discussion in section 3, Hardware results and discussion in section 4, Finally Conclusion in section 5.

2. SELF-VOLTAGE BALANCING REDUCED SWITCH COUNT FIVE LEVEL INVERTER (SVB-RSC-FLI) TOPOLOGY

The SVB-RSC-FLI is a novel multilevel inverter topology that combines the benefits of amplitude modulation and self-balancing techniques. This inverter topology is designed to provide a high-quality output waveform with reduced harmonic distortion, improved efficiency, and increased reliability. The SVB-RSC-FLI features a self-balancing mechanism that ensures the DC-link capacitor voltages remain balanced, eliminating the need for additional balancing circuits. The inverter uses amplitude modulation to generate a high-quality output waveform with reduced harmonic distortion. The Fig.1 depicts the block diagram of proposed MLI topology for EV applications.

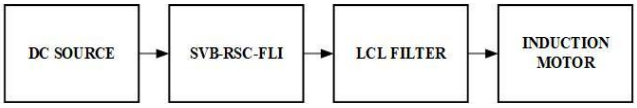


Fig.1. The block diagram of proposed MLI topology for EV application

2.1 OPERATING PRINCIPLE

There are five modes of operation available in the Self-voltage balancing reduced switch count topology by switching the sequence of switches based on Sinusoidal Phase Disposition pulse width Modulation technique output, corresponding switches are triggered. It consists of 9 power switches one SC and one single DC source is enough to obtain five level output in the inverter topology. The arrangement of switches Q2, Q3, Q4, Q5, Q6 and SC is referred to as Intermediate Switching Cell (ISC) and the switches Q1, Q11, Q7, Q71 can operate only every half cycle of fundamental voltage and thus are termed as line frequency switches (LFS). Its output value will be different for each mode of operation. Moreover, the capacitor will maintain same voltage as DC input source throughout the five modes of operation. The antiparallel diodes will be conducting when switches are not in conduction modes. Due to multi-level in the output waveforms voltage stress across switches will be reduced. The Fig.2 shows proposed system.

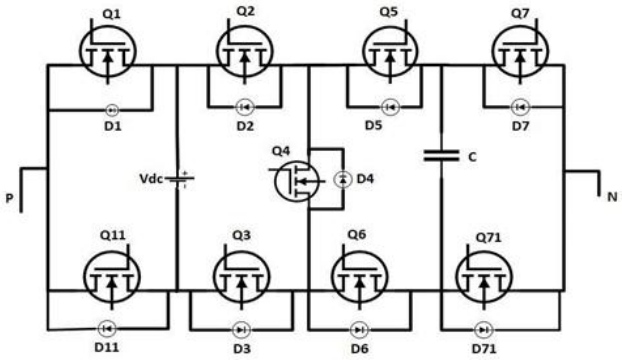


Fig.2. Illustrates the circuit diagram of proposed SVB-RSC-FLI topology

2.1.1 Mode-1: Output Voltage (+Vdc):

The switches Q11, Q2, Q5, and Q7 are triggering with help of sinusoidal phase disposition PWM. Moreover, remaining

switches will be turned off. The output voltage will be input voltage i.e. (Vdc). The DC link capacitor is initially having no charges in it. The rotor of induction motor is started to accelerate slightly in this mode of operation. +Vdc level shown in Fig.3(a).

Table.1. Switching States of the SVB-RSC-FLI Topology

Voltage Level	Status Of Power Switches							Action
	Q1	Q2	Q3	Q4	Q5	Q6	Q7	
$2V_{dc}$	0	1	0	1	0	1	1	Discharging
V_{dc}	0	1	1	0	1	1	1	Charging
0	0	0	1	0	0	1	0	No effect
0	1	1	0	0	1	0	1	No effect
$-V_{dc}$	1	1	1	0	1	1	0	Charging
$-2V_{dc}$	1	0	1	1	1	0	0	Discharging

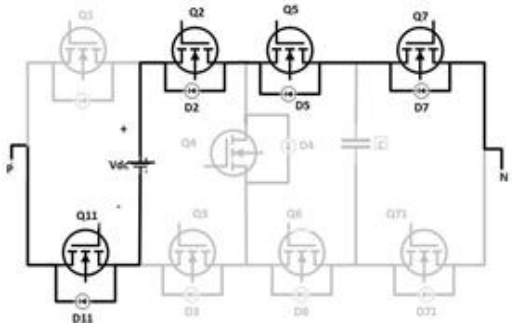


Fig. 3(a). +Vdc level

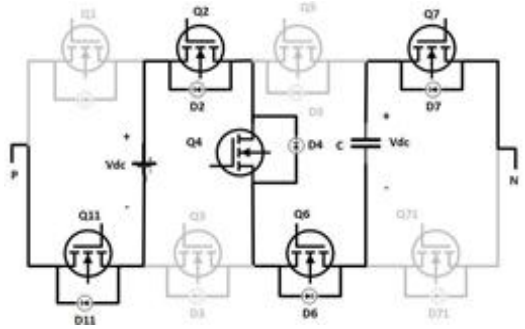


Fig.3(b). 2Vdc level

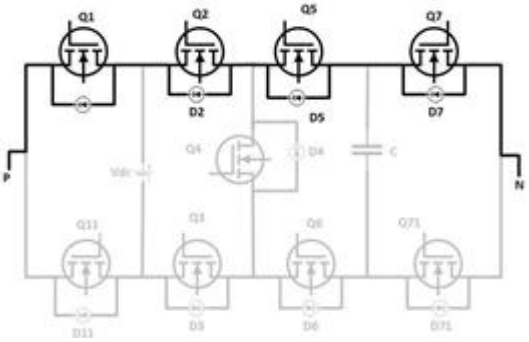


Fig.3(c). 0V level

2.1.2 Mode-2: Output Voltage (+2Vdc):

The switches Q11, Q2, Q4, Q6 and Q7 are triggering with help of Sinusoidal Phase Disposition PWM. Moreover, remaining switches will be turned off. The output voltage will be two times input voltage i.e. (2Vdc). The DC link capacitor is accepting the current through it. The rotor of induction motor is started to accelerate in this mode of operation. +2Vdc level shown in Fig.3(b) of operation. +2Vdc level shown in Fig.3(b)

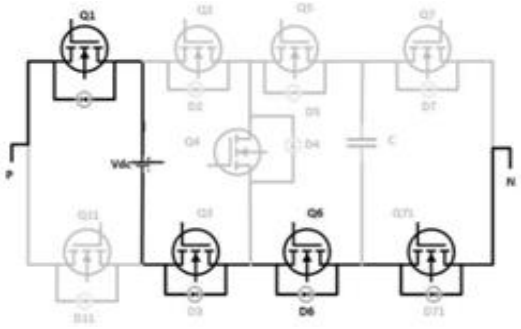


Fig.3(d). -Vdc level

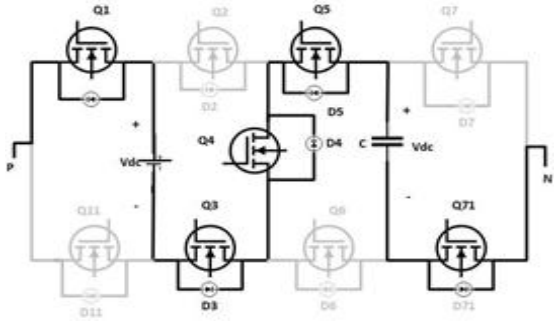


Fig.3(e). -2Vdc level

2.1.3 Mode-3: Output Voltage (0V)

The switches Q1, Q2, Q5, and Q7 are triggering with help of Sinusoidal Phase Disposition PWM. Moreover, remaining switches will be turned off. The output voltage will be zero voltage i.e. (0V). The rotor of induction motor has no variation in this mode of operation. 0 level shown in Fig.3(c)

2.1.4 Mode-4: Output Voltage (-Vdc)

In this operating mode, switches Q1, Q3, Q6, and Q71 are activated using the Sinusoidal Phase Disposition Pulse Width Modulation (SPDPWM) technique. All other switches remain deactivated. This switching configuration results in an output voltage equal to the negative value of the input DC voltage, i.e., −Vdc. Consequently, the induction motor starts to rotate in the reverse direction. The corresponding output voltage level for this mode is depicted in Fig.3(d).

2.1.5 Mode-5: Output Voltage (-2Vdc)

The switches Q1, Q3, Q4, Q5, and Q71 are triggering with help of Sinusoidal Phase Disposition PWM. Moreover, remaining switches will be turned off. The output voltage will be two times negative input voltage i.e. (-2Vdc). The rotor of induction motor has to rotate in the reverse direction as deceleration in this mode of operation. –2Vdc level shown in Fig.3(e). The Table.1 provides switching states of the SVB-RSC-FLI topology.

2.2 SINUSOIDAL PHASE DISPOSITION PULSE WIDTH MODULATION (SPDPWM) TECHNIQUE

SPDPWM is a form of Pulse Width Modulation (PWM) where the sinusoidal reference signals for each phase of a multi-phase inverter are generated with specific phase shifts relative to each other. These phase shifts are designed to improve the harmonic performance of the system. It minimizes Total Harmonic Distortion (THD) present in the output voltage waveform. When the reference signal are compared with help of comparator, it gives corresponding signals to switches. The amplitude of the reference signal would be 2. The frequency of the reference signal is to be normally 50 HZ and switching waveform of SVB-RSC-FLI is shown in Fig.4.

A switch's ON status is indicated by the entry "1," while its OFF status is indicated by the entry "0." To synthesize the output voltage with the necessary steps, the right gating signals must be produced. A single completely rectified signal of the sinusoidal reference (V_{ref}=$V_m$sinωt) and two level-shifted high-frequency carriers (Vcr1 and Vcr2) are used for this. The comparator outputs Vcp1 and Vcp2 undergo appropriate logic operations in order to derive switching functions (SFs). When V_{Ref}>0 a zero-crossing detector (Z_C) which is defined as Z_C=1. The switching function equations are shown in Eq.(2)-Eq.(8).

The no of carrier signal (N_C) required is,

$$N_c = \frac{N-1}{2} \tag{1}$$

$$Q_1 = V_{cp1}\bar{Z}_c \tag{2}$$

$$Q_2 = V_{cp1}Z_C + \bar{V}_{cp2} \tag{3}$$

$$Q_3 = \bar{V}_{cp2}Z_C + \bar{Z}_c \tag{4}$$

$$Q_4 = V_{cp2} \tag{5}$$

$$Q_5 = \bar{V}_{cp2}Z_C + V_{cp1}\bar{Z}_c \tag{6}$$

$$Q_6 = Z_C + \left(V_{cp2}Z_C\right) \tag{7}$$

$$Q_7 = V_{cp1}Z_C \tag{8}$$

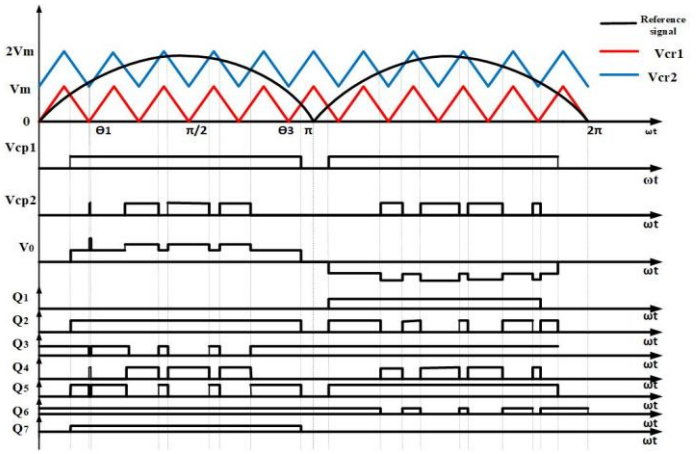


Fig.4. The theoretic analytical operating waveform of SVB-RSC-FLI topology

2.3 DESIGN OF CAPACITOR AND LCL FILTER

The DC power source and the switched capacitor (SC) are connected in parallel to generate output voltage levels of ±Vdc. The switched capacitor is designed to operate in a charge – discharge cycle, where it charges during one part of the cycle and discharges during another. Over time, this process results in the capacitor voltage stabilizing to match the magnitude of the input DC voltage. Provided that the switches in the charging path exhibit minimal parasitic effects, the SC can quickly charge to the input voltage level. For output levels of ±2Vdc, the SC is connected in series with the DC supply across the load, effectively increasing the output voltage to twice the input value. The minimum value of capacitor required is,

$$C_{\min} = \frac{2V_{DC}}{\omega_0 R_0 \Delta V_r} \tag{9}$$

where

C_{min} - minimum value of capacitor is required for SVB-RSC-FLI.

V_{dc} - Input DC voltage to be provided to the Inverter,

ω_0 is fundamental angular frequency in rad/sec.

R_0 is output load resistor in ohm.

ΔV is the change in ripple voltage in volts.

The inverter power rating (S):

$$S=VI$$

where

S=apparent power of proposed inverter.

V=voltage rating of inverter in volts.

I=current rating of inverter in amps

The capacitor value for LCL filter is,

$$C = \frac{0.05S}{V^2 \cdot 2\pi f} \tag{10}$$

$$C = 6.017\ \mu\text{F}$$

$$S = VI_0, \quad I_0 = 8.695\ \text{A} \tag{11}$$

$$\Delta I^{P\max} = 0.2I_0 \tag{12}$$

The inductor calculation for SVB-RSC-FLI topology,

$$L_1 = \frac{V_{DC}}{4F_{SW}\Delta I^{P\max}};\ L_1 = 0.6\ \text{mH} \tag{13}$$

$$L_1 + L_2 = \frac{0.1V^2}{S \cdot 2\pi f}; L_2 = 7.81\ \text{mH} \tag{14}$$

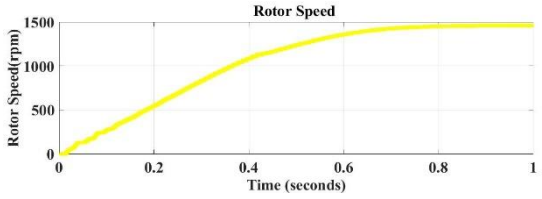
Table.2. LCL filter parameters for SVB-RSC-FLI topology

Sl. No	Parameters	Value
1.	Inductor (L1)	0.6mH
2.	Inductor (L2)	7.81mH
3.	Capacitor (C)	6.017µF

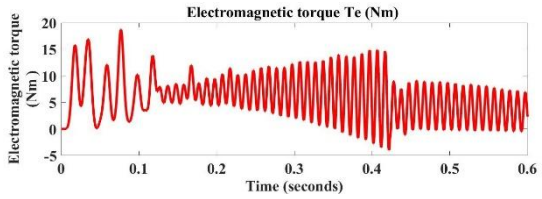
3. SIMULATION RESULTS AND DISCUSSION

The SVB-RSC-FLI simulation diagram is shown below. There are nine power switches are used in the Simulink model.

the Table.4 gives Simulation parameters of proposed topology. The DC voltage source and capacitor are connected as per the circuit diagram configuration of SVB-RSC-FLI five level inverter. The DC input voltage is 115V and the capacitor stores the same value of DC input voltage source.it operates the fundamental frequency of 50Hz. LCL filters are used in the Simulink model to filter out the higher order harmonics presented in the output voltage waveform and it gives the better performance than conventional LC filter.it smoothens the output voltage waveform for satisfactory operation of the induction motor. Here single-phase capacitor start induction motor is used in the SVB-RSC-FLI five level inverters. Then corresponding rotor speed, rotor current and electromagnetic torque will be observed in the Fig.5.



(a)



(b)

Fig.5. Single phase induction motor parameters waveform a) Rotor speed b) Electromagnetic torque

The resistor value of 50 ohm is connected across the terminals of the proposed topology. The capacitor start single phase induction motor has the advantage of self-starting capability. The gain value of 60/2*pi will be connected in series with rotor speed to get rotor speed in rpm and gives the five-level output voltage waveform. The triggering pulses for the power switches will be given to the corresponding switches. The sinusoidal phase disposition PWM will be used to generate the PWM signal at required instances of switching period. Then THD values of without filter and with filter will be compared in the Simulink model. THD value will be comparatively less in the SVB-RSC-FLI five level inverters. The Simulink diagram will be shown below in the Fig.6.

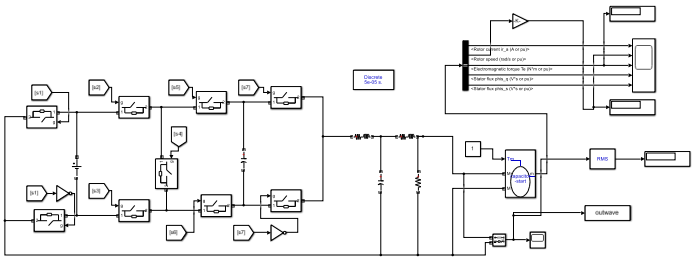


Fig.6. Simulink diagram of SVB-RSC-FLI topology with induction motor

3.1 SWITCHING PULSE GENERATION

The sinusoidal phase disposition modulation technique are used to generate the gate pulses to turn-on the power switches and the sinusoidal signal is taken as reference signal is compared with carrier signal. Switching pulse generation simulation diagram was shown in Fig.7. The repeating sequence block is used to generate a carrier signals. There are two comparators are used in this model. Then ABS block is used to take magnitude of reference signal. Then the logic gates are used in the Simulink model. Here in the Simulink model is mostly the AND, NOT and OR gates are used to generate the gate pulses. These gate pulses will be viewed in the scope, and two complimentary switches are used. The switching pulse waveform are generated and viewed in the scope as shown in the Fig.8. The output voltage waveform without filter and with filter was shown in Fig.9 and Fig.10.respectively.

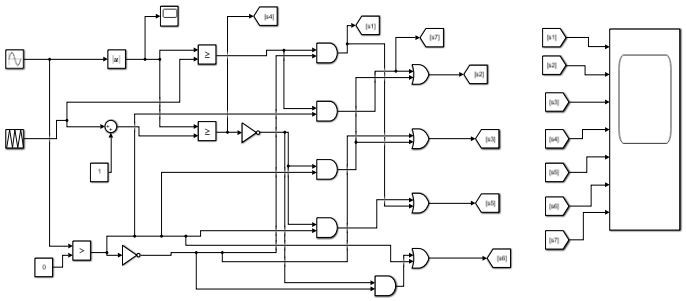
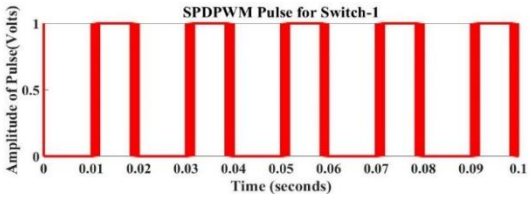
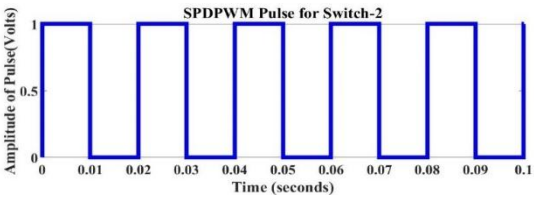


Fig.7. Switching pulse generation simulation diagram



(a)



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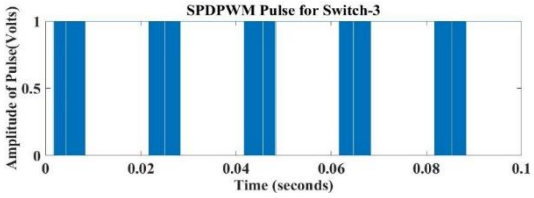
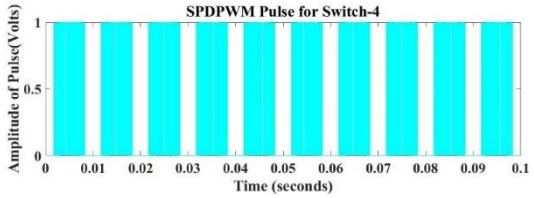
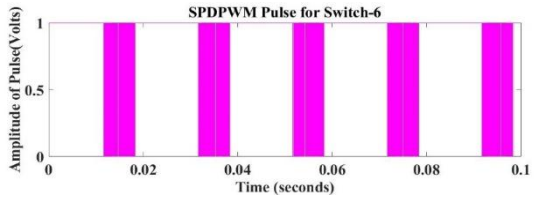


(c)

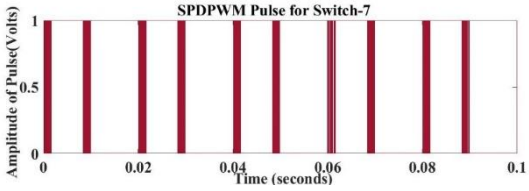


(d)

(e)



(f)



(g)

Fig.8. Switching pulses of the SVB-RSC-FLI topology. (a) Switch-1 pulse (b) Switch-2 pulse (c) Switch-3 pulse (d) Switch-4 pulse (e) Switch-5 pulse (f) Switch-6 pulse (g) Switch-7 pulse

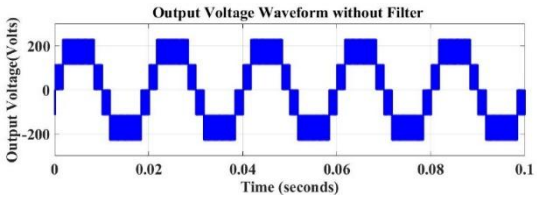


Fig.9. Five level output waveforms of SVB-RSC-FLI topology

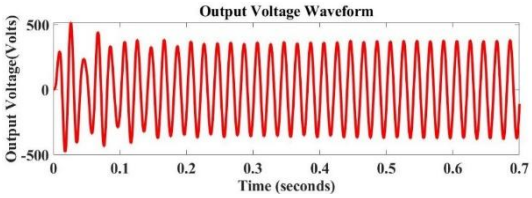


Fig.10. Output Voltage waveform of SVB-RSC-FLI topology

3.2 SINGLE PHASE INDUCTION MOTOR V/F CONTROL

Single-phase induction motors are commonly used in low-power residential and commercial applications. A practical method to achieve soft starting and speed control in these motors involves adjusting the supply frequency while maintaining a constant voltage-to-frequency (V/f) ratio. This technique ensures that the air-gap magnetic flux remains constant, allowing the motor to deliver maximum torque at any operating frequency. The equivalent circuit diagram for this configuration is shown in Fig.11. When the motor rotates in the forward direction, the forward magnetic flux (φ_f) is significantly greater than the backward magnetic flux (φ_b), resulting in a much higher forward electromotive force (E_f) compared to the backward electromotive force (E_b).

In addition, the forward resistance (R_f) is substantially higher than the backward resistance (R_b), causing the forward air-gap power (P_f) to exceed the backward air-gap power (P_b). The forward emf, backward emf and torque equation will be shown as follows.

$$E_f = 4.44 N_s f \phi_f \tag{15}$$

$$E_b = 4.44 N_s f \phi_b \tag{16}$$

The developed torque is (T_d),

$$T_d = \frac{P_f}{\omega_s} - \frac{P_b}{\omega_s} \tag{17}$$

where, ω_s - synchronous speed at desired frequency.

The waveform analysis of a single-phase capacitor start induction motor is carried out with a constant load torque set at a value of 1 unit. The motor parameters used for the analysis are provided in Table.4. The generated electromagnetic torque displays an alternating behavior, and the stator flux also alternates with time. As the motor operates, the rotor speed gradually increases. It starts at a low value and rises progressively in a linear manner as time advances. Initially, the rotor current waveform exhibits high-frequency oscillations, which diminish gradually as the motor reaches steady-state conditions.

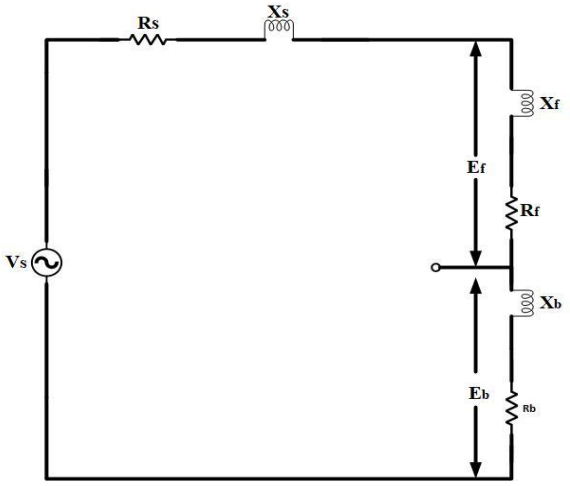


Fig.11. Equivalent circuit diagram of single-phase induction motor

3.3 THD ANALYSIS OF OUTPUT WAVEFORM WITHOUT FILTER

Power switches is used to trigger the five-level output from the self-balancing amplitude modulated five-level inverter. It is not a pure sinusoidal waveform. After that, THD analysis is carried out the magnitude and frequency of Matlab/Simulink software. The total harmonic distortion is derived from the fundamental value is close to 46.43%. The Fig.12 shows the displays of the output waveform.

3.4 THD ANALYSIS OF OUTPUT WAVEFORM WITH FILTER

The output waveform's contains harmonics are removed by the LCL filter. The MATLAB/SIMULINK program is used to view the THD analysis versus magnitude and frequency. THD values is decreased to 1.90% by using the filter. Generally, a THD of less than 5% is sufficient to provide a superior sinusoidal waveform. The induction motor is thereafter driven by the filtered waveform and shows the THD graph in Fig.13.

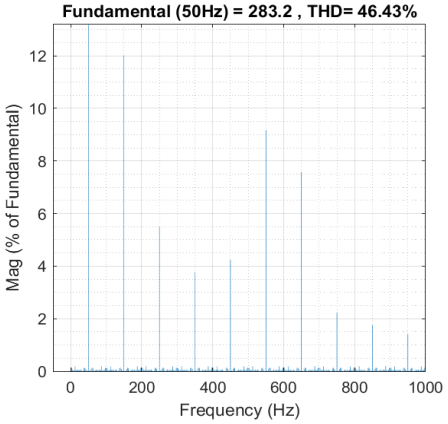


Fig.12. %THD of output waveform without filter

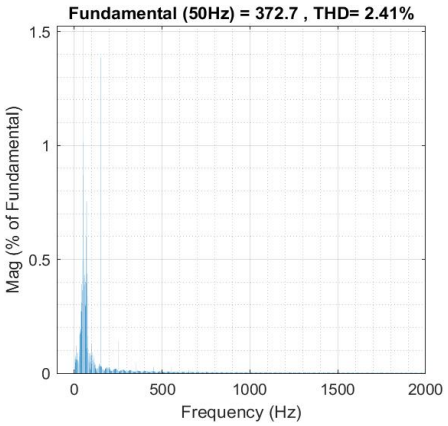


Fig.13. % THD of output waveform with filter

Table.4. Simulation parameters of SVB-RSC-FLI topology

Simulation Parameters	Value
DC input voltage	115V
Capacitor	1.52F
Inductor(L1)	0.6mH
Inductor(L2)	7.81mH
Capacitor (Cf)	6.017μF
Carrier frequency	50kHz
Single phase induction motor	0.25HP
Inverter power rating	2kVA
Output voltage	230V
Capacitor start	76.4μF
Stator resistance	8.08Ω

4. HARDWARE RESULTS AND DISCUSSION

4.1 EXPERIMENTAL SETUP OF SVB-RSC-FLI

The Self-Voltage Balancing Reduced Switch Count Five-Level Inverter (SVB-RSC-FLI) topology utilizes nine MOSFET switches, each equipped with an antiparallel diode to enable bidirectional current conduction. To maintain voltage uniformity across different stages of the converter, appropriately positioned capacitors are employed. Table 5 shows the Hardware parameters of SVB-RSC-FLI. This inverter generates a five-level output voltage by combining amplitude modulation with its built-in self-balancing capability. The overall configuration includes a DC-link capacitor, multiple power electronic switches, and a control unit designed to regulate the switching sequence and ensure efficient operation. The Fig.14 gives the Power circuit and output waveform of SVB-RSC-FLI.

4.2 OUTPUT OF SVB-RSC-FLI

The Five-Level Output waveform was measured using a digital storage oscilloscope. The power circuit and gate driver circuit were properly connected using appropriate wiring. The required gate pulses were generated by an Arduino Mega 2560, which provided the SPDPWM (Sinusoidal phase disposition Pulse-Width Modulation) signals through digital pins 2 to 10. These pulses were used to trigger the corresponding switches in the circuit.

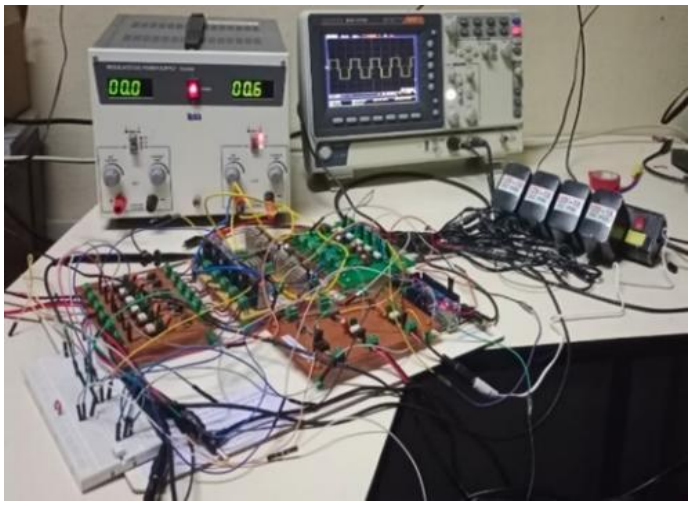


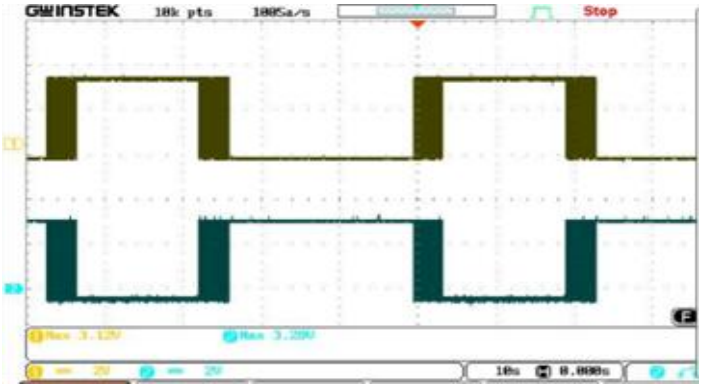
Fig.14. Power circuit and FLI waveform of SVB-RSC-FLI

Table.5. Hardware parameters Specification of SVB-RSC-FLI

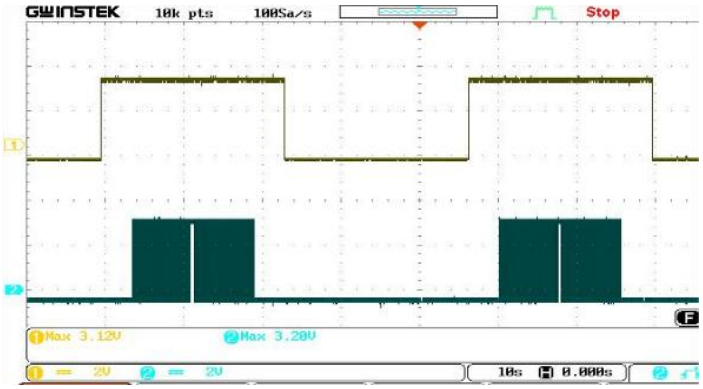
COMPONENT	RATING
MOSFET	200 V, 30A and IRFP250N
Arduino Mega	2560
Photo coupler	TLP250
Dot Board	-
Resistor	390Ω(1), 10Ω(2)
Capacitor	100nF&100μF/50V
Diode	FR306/800V,1A

4.3 SWITCHING PULSES OF SVB-RSC-FLI

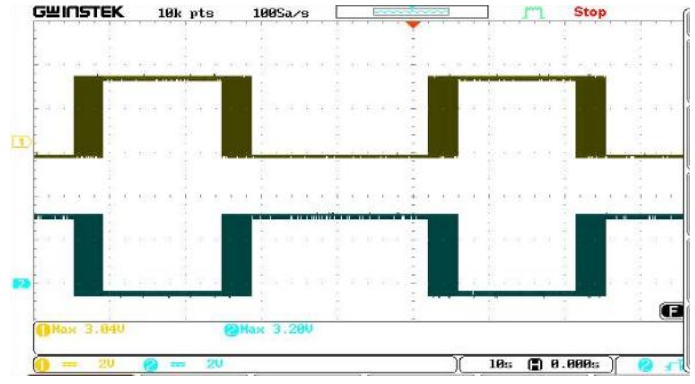
The switching pulses for each individual switch were derived using appropriately formulated switching logic equations. Distinct control signals were employed for each switch to synthesize the desired five-level output waveform. To prevent shoot-through conditions, an adequate dead time was incorporated between complementary switching devices within the topology. The resulting switching waveforms were captured and analyzed using a digital storage oscilloscope, as illustrated in Fig.15.



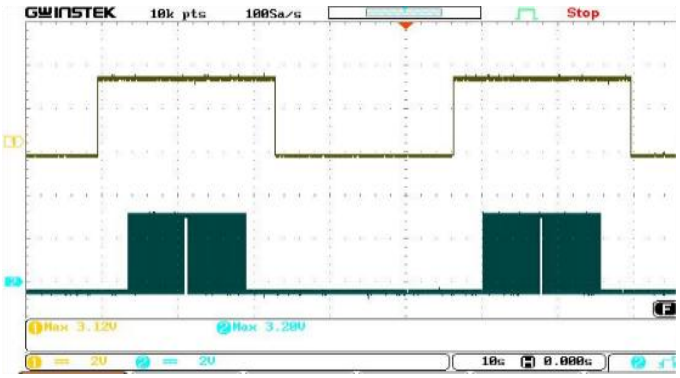
(a)



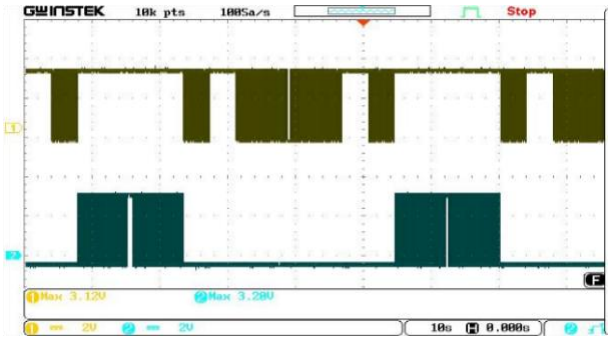
(b)



(c)



(d)



(e)

Fig.15.Switching pulse waveform: (a) Switch-1 and $\overline{1}$ (b) Switch-7 and $\overline{7}$ (c) Switch-2 and 3 (d) Switch-5 and 6 (e) Switch-4

5. CONCLUSION

The self-balancing capability of the SVB-RSC-FLI topology eliminates the need for additional voltage-balancing circuits, thereby simplifying the system architecture and enhancing overall reliability. By lowering voltage stress on the switching devices and reducing the switching frequency, the inverter achieves higher operational efficiency while minimizing stress on power components, which in turn extends their service life. The application of a sinusoidal PWM technique ensures that the output waveform closely approximates a pure sine wave, which is essential for sensitive applications such as motor drives. A comprehensive THD analysis was carried out on the output voltage both with and without the use of filtering. The results demonstrated a significant reduction in harmonic distortion, thereby improving the power quality delivered to the load. To further assess the inverter's performance, a single-phase induction motor was modeled and simulated in Matlab/Simulink.

The simulation confirmed that the SVB-RSC-FLI could effectively operate the motor, delivering improvements in torque, speed regulation, and efficiency when compared to conventional inverter configurations.

5.1 FUTURE SCOPE

This inverter can be effectively used in solar energy applications to enhance overall system performance and improve energy conversion efficiency.

- *Grid Integration*: The inverter is suitable for grid-connected systems, enabling seamless integration of renewable energy sources with the utility grid.
- *Industrial Applications*: It can be applied in industrial environments, offering reliable operation, efficient power handling, and suitability for various high-demand applications.
- *Advanced PWM Techniques*: The switching PWM strategies should be further optimized to achieve higher efficiency and improved overall performance in inverter operations.
- *Reduction of Filter Size*: The filter size can be reduced to lower the overall system cost while still maintaining adequate harmonic suppression and performance.

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