ISSN: 2395-1680 (ONLINE)
DOI: 10.21917/ijme.2025.0350

DESIGN OF HIGH-PERFORMANCE,ULTRA-LOW POWER LEVEL SHIFTER FOR DIGITAL CMOS CIRCUITS

Srilekha Pappu, Varnateja Purugula, Viswathez Reddy Chinthareddy and Silpa Kesav Velagaleti
Department of Electronics and Communication Engineering, CVR College of Engineering, India

Abstract

This paper presents the design and simulation of an ultra-low leakage, wide-range voltage level shifter optimized for low-power digital CMOS VLSI applications. Implemented in 45 nm technology, the proposed circuit efficiently converts low-voltage input signals (0.3V) to a higher output voltage (1.2V) while minimizing power dissipation. The design incorporates leakage shut-off transistors and a low-threshold pull-down network to enhance energy efficiency and transition speed. Simulation results demonstrate a static power consumption as low as 140 fW in the Fast-Fast (FF) process corner and up to 180 fW in the Slow-Slow (SS) corner. The level shifter achieves a propagation delay between 5.8 ns (FF) and 8.5 ns (SS), with energy per transition ranging from 0.81 fJ to 1.53 fJ. These results validate the circuit's robustness and efficiency across different PVT variations, making it a suitable design for ultra-low power.

Keywords:

Voltage Level Shifter, Ultra-Low Leakage, Multi-Supply Voltage, Energy-Efficient Design, System-on-Chip (SoC)

1. INTRODUCTION

With the increasing demand for low-power digital circuits, Voltage Level Shifters (VLS) play a crucial role in enabling communication between different voltage domains in modern CMOS VLSI systems. As technology scales down, power efficiency and leakage reduction become critical design constraints. Conventional level shifters [3-4] often suffer from increased static power consumption, reduced noise margins, and slower transition speeds when operating at ultra-low supply voltages. To address these challenges, a Wide-Conversion Range and Minimal Leakage Level Shifter WCMLS [5] is proposed, which efficiently converts low-voltage signals to higher voltage levels while minimizing leakage currents. Unlike conventional designs, WCMLS [5] leverages a strong pull-up network with a cross-coupled PMOS structure to achieve robust operation across a wide voltage range. Additionally, it ensures ultra-low leakage by employing a carefully designed transistor stacking technique, making it highly suitable for nodes where leakage currents are more pronounced. Furthermore, technology nodes shrink to subthreshold leakage and short-channel effects become more prominent, leading to higher static power dissipation in conventional level shifters [3-4]. WCMLS (Fig.1) mitigates these issues by utilizing an optimized transistor arrangement that reduces leakage while maintaining a strong drive capability. The circuit also achieves robust operation across a wide range of supply voltages, making it highly adaptable. By leveraging an improved pull-down network and minimizing contention during switching, WCMLS [5] enhances speed and energy efficiency, making it a superior alternative to traditional level shifters in ultra-low-power and high-performance applications.

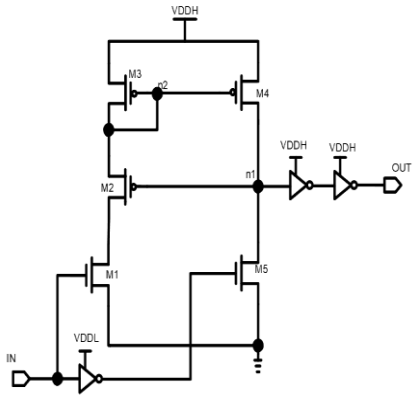

Fig.1. Wilson current mirror-based Level Shifter

This paper is structured as follows: Section 2 gives an extensive literature review, discussing voltage level shifters that have been proposed so far, their operating mechanisms, and shortcomings in low-power applications. Section 3 describes the design methodology, i.e., the circuit topology, transistor sizing requirements, and optimization techniques for using the level shifter in 45 nm technology. Section 4 outlines the simulation configuration and presents a detailed analysis of the transient response, power dissipation, delay behavior, and performance comparisons versus traditional designs. Section 5 concludes the paper by summarizing the main contributions and noting future research challenges, including possible applications in ultra-low-power digital CMOS circuits.

2. LITERATURE REVIEW

The relentless scaling of semiconductor technology to the 45 nm node has had a profound impact on low-power digital circuit design, particularly in portable and battery-powered equipment. In light of increasing demand for low-power and high-performance systems, researchers have concentrated on how to make circuit designs more efficient to improve transistor density and performance while reducing power dissipation. Technologies like High-k/Metal Gate (HKMG) and strained silicon have been essential in meeting these objectives by improving electrostatic control and carrier mobility. To meet power efficiency and performance challenges, numerous hardware solutions such as ultra-low leakage level shifters have been suggested. Such designs typically involve leakage shut-off transistors and voltage hysteresis transistors to minimize static power dissipation while facilitating high-speed voltage conversion. In addition, software methods like Dynamic Voltage and Frequency Scaling (DVFS) and adaptive body biasing have been utilized to dynamically control power consumption based on workload requirements, maintaining energy efficiency without sacrificing performance.

The developments in the recent past have also emphasized the efficiency of low- power design but an efficient design would be when a circuit is operated in the subthreshold range of voltages. OAI (OR-AND-INVERT) logic [14] has shown positive promise to improving performance while simultaneously lowering power in components like ALUs and registers [15]. These allow the circuit to perform the computations without needing to consume any power and find very good applications in ultra-low powered applications. In addition to power efficiency, security in digital systems has been a growing concern, leading to innovative implementations that integrate gated D-latch mechanisms for enhanced protection [16]. Such approaches are particularly relevant in applications requiring secure and reliable state retention while maintaining minimal energy usage. These efforts contribute to the ongoing evolution of CMOS-based digital systems, ensuring both functional robustness and efficiency in modern computing architectures.

Earlier designs, including those of Lee [3] and Kabirpour [4], have confronted comparable issues but were marred by limitations in leakage and drive strength. Lee's design [3] had higher power dissipation because of direct supply-to-ground routes, whereas Kabirpour design [4] had poor drive strength at low voltages. The new designs rectify these shortcomings by utilizing leakage cutoff transistors and the application of hysteresis mechanisms to improve power efficiency and strength. As technology keeps miniaturizing, merging hardware and software breakthroughs becomes imperative, allowing hybrid techniques such as cross-layer approximations and quality-configurable circuits. Such techniques enable designers to effectively trade performance and power consumption, leading to sophisticated low-power applications while ensuring reliability and accuracy, particularly in safety-critical systems.

3. DESIGN OF PROPOSED LEVEL SHIFTER

The traditional Level Shifter [1] (LS) connector was created and simulated for their performance assessment. Two forms of them, based on Lee's and Kabirpour's [4] architectures, have been developed and analyzed. Although these circuits execute voltage level shifting, they have some obvious shortcomings that prevent their effectiveness in low-power applications from being achieved. The Lee's Level Shifter [3] shown in Fig.2 is implemented using a cross-coupled PMOS transistor structure to enhance the switching speed. However, the design also has problems with high static power consumption during certain transitions as the direct current path appears between VDDH and VSS for each PMOS transistor sometimes when in a conducting state. In addition, the circuit has trouble with the low supply voltage, because slow signal transitions and the increased propagation delay are the results of the reduced drive strength of the pull-up PMOS transistors. The narrowest the operating voltage range the circuit can cover is, it is the fact that the circuit is barely able to perform reliable level shifting when transitioning from an extremely low input voltage (VDDL) to a high output voltage (VDDH) due to mainly threshold voltage constraints and leakage issues. Yet, Kabirpour's Level Shifter [4]in Fig.3, by introducing an additional pull-down path using stacked NMOS transistors, realizes the same without having to sacrifice switching behavior. Nevertheless, this model still shows a big amount of short-circuit current. It is mainly caused by the whole process of switching. Moreover, circuit operation is also quite unstable at ultra-low voltages since pull-up transistors are usually quite weak and therefore provide insufficient drive strength for high-speed transitions. Moreover, in intermediate nodes, a signal degradation occurs, which leads to incomplete voltage swings and a decrease in stability of the system when supply voltage changes.

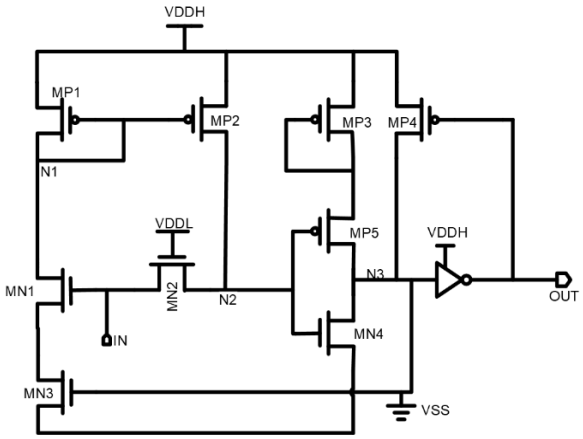

Fig.2.Lee's Level Shifter

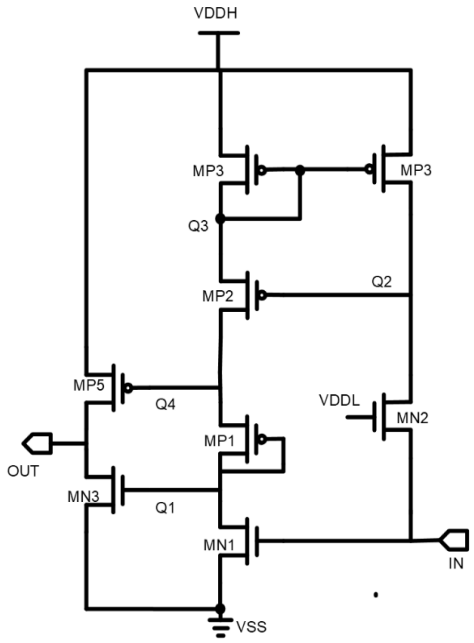

Fig.3.Kabirpour's Level Shifter

To produce these advantages, a new level shifter design is proposed. It is going to be an artistic new design which will affect energy efficiency, switching path and operational voltage range. The new design significantly reduces the static power loss, ensures better voltage scaling adaptability, and is embedded with an optimized transistor arrangement that makes it possible to achieve improved performance. The following section provides an in-depth discussion of the proposed LS architecture, highlighting its structural improvements and performance advantages over conventional designs. Fig.4. shows the proposed level shifter.

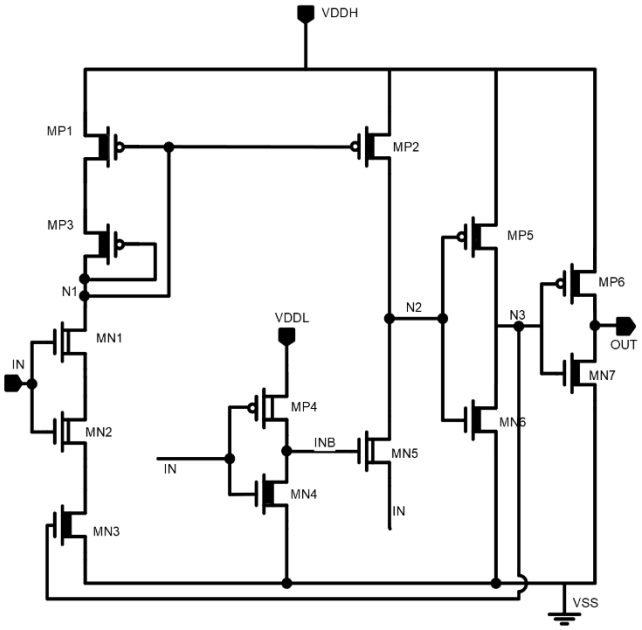

Fig.4. The Proposed Level shifter

The proposed level shifter (LS) circuit introduced is developed employing 45nm CMOS technology. Each of the PMOS and NMOS transistors have a width of 600 and 480 nm. The high-speed level shifter has the provision of Pull-Up Network (PUN) and a Pull-Down Network (PDN) to move low voltage (VDDL) signal to a higher voltage domain (VDDH) with less power dissipation. The pull-up network that is in cross-coupled form with MP1 (selected from the high-to-low transitions) and MP3 to have a reduced transition delays is the strength of the PUN. On the other hand, The MP5 and MP6 transistors which imitate a voltage swing are the components of the PUN. The PDN that consists of stacked NMOS transistors MN1, MN2, MN3, MN5, MN6, and MN7 provides the necessary pull-down path is short enough to cope with the low-to-high and high-to-low transition in the output. To exert the dynamic stability of the circuit, the use of hysteresis transistors MP4 and MN4 introduces the hysteresis effect, which in turn prevents unnecessary oscillations and improves the immunity against noise. Thus, allowing the circuit to operate at a lower voltage with extra stability. The proposed level shifter circuit has managed to allow reliable voltage translation with the help of PUN and PDN; therefore, the operation is quite efficient. The Level Shifter [1] employs leakage shut-off transistors to eliminate static power dissipation in standby mode, while a voltage hysteresis transistor improves the PUN response, ensuring a fast and complete internal node charging. In contrast, the proposed level shifter builds upon these principles while ensuring strong rail-to-rail voltage conversion from 0.3V to 1.2V without excessive delay. When the input IN is at 0V, the PDN remains inactive, and the intermediate node N1 is pulled to VDDH (1.2V) via MP1 and MP3, ensuring a strong logic HIGH at N1. This in turn keeps OUT at 0V (nano-volts due to leakage control), maintaining an ultra-low static power state. When IN switches to 300mV, the PDN activates, pulling N1 to 0V, turning OFF the PUN (MP1, MP3), and enabling MP2, which charges N2 to 1.2V, propagating a logic HIGH to the output. The Proposed Level Shifter optimizes the pull-down strength using low-threshold NMOS devices to ensure fast transitions with minimal contention while completely cutting off leakage pathways using stacked NMOS shut-off techniques. The results accurately translate 0.3V logic to 1.2V logic without inverting the signal, ensuring robust and power-efficient level shifting. With a propagation delay of 7ns and a static power consumption of 158.1fW at 0.3V, proposed level shifter significantly outperforms conventional designs by balancing speed, energy efficiency, and leakage suppression, making it ideal for low-power digital CMOS VLSIs. The hysteresis feedback plays a significant role in increasing the noise immunity and a decrease in glitches, thus the stable switching is guaranteed.

4. SIMULATION RESULTS

To verify the performance of the proposed LS, some recent LSs and the proposed LS are simulated in the 45 nm process. The output load is set to 0.1 pF. Three PVT corners were adopted to explore the stability of the proposed LS across different PVT corners, ranging from the worst corner to the best corner. The typical PVT corner is 25 ◦C, the typical NMOS, and the typical PMOS. The best and worst cases are fast-NMOS, fast-PMOS, -45 ◦C, and slow-NMOS, slow-PMOS, 125 ◦C, respectively. The following table shows the comparison of the performance analysis of a voltage level shifter for all the three PVT corners: Typical-Typical (TT), Slow-Slow (SS), and Fast-Fast (FF). The voltage of the input is 0.3V, and the one of the outputs is 1.2V, which reveals the level-shift operation. The circuit will be running with a lower supply voltage (VDDL) of 0.3V at 10 MHz and a higher supply voltage (VDDH) of 1.2V. Static power consumption ranges from 180 fW (SS) where there is increased leakage to 140 fW (FF) with increased efficiency. The propagation delay is the longest in case of SS (8.5 ns) and the shortest in the case of FF (5.8 ns), which is due to the transistor speed variation. Besides, energy per transition is the most in SS (1.53 fJ) and the least in FF (0.81 fJ). The data show that the voltage level shifter is more energy efficient if manufactured under FF corner conditions; however, it will use higher power if fabricated under SS process corner conditions. The less time of a transition of the positive edge, the less static power is dissipated; however, the cycle count itself is also less which is why FF obtains lower circuit power. All these findings indicate a certain phase change in the material, which affects the way the circuit operates. Among the three PVT corners, there is the most leakage current in SS leading to the device most energy consumption while FF produces the least current. Thus, when it comes to device efficiency, FF is superior in this regard. We can see that the performance of a level shifter dramatically changes with the sum of VDDH and VDDL. This affects the technology of FinFET transistors in the device. It is a valuable tool for precise power analysis, a crucial factor in embedded applications.

Table.1. Proposed Level shifter in different PVT corners where Input voltage=0.3V, VDDL=0.3V, VDDH=1.2V, Output voltage=1.2V

PVT Corner	Static Power (fW)	Delay (nS)	Energy per Transition (fJ)
TT (Typical)	158.1	7.0325	1.112
SS (Slow-Slow)	180	8.5	1.53
FF (Fast Fast)	140	5.8	0.81

The Fig.5 depicts the transient response simulation of the voltage level shifter demonstrates its ability to convert a low input voltage (300 mV) to a higher output voltage (1.2V). The waveform shows a transition at 500 ns, where the input shifts from high to low, and the output follows accordingly, confirming proper functionality. The results validate the level shifter's efficiency in achieving ultra-low leakage and wide-range voltage conversion, ensuring reliable operation in low-power digital CMOS applications than other level shifters [1] [3] [4] [8] [10] [11]. The Fig.6 depicts the transient response simulation of the voltage level shifter shows the conversion of a 300-mV signal to a 1.2V output while operating with VDDH at 1.2V and VDDL at 300 mV. The input is a periodic square wave, and the output correctly follows, demonstrating successful level shifting. The internal node voltageN1 reveals charging and discharging behavior, indicating transistor switching activity.

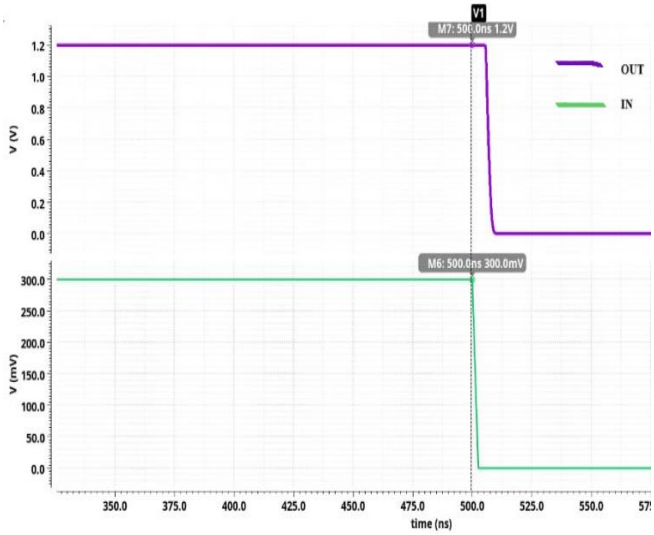

Fig.5. Transient waveform of operation details of proposed level shifter

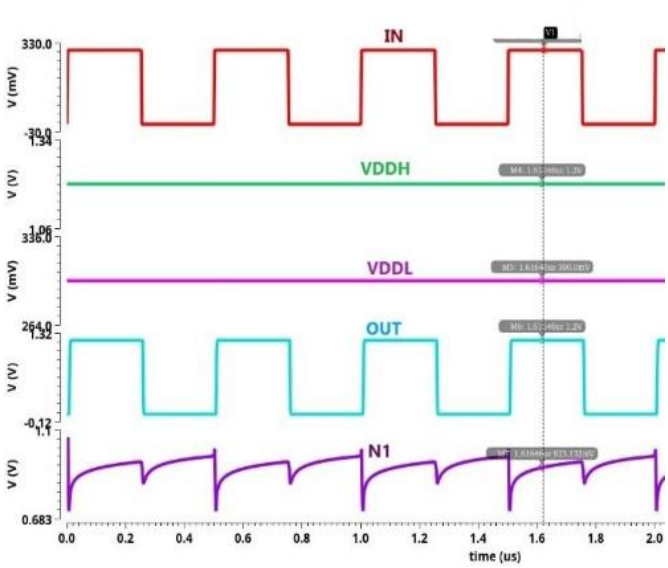

Fig.6. The transient waveform at internal node N1

The Fig.7 depicts the transient response simulation for the voltage level shifter demonstrates the successful conversion of a low-voltage input (300 mV) to a higher output voltage (1.2V). The input signal transitions between 0V and 300 mV, while the corresponding output signal follows the expected level-shifting behavior, reaching approximately 1.2V. The waveform shows proper signal integrity with a smooth transition, indicating effective switching and minimal delay.

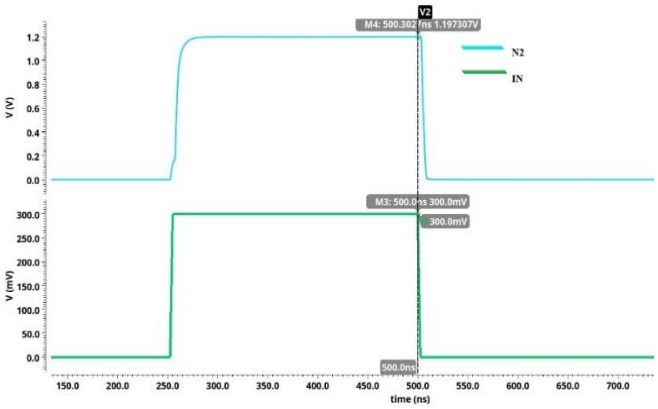

Fig.7. The internal voltage at node N2

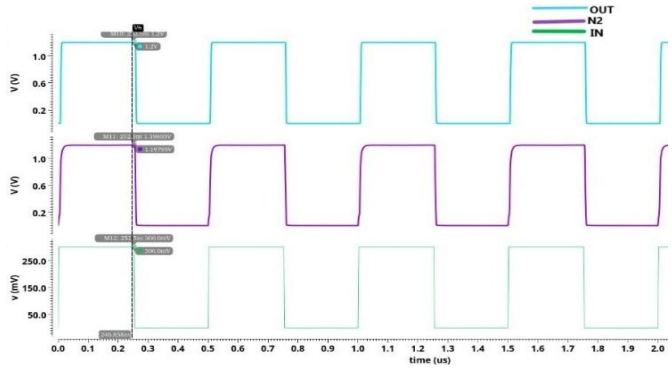

Fig.8. The transient waveform at internal node N2 w.r.t OUT

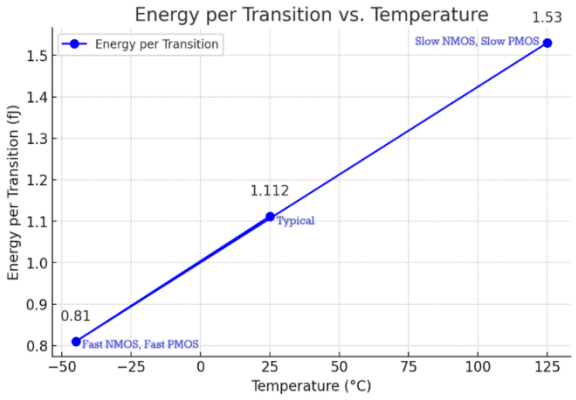

Fig.9. Energy per Transition vs Temperature at different PVT Corners

The Fig.8. depicts the transient response simulation for the voltage level shifter illustrates the proper conversion of a low-voltage input (300 mV) to a higher output voltage (1.2V). The input signal transitions between 0V and 300 mV, while the intermediate node and the final output follow the expected level-shifting behavior, reaching approximately 1.2V. The waveforms

indicate smooth transitions anminimal propagation delay, confirming efficient signal conversion.

The Fig.9 represents the relationship between the energy per transition and temperature. The diagram reveals the positive correlation and as a result, we conclude that with increasing temperature, the energy for the transitions is also going up. On the one hand, at -45°C, the energy per transition is nearly 0.81 fJ while at 25°C, it is 1.112 fJ, further at 125°C, it goes up to 1.53 fJ. From this point of view, everything indicates that certainly, the highest temperatures are indicative of the maximum power consumption, which is very meaningful for the performance of the circuit and the matter of energy efficiency. This transient response simulation for the 45 nm voltage level shifter illustrates the proper conversion of a low-voltage input (300 mV) to a higher output voltage (1.2V). The input signal transitions between 0V and 300 mV, while the intermediate node and the final output follow the expected level-shifting behavior, reaching approximately 1.2V. The waveforms indicate smooth transitions and minimal propagation delay, confirming efficient signal conversion.

5. CONCLUSION

This paper presents an ultra-low leakage and wide-range voltage level shifter optimized for low-power digital CMOS VLSIs. The proposed design reduces static power by 52.81% compared to Lee's design and 64.87% compared to Kabirpour's, achieving a remarkably low 158.1 femtowatts of static power. It also exhibits a 7.0325 ns propagation delay, with a power-delay product (PDP) of 1.1118×10^{-21} joules (J), ensuring an efficient balance between power and speed. Implemented in 45 nm technology, the design demonstrates improved energy efficiency and robust performance across varying supply voltages. Future work may focus on further optimizing delay and expanding its operational range for next-generation semiconductor technologies. Future work may focus on further optimizing delay characteristics and expanding the operational range to enhance adaptability for emerging semiconductor technologies.

REFERENCES

[1] M. Alioto, "Ultra-Low Power VLSI Circuit Design Demystified and Explained: A Tutorial", *IEEE Transactions on Circuits and Systems I: Regular Papers*, Vol. 59, No. 1, pp. 3-29, 2012.

[2] V.L. Le and T.T. Kim, "An Area and Energy Efficient Ultra-Low Voltage Level Shifter with Pass Transistor and Reduced-Swing Output Buffer in 65-nm CMOS", *IEEE Transactions on Circuits and Systems II: Express Briefs*, Vol. 65, No. 5, pp. 607-611, 2018.

[3] S. Kabirpour and M. Jalali, "A Power-Delay and Area Efficient Voltage Level Shifter based on a Reflected-Output Wilson Current Mirror Level Shifter", *IEEE Transactions on Circuits and Systems II: Express Briefs*, Vol. 67, No. 2, pp. 250-254, 2020.

[4] S. Lutkemeier and U. Ruckert, "A Subthreshold to Above-Threshold Level Shifter Comprising a Wilson Current Mirror", *IEEE Transactions on Circuits and Systems II: Express Briefs*, Vol. 57, No. 9, pp. 721-724, 2010.

[5] M. Lanuzza, F. Crupi, S. Rao, R. De Rose, S. Strangio and G. Iannaccone, "An Ultralow-Voltage Energy-Efficient Level Shifter", *IEEE Transactions on Circuits and Systems II: Express Briefs*, Vol. 64, No. 1, pp. 61-65, 2017.

[6] S.C. Luo, C.J. Huang and Y.H. Chu, "A Wide-Range Level Shifter using a Modified Wilson Current Mirror Hybrid Buffer", *IEEE Transactions on Circuits and Systems I: Regular Papers*, Vol. 61, No. 6, pp. 1656-1665, 2014.

[7] L. Fassio, "A Robust, High-Speed and Energy-Efficient Ultralow Voltage Level Shifter", *IEEE Transactions on Circuits and Systems II: Express Briefs*, Vol. 68, No. 4, pp. 1393-1397, 2021.

[8] H. You, J. Yuan, W. Tang, S. Qiao, and Y. Hei, "An Energy-Efficient Level Shifter for Ultra Low-Voltage Digital LSIs", *IEEE Transactions on Circuits and Systems II: Express Briefs*, Vol. 67, No. 12, pp. 3357-3361, 2020.

[9] K. Kim, J.Y. Kim, B.M. Moon and S.O. Jung, "A 6.9-μm^2 3.26-ns 31.25-fJ Robust Level Shifter with Wide Voltage and Frequency Ranges", *IEEE Transactions on Circuits and Systems II: Express Briefs*, Vol. 68, No. 4, pp. 1433-1437, 2021.

[10] M.N. Sharafi, H. Rashidian and N. Shiri, "A 38.5-fJ 14.4-ns Robust and Efficient Subthreshold-to-Suprathreshold Voltage-Level Shifter Comprising Logic Mismatch-Activated Current Control Circuit", *IEEE Transactions on Circuits and Systems II: Express Briefs*, Vol. 70, No. 6, pp. 1906-1910, 2023.

[11] E. Late, T. Ytterdal and S. Aunet, "An Energy Efficient Level Shifter Capable of Logic Conversion from Sub-15 mV to 1.2 V", *IEEE Transactions on Circuits and Systems II: Express Briefs*, Vol. 67, No. 11, pp. 2687-2691, 2020.

[12] R. Lotfi, M. Saberi, S.R. Hosseini, A.R. Ahmadi-Mehr and R.B. Staszewski, "Energy-Efficient Wide-Range Voltage Level Shifters Reaching 4.2 fJ/Transition", *IEEE Solid-State Circuits Letters*, Vol. 1, No. 2, pp. 34-37, 2018.

[13] A.K.M.M. Islam, J. Shiomi, T. Ishihara and H. Onodera, "Wide-Supply-Range All-Digital Leakage Variation Sensor for on-Chip Process and Temperature Monitoring", *IEEE Journal of Solid-State Circuits*, Vol. 50, No. 11, pp. 2475-2490, 2015.

[14] S.K. Velagaleti and D. Lahari, "Design of 8-bit ALU using OAI Logic at Subthreshold Voltage", *Proceedings of the International Conference for Innovation in Technology*, pp. 1-7, 2023.

[15] D. Lahari, S. Velagaleti and V. Nikitha, "Design of 8-bit Register using OAI Logic at Subthreshold", *Proceedings of the International Conference on Intelligent and Innovative Technologies in Computing, Electrical and Electronics*, pp. 1117-1122, 2023.

[16] S. Velagaleti, "An Integrated Security System for Bank Lockers using Gated D-Latch", *Proceedings of the International Conference for Innovation in Technology*, pp. 1-5, 2023.