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LOW CRITICAL DELAY LIFTING BASED DWT ARCHITECTURE USING MULTIPLIER LESS CIRCUITS IN FINFET TECHNOLOGY

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Abstract

The implementation of 2D DWT is a challenge using CMOS technology for miniature device (65nm minimum). For applications like biomedical engineering the area and power consumption are to be reduced. The Limitation of Existing methods is addressed in this paper and an alternate method of implementing the algorithm is presented. In addition, problems lie on high critical path due to the presence of multipliers, Delay is high due to critical path and computation, Execution Speed is less due to multipliers in existing DWT architecture. On the other hand below 45nm the problems in CMOS devices on leakage current, limitations on threshold voltage, short channel effect, high field effects and dopant number fluctuations, and interconnect delays are faced. The work focuses on designing the 2D DWT architecture using FinFETs which has leakage power superiority and power minimization. The proposed VLSI architecture for lifting based 2D-Discrete wavelet transforms (DWTs) using FinFET in 32nm technology is efficient when compared to the existing convolution-based architecture. The Predict and update stage of lifting based DWT without multiplier is implemented using HSPICE. The critical delay due to multiplier usage is eliminated. The multiplier less design enhances the performance of the system.

Keywords:

Discrete Wavelet Transform, Multiplier Less, Lifting Based Architecture, Predict, Update, FinFET, CMOS

1. INTRODUCTION

In biomedical applications, several algorithms and methods are used to analyse the information in the image. These algorithms and methods are to be implemented in Hardware. The hardware to be used or implemented depends on the computation requirement of the methods [1]. In addition, the signals are to be filtered in the data acquisition units or camera units. Fail to remove the noises the signals will be corrupted considering the fact that most signals are non-stationary [13]. Now the challenge is on the processing unit which should be computationally efficient. Methods are to be computationally better and should be easy to implement [15-17]. Considering several methods from the literature the wavelet transform (WT) considered to be a time-frequency method not only enhances the performance when compared to short time Fourier transform (STFT) and statistical methods but easy to implement [18-23]. The frequency resolution property in Wavelet transform and Fourier Transform varies much. When WT decomposes the frequency and provides different resolution while Fourier Transform provides uniform resolution over all frequencies. Using multi-resolution technique this is done in Wavelet Transform. The windowing method in STFT analysis is similar to the multi-resolution steps.

1.1 LITERATURE REVIEW

The Discrete Wavelet Transform (DWT) and Integer wavelet transform (IWT) are significant in image processing applications. Dhakar and Pathak [13] presented low area architecture by eradicating line buffer and frame buffer. [14] used Dual mode lifting based scheme. Dual mode lifting based discrete wavelet transform can be used. Tahrim et al [5] applied Daib and bi-orthogonal filters for multilevel 2-D DWT. Compact design and lower clock period minimize the ADP and EPI by Tahrim et al. [5]. Lifting algorithms consists of processing units that use inherent parallelism to a great extent on the basis of 2D DWT to reduce the memory requirement and critical path. The Attractive feature of this architecture was 23% to 29% of efficiency in reduction when compared to mirror structure and 25% to 50% by Madanayake et al. [6]. Design of FPGA and VLSI are presented by Palanisamy et al. [8]. A 1-D DWT design was extended with an modified lifting architecture and it is used in 2-D DWT with z type block scanning method by Pinto and Shama et al. [9]. The Lifting based 3D DWT schemes accomplished without any restrictions by Ravindrakumar et al. [10]. The DWT execution of bit parallel and digit-serial precision optimization is carried out. Addition to this it is observed that block processing yields maximum speed and optimizes hardware with minimum power overhead by Ravindrakumar and Joselyn [11]. A 1-D DWT and 2-D DWT was designed to execute an independent image size. The Z fashion scanning process was performed to minimize the temporal buffer by Ravindrakumar and Joselyn [11]. A modified DWT processor is designed. This architecture was executed on zedboard by Senthilkumar et al. [2]. A modified 2D DWT was constructed for image coding for the execution of adaptive directional lifting algorithm by Senthilkumar et al. [3]. Pinto et al [9] presented a fast and memory efficient lifting based 1-D and 2-D DWT architecture. It has used in Daubechies 5/3 and 9/7 filters. Scanning process for one level 2-D transform is in Z fashion for an N*N image. It was executed with VHDL and synthesized with Cadence tool in 90nm technology. Naik et al. [7] modelled modified dual memory controller based VLSI architecture for DWT. Hence a dual memory controller based on DWT is designed and executed on Zedboard. Yun et al. [12] described a VLSI based 2-D DWT which is to be used with adaptive directional lifting (ADL) for image coding. Tahrim et al [5] analyzed performances of 1-bit FinFET full adder cells. This Analysis majorly concentrates on sub threshold region with 16 nm process technology. This Process used PTM and Berkeley short channel IG FET methodology. Chakraborty et al. [4] revealed the modified lifting based 1D/2D DWT with pipelined VLSI architecture. This Design has utilized minimum number multipliers. The total processing time of this architecture are minimized by with help of block which as Z type memory

scanning functions. The leakage problem can be addressed by the channel control unlike CMOS devices by which the dynamic power consumption be optimized using FinFET devices. In FinFET device the load capacitance charges and discharges with higher magnitude [14]. The challenges due to scaling down of MOSFET devices geometrics below 45nm are the main bottleneck due to the factors discussed above. The other possibility to reduce the power consumption is the reduction of power supply voltage level which is a dependent parameter on energy. This also contributes to leakage current. But energy-per-operation reduces during switching instance. In addition dynamic scaling can save some energy in multicore devices.

1.2 BACKGROUND METHODOLOGY

Discrete Wavelet Transform (DWT) decomposes the discretized biomedical signal using time shifting, dilated / contracted of the wavelets. One of the main block in the complete system is the preprocessing unit which adopts methods based on time analysis. Statistical analysis and numerical methods. In recent years telemedicine adopts methods based on medical data analysis and transmission of data. In DWT computation the given input biomedical data is decomposed into sub bands corresponds to low pass and high pass sub band spectrum. The filters are designed using Infinite Impulse response and finite impulse response (FIR) filters. The IIR filter is not suitable for biomedical application where the linear phase is required. So most of the filters are designed using FIR. Several algorithms are implemented using different VLSI architectures. The DWT based methods were used in long time for the analysis of biomedical signals. In image processing the architectures should be computationally stable and efficient. The two dimensional (2D) discrete wavelet transform is been used in several applications. The implementation of 2D DWT is a challenge using CMOS technology for miniature device (65nm minimum). For applications like biomedical engineering the area and power consumption is to be reduced, so the need for an alternate solution arises. The sub threshold current reduction is less and the leakage current reduction saves some power. The computations in the biomedical signal processing is more, the leakage current in every processing steps will contribute to higher power consumption. In sub -25nm region, transistor channel should be electrostatic controlled for the reduction of threshold voltage. At the same time the gate overdrive voltage should be increased without increasing the sub-threshold current.

1.3 FINFET TECHNOLOGY

In recent years, the fabrication in nanometre technologies have improved in capacity and at the same time the compatibility with past devices for fabrication was improved. The operating speed and power consumption was minimized using the battery. The consumer requirements especially in biomedical systems like the present work requires higher computation methods to attain several features. This led to alternate device uses and power supply options. On the other hand CMOS devices below the 45nm with high package density consumed more power for the highest performance. Therefore, a new device which can handle high speed, package density and power efficiency made this thesis to explore Fin type Field Effect Transistors (FinFET). The device material and process technology were compatible with CMOS with promising performance especially when processing elements were designed (Sujatha et al. 2018).

1.3.1 Device Structure of FinFET:

FinFET technology in recent years were used in several integrated circuits based application like 65 nm and 45 nm. The superior levels of scalability and high device integration within integrated circuits increased the use of FinFET thereby replaced MOSFET at submicron level. The short channel effects removed through the FET structure with fins as shown in Fig.2. The Silicon on Insulator (SoI) finger termed fin is designed with silicon fin nitride and thin pad oxide protects the fins gate poly SiGe etching. Here a single gate is stacked on top of two vertical gates. This increase the surface area for electrons to travel. The threshold voltage can be adjusted by using the gate control voltage. Fig.3(a) shows the FinFET dimensions and layouts.

The structure consists of a front gate, back gate, fin, source and drain. The fin channel is controlled the conduction and also the threshold voltage. The Vt is controlled by the back gate potential. The poly silicon layer forms the Gate.

There are three different modes of operation in FinFET multi-gate devices. They are

- Shorted Gate (SG-mode)
- Low Power (LP-mode)
- Independent Gate (IG-mode).

Each operating mode has its own features and characteristics. These features of the device make it more flexible. Greater performance can be achieved by low off-state current of LP mode. In LP-mode P-FinFET the bias voltage is 1.2V whereas in LP-mode N-FinFET the bias voltage is 0.2V. In SO-mode of operation in FinFET device offers greater on-state current and greater switching speed. We use Predictive Technology Model (PTM) for carrying out simulations from which is it noted that the leakage power dissipation is considerably minimized. 32nm FinFET technology is utilized here.

In FinFET the channel is perpendicular to wafer plane and the flow of current is parallel to wafer plane making it a quasi-planar device. The continuous scaling in MOSFET is not increasing its performance for devices smaller than 45nm due to the leakage current associated with it and the device-to-device variability.

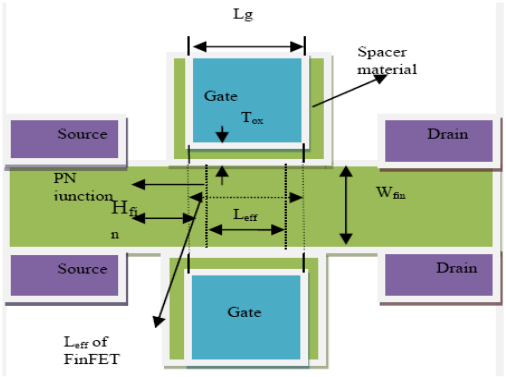

Fig.1. FinFET structure: Lg= gate length, Tox= gate oxide thickness, Leff= effective channel length, Hfin= height of fin, Wfin= width of fin

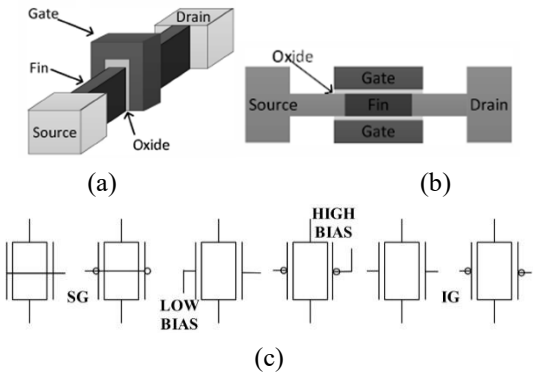

Fig.2 (a) Three dimensional structure, (b) Cross- sectional Top view, (c) Electrical mode schematic

1.3.2 Double-Gate FinFET Transistor:

Double-gated FinFET devices are the improved and modernized technology design in the digital and analog circuits. The DG- FinFET has two gates within it and they are named as front gate and back gate respectively. These gates are used in two ways. One way is to short these two gates into one. By this way the area of the circuit, transistors and capacitance of the circuit are all reduced. The other ways to use these gates are by giving varying voltage to each gate, such that the back-gate is biased with reverse voltage while the front gate is biased with high voltage. Parallel transistors are the pair of transistor in which the source and drain terminal of both transistors are connected together (ie., both source terminal are connected and both drain terminal are connected). Short channel effects are dealt better by the double gate FinFET that has control over the opposite direction. This type of FinFET also has better resistance to leakage current. They also have many benefits such as better control even without scaling, high channel doping density. This also reduces the number of transistors to be used to perform a certain operation when compared to CMOS device.

1.3.3 Predictive Technology Models for FinFET:

An accurate and customizable model is always required to explore the features of future technologies before it is fully developed. Predictive Technology Model (PTM) were used in this work for CMOS and FinFET. Berkeley Predictive Technology Model (BPTM) evolved into PTM with novel features like new methodology prediction and scalable device for FinFET. The models of multi gate devices with compatibility in circuit simulators like SPICE is required. PTM contains models which are scalable for strained Si, multiple V_{th} and High K Metal Gate (HKMG) processes for FinFET structure. Technology enhancements influenced the models to constitute primary parameters. From the literature is verified that the thermal effect, mobility and V_{th} is not changing on scaling.

2. EXISTING DWT ARCHITECTURES FOR BIOMEDICAL APPLICATION

The existing methods employs VLSI based CMOS devices in it for lifting based and convolution based 1-D DWT and 2-D DWT. The construction of overall design is done with the elements such as adders, multipliers and delay elements. Parallel stage based lifting DWT architecture is fast due to its lower delay. This design uses a single floating point adder and a fused multiplier. Both the convolution based DWT and lifting based DWT are compared and observed keenly. The Results from the observation proved that the performance and efficiency of lifting based DWT had obtained considerable good results than the convolution based DWT. The complex parameter in computation was repaired by replacing the higher and lower triangular matrices with low pass and high pass filters.

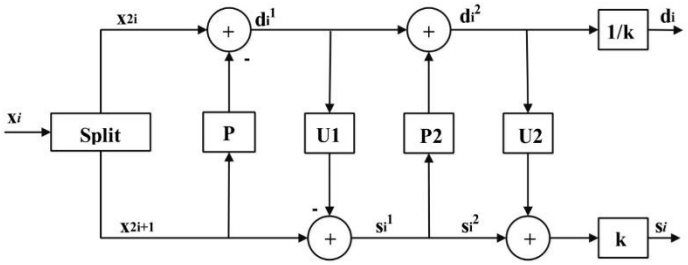

Fig.3. Architecture of Lifting Scheme

The illustration of lifting scheme is given in Figure 3. The two states (two prediction states and two updating states) are responsible for variation in the coefficients of the lifting scheme. The controller chooses the effective lifting coefficient for each clock cycle. Even clock cycle is used to perform first half of the operation (ie., to perform operation of even samples) and the next half of the clock cycle is used for odd samples. Consider an image processing operation in which the input pixels are arranged in row and they are split as even and odd samples such that one clock cycle is used for performing operation on one pixel. Then they are driven by lifting coefficients a, b, c and d. Each pair consists of a low pass and high pass coefficients

2.1.1 Limitation of Existing Methodology:

The Multipliers employed in the above methods gives rise to a greater critical path values. The critical path, computations and delay have direct relationship with each other. Hence the rise in critical path leads to complex computation and maximizes the delay of the overall design. So the DWT architectures employing multipliers was very slow and inefficient. Fabrication of below 45nm leads to many complications such as leakage current, greater field effects, limitation in threshold values, delays in interconnects and series of fluctuations in dopants. In addition to this, the fabrication of below 65nm leads to second order effects.

Power optimization was done with the view of Voltage (V_{DD}), Thickness of gate oxide (t_{ox}), threshold voltages (V_{th}), Length of channel (L), optimization of power. The bulk and wide area of DWT architectural design arises as a result of convolution based DWT model. Taking all the existing methods account, it is obvious that the multiplier less model based on pipeline architecture for 2-D DWT based on lifting approach operates faster than all other methods and the design of multiplier using shifter and adder logic gives a great reduction in critical delay when compared with all other existing methods.

The conventional lifting based architecture has multiplier blocks which increase the critical delay. Designing the wavelet transform without multiplier is a effective task especially for the 2-D image analysis. Without multiplier wavelet implementation in forward and inverse transforms may find efficient. The proposed lifting scheme for reduces critical path through multiplier less and provides low power, area and high throughput.

The architecture is Multiplier less in the predict and update stage and the implementation carried out in synopsis hspice

3. PROPOSED MULTIPLIER LESS FINFET BASED DWT -LIFTING SCHEME

The Lifting steps for 9/7 filter, Predict1, Update1, Predict2, Update2 modules done with multiplier less architecture. The architecture here presented has two stages of predict and update blocks. In conventional circuit the critical path is mainly depends on the multiplier. But here in the multiplier less architecture the critical delay is dependent on the adder only. In addition, the operating speed of the DWT depends on the critical path delay, but that delay can be reduced by using pipeline architectures. The lifting stages pipelined will improve the operational speed of row processor/column processors of 2D. The proposed FinFET based architecture will be designed using adders/subtracters and shifters. In this research work to reduce the problems faced in conventional methods, a FinFET based lifting Discrete Wavelet Transform for biomedical image processing is presented. The proposed method is designed without multipliers using FinFET devices. FinFET based design and CMOS results were compared. The implementation of lifting scheme has three steps. The first step is to split the data into two parts as even and odd. The second step is to make prediction. And at the last step is updating samples. During updating the even samples are updated with computed odd samples. These three steps are repeated to all data samples. This method has low complexity hence they are used efficiently. Figure 5 and 6 shows lifting steps for 9/7 filter, Predict1, Update1, Predict2, Update2

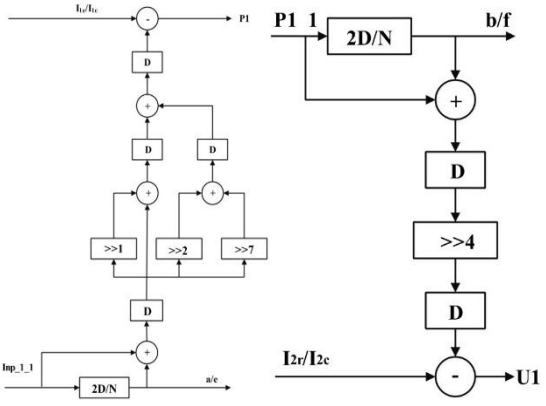

Fig.4. Architecture of Predict 1 and update 1 Stage without multiplier

For computation only adders are used with a critical path of one adder delay. To boost up the speed of computation pipelining can be inherited in predict and update module. Predict and update modules perform row and column processing in lifting stage. Our proposed work is constructed with the use of adders/subtractors and shifters and it employs 14nm FinFET technology along with lifting DWT architecture. The results of proposed FinFET technology are compared with the conventional CMOS technology. The proposed work is a multiplier less system. The design of proposed system can be done only with adders, subtractors and shift registers. Power consumption is our proposed design is lower. The table 1 represents that FinFET based blocks has utilized minimum power which is10 times efficient in power consumption. But shifter and multiplexer had power efficiency about four orders than CMOS.

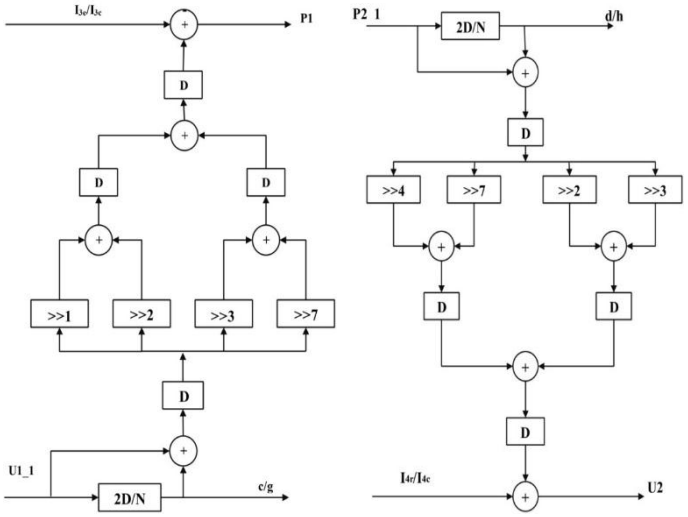

Fig.6. Architecture Of Predict 2 And Update 2 Stage Without Multiplier

The results of various unit corresponding to the various design is shown in Table.1. The circuits were simulated with Synopsis HSPICE. The Table.1 shows that the FinFET based blocks has consumed low power when compared to the existing methods.

Table.1. Power Analysis of Existing and Proposed Design

Block	CMOS Average Power (W)	CMOS Peak Power (W)	FinFET Average Power (W)	FinFET Peak Power (W)
Adder	55µ	55µ	1.3µ	1.32µ
Subtractor	727µ	723µ	33µ	34µ
Shift Register	208µ	5.03m	835 µ	377 µ
Latch	53 µ	1.2m	1.5 µ	973 µ
Multiplexer	381 µ	433 µ	92n	94n
Delay unit	54 µ	1.2m	1.5 µ	973 µ

The lifting based discrete wavelet transform architecture was designed with the FinFET device limits the leakage current and provides lower average and peak power. Synopsis HSPICE is used here for implementation. The results are summarized in Table.1. The Table.2 shows a comparative analysis on the MOSFET and FinFET design.

Table.2. Comparison Table

Stage	Average Energy		Average Power		Average Current	
	MOSFET	FinFET	MOSFET	FinFET	MOSFET	FinFET
Predict 1	28.3p	3.9p	4.2m	567u	4.26m	562u
Update 1	19.8p	698f	3.61m	120u	3.61m	110u
Predict 2	32.9p	2.91p	5.22m	445u	5.24m	431u
Update 2	33.8p	2.92p	5.23m	452u	5.33m	435u

4. CONCLUSION

Over the past few years innovation in green computing makes the multimedia applications simple and efficient. Many devices are designed in a energy efficient manner to reduce power consumption. For image processing most commonly used device is CMOS. But CMOS is not efficient for scaling below 45nm. Channel length below 45nm in CMOS will lead to various effects, out of which the major issue is Short Channel Effects (SCE). 2-D image analysis can be performed effectively using DWT (Discrete Wavelet Transform). Yet the design of DWT consists of more number of multipliers which results in increase in delay. Convolution based process use filter in its design, due to which it becomes harder to attain sharp cutoff. In this paper a novel method is presented for the lifting based 2D Discrete Wavelet Transform implemented using FinFET. This method is a multiplier-less design. They do not have multipliers to eliminate delay. From the analysis it is been observed that the FinFET based design outperforms CMOS.

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