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# IMPACT ANALYSIS OF DUAL EDGE TRIGGERING FLIP-FLOP USING SINGLE PHASE SINGLE-TRANSISTOR-CLOCKED BUFFER WITH LOW POWER REDUNDANT TRANSMISSION

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***Abstract***

***The Power Consumption (PC) of VLSI circuits is a crucial reason that requires careful consideration especially for packages that must have the lowest possible strength. Power dissipation in Flip-Flops (FF) and clock distribution networks must be minimized because contemporary portable digital circuits have a very constrained strength budget. Additionally, because of the limited time finances at high frequency operation turn-flop latency must be minimized. Thus it is crucial to design with low latency and electricity intake in mind when using current VLSI generation. A processors clocking mechanism is mainly made up of clock supply networks and Flip-Flops (FF). Because the alternative clock part is designed for data processing the traditional single-phase clock FFs method introduces statistics by using the best clock part at a time causing a redundant strength overhead. Dual edge-triggering (DET) FFs use each clock edge (CE) to technique facts permitting them to cut the clock frequency in half by preserving throughput. To address these issues a useful dual-edge-triggering (DET) FF that eliminates clock redundant transitions (RTs) entirely and improves performance through feel amplification is proposed. The first of its kind to totally eliminate the clock and inner redundant switching is the proposed DET FF. FF design employs zero redundant transition (RT) single-transistor-clocked (STC). A sensing amplifier primarily based flip-flop (SAFF) that can operate dependably over a broad voltage and temperature range is included in this painting. Similar to a differential sensing stage turn flops that are primarily based on feel amplifiers have a slave latching degree. The purpose of the sensing degree is to report information at the rising Edge (RE)and falling edges (FE) of the clock while the sense amplifiers output is sustained for the duration of the clocks effective half cycle. Consequently, the size restrictions associated with traditional pulse-precipitated flip-flops are eliminated. SAFF (Sense-Amplifier FF) has various capabilities such as reduced clock load shorter hold intervals and a poor or almost zero setup time. SAFFs outperform pulse-induced turn flips and master slave flip flips when it comes to low voltage operation. Utilizing 22 nm CMOS technology the cautioned hybrid layout is designed using the MICROWIND device. Power-delay-product (PDP) and proximity electricity delay are compared between the current DET designs and the proposed design.***

***Keywords:***

***Power Consumption, GDI technique, Universal Gates, FD-SOI and PDP***

## 1. INTRODUCTION

PC has become a major concern for CMOS digital designers due to the demands of modern GPU/AI neural network (NN) processors. AI training requires twice as much processing power every three to four months [1]. It has been believed that optimizing a modern processors power is essential to addressing the previously mentioned power dissipation problem because the clocking structure can use more than half of its power [2].

A processors clocking system is primarily composed of FF and clock distribution networks. The power overhead of typical single-phase clock (SPC) FFs is needless since they only process input data on one clock edge at a time leaving the other clock edge is new for data processing. By processing data using both clock edges, DET front-end processors can cut the clock frequency in half and conserve power without compromising throughput. A new topology that utilizes a True SPC (TSPC) is proposed in this brief to further reduce the EC of the DET FFs. These are the primary contributions of the brief. The suggested DET FF totally does away with the clock and internal redundant switching for the first time. Our FF design suggests using zero RT STCB.

The fundamental unit of data path structure is the flip-flop. They allow data processing via combinational circuits as well as operation synchronization at a specific clock frequency. These essential elements serve as the foundation for the digital electronics systems present in computers and several other types of devices. Simple devices are known as latches and they can be either basic or timed flip-flops. The primary purpose of a level-sensitive latch is as a storage element. Additionally, flip-flops are timed devices. A positive or negative going edge is the only kind of clock edge that can change the output of a flip-flop because they are edge-sensitive [3-6]. For short periods of time they are commonly used in computational circuits to receive and store data so that other circuits in the system can process it further. Flip-flops are devices that retains information at the RE and FE of clock pulses. They are called DET FF and are used as inputs in a range of combinational or sequential circuits. Flip-flops are appropriate for use in other combinational or sequential circuits because of their capacity to store data at both the RE and FE of clock signals.

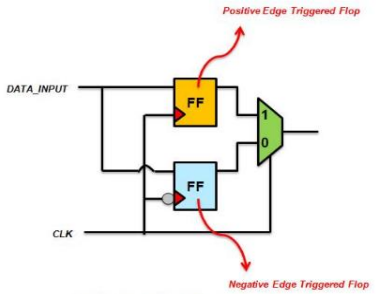


Fig.1. Schematic of DET FF

VLSI designers in that earlier era were more concerned with the circuits area and performance. Cost and dependability also became very important while power consumption was viewed as a secondary consideration. However, this has changed dramatically in recent years with power now being seen in the same light as area and velocity. PC and propagation delay are the two primary performance problems. The PC of an integrated

circuit is one of its primary limits. Performance and power are typically traded off in some way. Three distinct methods exist for CMOS circuits to lose power. The first is static power loss also known as leakage which is unaffected by switching activity but linked to the LS of the circuits. When both the NMOS and PMOS transistors in the circuit are turned on the second is power dissipation from short circuits. A sequential component that samples data at both the positive and negative edges of the clock is called a DET FF. This could be useful in applications with extremely high throughput. The lack of a dual edge induced flip in contemporary conventional cell libraries may surprise you! That means that the designer can use the conventional cells that are on hand to create a DET FF.

## 2. LITERATURE SURVEY

### 2.1 TSPC FF

The power of digital systems can be greatly decreased by improving the power consumption of FF which are crucial components. This article suggests a retentive TSPC FF that uses less energy. The recommended TSPC FF only precharges when required when the input-aware precharge strategy is used [7] Transistor-level optimization and the use of floating-node analysis are further measures to guarantee the FFs outstanding energy efficiency without appreciably expanding their area. According to SMIC 55-nm CMOS post-layout simulations it is shown that the recommended FFs power consumption at 10% data activity is 83%–38% lower than that of a conventional transmission-gate FF at 1. 2 V supply voltage. The reduction rate increases at 98% and the proposed FF uses just 0 at 10% data activity. Two thirds less than TGFF. According to evaluations of ten test chips the recommended FF has an extremely high energy efficiency. For FFs a CK-to-Q delay is also recommended. when the supply voltage is adjusted to be 18% lower than TGFFs.

### 2.2 PULSE-TRIGGERED CNTFET-BASED FF

The two main issues facing modern electronics are scaling the devices and lowering PC. One of the most important components of electrical devices is the FF. As a result, when these FFs are improved the electronic devices perform better. [8] This work suggests a novel pulse-activated D-Flip structure based on CNTFETs. A signal feed-through technique is used in this structure to reduce the number of CNTFETs needed for the 0 to 1 transition. Using only two CNTFETs also improves the discharging path reducing the transition delay time from 1 to 0. The new structure in H spice is replicated using the Stanford model. In terms of PC, the D-to-Q delay (D2Q) PDP, and the number of transistors needed, the output results indicate that the suggested design outperforms the current pulse-triggered FF (PTFF) structures by a large margin.

Scaling the devices and reducing their power consumption are the two primary challenges facing modern electronics. Flip-flops (FF) are among the basic parts of electrical devices. A novel pulse-activated D-Flip structure based on CNTFETs is proposed in this work. This topology uses fewer CNTFETs to accomplish the 0 to 1 transition by using the signal feed-through technique. Additionally, by two CNTFETs, the discharging path is enhanced to reduce the 1 to 0 transition delay time. Then use the Stanford model to reproduce the new design in H spice. In terms of PC D2Q delay PDP and required transistor count the results show that the design performs well than the current PTFF structures.

### 2.3 EXPLICIT-PULSED DET SAFF WITH HIGH EE

A novel DET-SAFF with good performance and low PC is presented in this work. Conditional pre-charging and a DET mechanism combined with the new fast latch could allow the DET-SAFF to operate with little delay and low PC. The PC of a clock-gated SAFF is significantly reduced at low switching activities. The given DET-SAFF exhibits both high-speed and LP characteristics with power reductions of up to 33 according to extensive post-layout simulations. 5% and up to 43% in delays. correspondingly 3% of the prior art. The suggested CG-SAFF operates more effectively in terms of power reduction when the α is below 0.5. Up to 86% of the power can be saved by CG-SAFF when there is no input switching activity. Finally, improvements to the suggested circuit resulted in a higher DET-SAFF common-mode rejection ratio (CMRR).

### 2.4 SEQUENTIAL ELEMENTS FOR LP CLOCKING SYSTEM DESIGN

A study of design strategies for LP clocking systems is presented. Reducing the clock load capacity can be achieved most effectively by using fewer clocked transistors. [9-10] To address this we suggest a unique shared flip-flop called a clocked pair which lowers the quantity of locally clocked transistors by about 40%. A twenty-four percent reduction in clock driving power is achievable. The new flip-flop can also be readily modified to support double edge clocking and low swing in order to create clocking systems.

### 2.5 USING SEVERAL C-ELEMENTS, LOW POWER DET FLIP-FLOPS

Static DET FF that display unusual circuit behaviour when C-elements are incorporated into the design, and it is presented in this research. Two high-performance models that outperform the conventional Latch-MUX DET FF because none of their internal circuit nodes react to input changes are among the five distinct DET FFs for demonstration. One common feature caused by input glitches is the low energy dissipation of the flip-flops that are shown. New and existing DET FF are compared using 28nm CMOS technology [11]. The authors shown to have better features for a range of switching operations including power and PDP. The suggested designs' resilience to PVT fluctuations is shown by comprehensive Monte Carlo and voltage scaling simulations.

### 2.6 21-TRANSISTOR FLIP-FLOP THAT IS FULLY STATIC AND TOPOLOGICALLY COMPRESSED, REQUIRING 75% LESS POWER.

The use of a topological compression FF (TCFF) a very LP FF is advised. In the absence of data activity, the FF reduces PC by 75% in comparison to traditional FF [12]. This FF has the highest power reduction ratio among those that have been observed so far. In order to accomplish this reduction topological compression techniques and an unconventional latch structure are used to

combine equivalent transistor elements. The same cell of the FF can be used, but lowering PC due to the LP supply and the few transistors (only three) connected to the clock signal. Its fully static operation also makes the cell unaffected to differences in supply voltage and input slew. With the same layout area and system performance the suggested FF can be used in place of nearly all conventional FFs according to an chip design created using 40 nm CMOS technology.

### 2.7 LP DUAL DATA RATE (DDR) FF

The implementation of DE FF has drawn the interest of numerous scholars recently as a means of lowering PC and maintaining the functionality of digital systems. The new low-power and dependable DE FF is demonstrated in this paper using c-elements. The suggested architecture [15] captures the data using direct clock pulses, lowering the clock dynamic PC by a factor of two in contrast to the present DDR FF. This current DDR FF requires extra pulse generator circuitry for the clock signal. Additionally, because of its low transistor count and robustness it is a simpler and more reliable alternative to DDR FF. The suggested DDR-FFs 45nm CMOS technology allows it to use 12% less $C_{2Q}$ delay and 32% LP than the p-DSFF (explicit-pulsed static hybrid flop) [13-14]. The suggested DDR-FF has a 41 percent better PDP than ep-DSFF (explicit-pulsed static FF) The suggested DDR-FF is an ASIC design flow that is easy to incorporate into cell libraries and has a low PC and high performance with only 24 transistors.

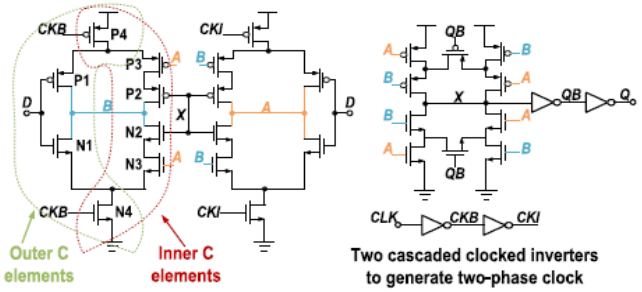


Fig.2. Two-phase clocking in the TSPC DET sense amplifier

## 3. ANALYSIS TSPC SINGLE TRANSISTOR CLOCKED DET

The static floating node C element is one of the common DET FFs. Full static (FS) DET as shown in the Fig.2. In the left side of Fig.2, 2 cascaded inverters generate the two clock phases ($CK_B$ and $CK_I$). Fig.2 illustrates the use of two-phase clocking in the TSPC DET sense amplifier DET S-DET CBS DEFF DE explicit-pulsed static FF (ep DSFF) reduced implementation DEFF and c-element DDR (CDDR) Flip. The cascaded inverters continue to switch continuously when the input data does not change, producing clock RT power. The bottom right corner of Fig.2 serves as an illustration of the redundant-transition behaviour present in FN_C-DET. The outer-C elements (P1, P4, N1, N4) and the inner- and outer-C components (P2, P3, P4, N2, N3, N4) at node B clash during the transition phase of FN_C-DET, similar to a short circuit. Node A also has an analogous argument.

### 3.1 SYNCHRONOUS SHIFT IN SINGLE-PHASE-CLOCK DETFF

To prevent cascaded clocked inverters and lower clock conversion power in dual-phase DET, single-phase DET FFs are suggested. Fig.3 is represented by FS TSPC DET. The third technique which has a complex design is one of them. Since FS TSPC only uses one clock phase it lacks an explicit clocked inverter [16]. However when the input is constant an implicit internal RT occurs. The NOR structure in the centre of the image turns into an inverter with one clock NMOS and one timed PMOS if D remains at 1 and DP remains at 0. Thus the two clocked transistors continuous switching has resulted in the implicit-redundant transition. Likewise the NAND structure will transform into an inverter with a continuous switching issue resulting in the implicit-redundant transition if DN remains at 1. The implicit RT has an effect on the TSPC DET, a different static TSPC DET. The Fig.3 shows Fully-static TSPC DET.

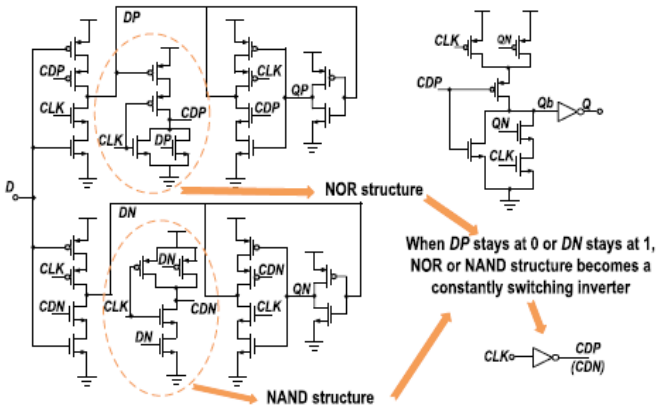


Fig.3. Fully-static TSPC DET

### 3.2 CLOCK WITH TSPC FF

To simplify clocking and reduce power consumption digital circuits especially sequential logic circuits employ a design technique known as TSPC.

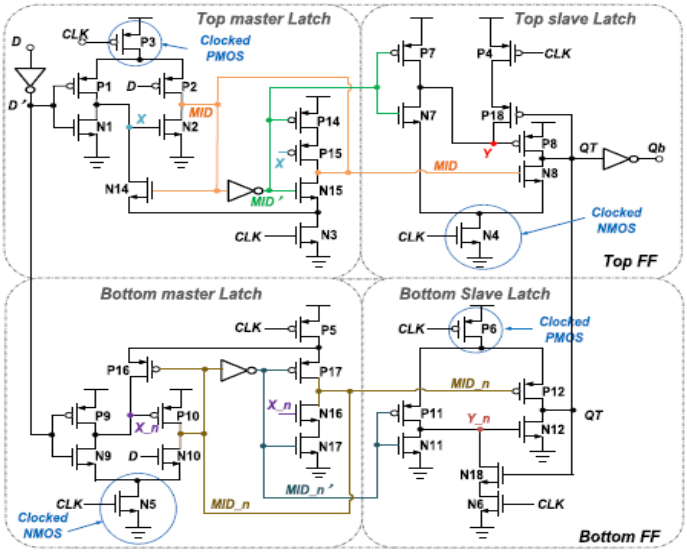


Fig.4. TSPC single transistor clocked DET, STC-DET.

This technique is widely used in the field of CMOS technology. An extensive analysis of TSPC and its significance may be found below Fig.4.

In most digital systems clock signals are used to synchronize data and control the sequence of events. Conventional systems commonly use multiple-phase clocking techniques where a number of clock signals at different phases control the circuits operation. Nevertheless building circuits that use multiple clock phases can be challenging and energy-inefficient. The clocking process was made simpler by TSPC by doing away with the need for multiple clock phases. The previously noted RT among 2 clocked transistors (one PMOS and one NMOS) is eliminated by using an LP TSPC DET FF with a unique redundant-free STCB architecture dual-edge FFs. The master slave-latch (MSL) structure is used by STC-DET, as shown in the Fig.4. On both the top and bottom there are flip-flops. A positive clock edge causes the top FF to sample the data and a negative clock edge causes the bottom FF to sample the input. Below is a description of the STC-DET FF-specific functions.

Consequently, Node X becomes D″ (see Figures upper left). At the point, transistors (P2 N2) are comparable to a virtual inverter (VI), Fig.5 illustrates a simplified logic design. If CLK = 0 in the top FFs data sampling (DS) path, Node X turns into D** and the top master latches clocked PMOS P3 activates.

In Fig.5, the upper slave latch, controlled by the timed NMOS N4, is deactivated. In the upper master latch, the input is directed to MI D (refer to the arrow in the upper left corner of the Fig.5) since node Y will not be 0, as PMOS P8 is deactivated due to CLK = 0. As QT in the upper FF is not linked to $V_{DD}$ or GND, it remains in a floating state (see to the top left of Fig.5.a). The negative-triggered STCBs signal sampling method employs a single clocked transistor (P3) (N1 N2 P1 P2 P3), as illustrated in Fig.4. The keeper employs an additional clocked NMOS transistor N3 beside transistor P3. This is located in the upper master latch instead of the DS path (refer to the upper left section of Fig.5). The number is four. In the DS path, each of the four clocked transistors (P3, N4, N5, and P6) is denoted by an arrow. The primary flip-flop is linked to a secondary positive-triggered static toggle cell, which is composed of transistors N4, N7, N8, P7, and P8, as illustrated in Fig.4. Furthermore, the pathways to P1 and N2 are inactive since the primary master latches timed PMOS P3 is deactivated at CLK = 1. The keeper (P14 P15 N3 N15) maintains MI D. LS intact, but the pull-down keeper (N3 & N14) will retain X when its logic state (LS) is 0. Conversely, Y was modified to MI D″ or MI D due to the temporal activations of the top slave latches NMOS N4. The arrow in the upper right corner of Fig.4(a) indicates that transistors (N8 P8) functioned as a voltage inverter, allowing the signal from MI D, which occurs immediately before the clock RE, to advance to QT. Consequently, at the positive edge (PE) of the clock, the upper flip-flop is engaged.

Upon the activation of the bottom master latches, NMOS N5 deactivates at CLK = 0 in the lower flip-flop (see to Fig.5, lower left). If the LS of $X_n$ is 1, the pull-up keeper (P5 & P16) will sustain the LS of MI $D_n$, while the keeper (P5 P17 N16 N17) will perform the same function, as the routes to N9 and P10 are inactive. In the upper section of the picture, you can find the clocked PMOS P6 in the lower slave latch (bottom right). Occurs when $Y_n$ transitions to MI $D_n$″ or MI $D_n$ when CLK is equal to 0.4. Prior to the clock reaching QT, FE emits the MI Dn signal, generated by P12 and N12 functioning as a VI (refer to the arrow in the left section of Fig.5 (b). If D stays the same there wont be any switching so there wont be any repetitive transitions. Two more STCBs are built using the transistors P9 P10 N5 N9 N10 and N11 N12 P6 P11 P12 in the lower FF.

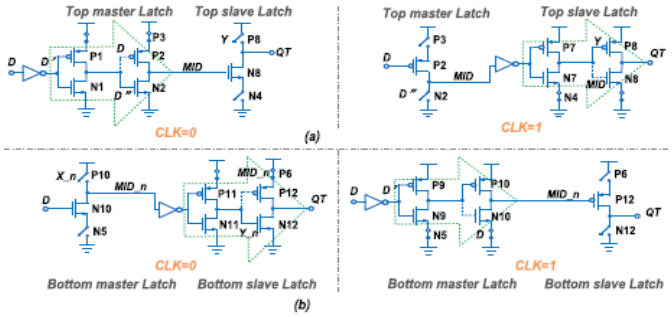


Fig.5. Procedure of the STC-DET: (a) Equivalent logic diagram of top FF (b) Equivalent logic diagram of bottom FF

The STC-DET may sample input at both CE because the PE of the clock and NE of the clock engage the top and bottom slave latches respectively. One of the two slave latches is always transparent while the other is always opaque as they are both activated by different CE. As a result, there is no interference when the slave latches outputs are coupled at QT. Its transparent connection to the ground or QT supply further ensures that it will never be a floating node. Simply sending the left-hand master latches an enable signal and a scan input, STC-DET scannable may readily support the design for test. Additionally, keepers can be added to the bottom or top FF ends respectively to change the FF design to a single edge.

## 4. RESULTS AND DISCUSSION

Eight nodes in total provide the clock or CLK. D serves as the FFs input and QT serves as its output. The value of $Q_b$ is the inverse of $Q_T$. When D changes from 1 to 0 or from 0 to 1 signal $Q_T$ is informed. This transition occurs on the next falling or rising edge. There are two flip-flops in the design: one at the top and one at the bottom. When the CE is positive the top FF samples the data and when the CE is negative the bottom FF samples the input.

When CLK = 0, the node Xs DS path in the upper flip-flops transitions to D. The arrow above the D″ input in the upper left corner of the image indicates its connection to MID in the top master latch. PMOS P8 is deactivated; however, NMOS N4 in the upper slave latch is also deactivated when CLK = 0, indicating that node Y will not be clocked to 0. The device is essentially D. The primary master latches, timed by PMOS P3, engage the combining transistors (P2 N2) to generate a VI. NMOS N4 is deactivated at the upper slave latch, leading to PMOS P8 being deactivated, as CLK = 0 signifies that node Y will not be clocked to 0. Subsequently, the input is directed to the M I D in the top master latch (refer to the arrow in the upper left corner of the photos). The QT in the upper FF is unconnected to both VDD and GND, rendering it floating. A negative-triggered STCB, consisting of transistors N1, N2, P1 to P3, employs a solitary clock transistor P3 within its signal sampling circuit. In STC DET, there is no resistance between one clocked PMOS and one

NMOS, whereas such resistance exists in FNC DET and FSTSPC. There is also no contention.

The primary master latch comprises the clocked transistor P3 and an additional clocked NMOS transistor N3, which functions as the keeper's data sampling pathway. Transistors (N4-7, N8, P7, and P8) are utilised to fabricate a second positive-triggered STCB in the upper flip-flop. As P1 is linked to the routes, the LS is presently zero. When C L K = 1, the top master latches are disabled. The rationale for this is that the clocked PMOS P3 is presently deactivated. The logical condition of MIDs. Maintain clocks N3, N15, P14, and P15 in a logic state of 0 to preserve the pull-down keeper (N14, N3). Nonetheless, the timed NMOS N4 activates at the upper slave latch Y as M I D″ or M I D. Immediately prior to the clock's rising edge, the M I D signal is transmitted to QT by transistors (P8 & N8) functioning as a voltage inverter. Consequently, the positive edge of the clock activates the top flip-flop.

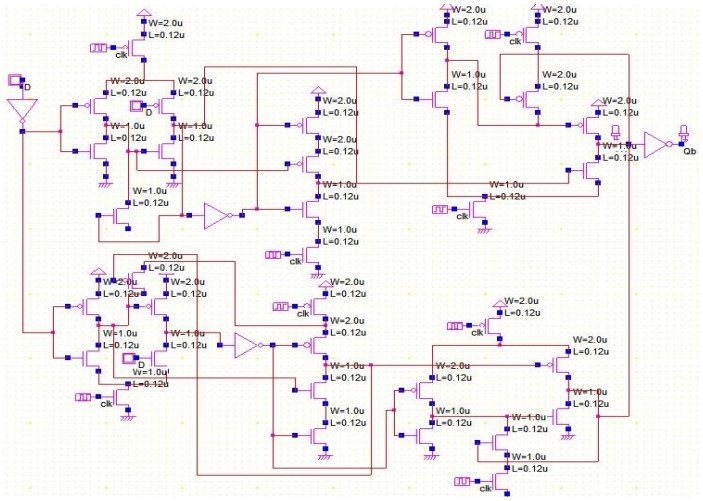

Fig.6. STC-DET Design

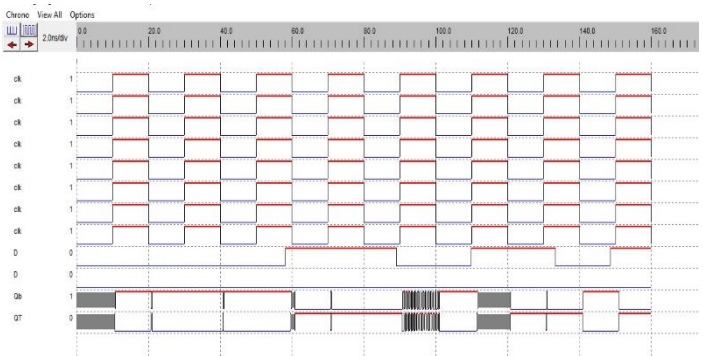

Fig.7 STC-DET Simulation

The bottom master latch N5s timed NMOS turns off when CLK = 0 in the bottom FF. As a result if $X_n$ is 1 keeper (P5 P17 N16 N17) maintains the logic state of MIDn while keeper (P16 P5) maintains the logic state of $X_n$. Consequently, the roads that lead to N9 and P10 are blocked. However, the timed PMOS P6 in the top Fig.in the bottom slave latch activates when C L K = 0. As a result P12 & N12 function as a virtual inverter changing $Y_n$ to $MID_n$ ″ or simply MIDn. The clocks falling edge is just before the signal from $MID_n$ flows to QT. The bottom FF is very sensitive on the clocks NE. There won't be any repetitive transitions if D stays at the similar number, because there won't be any switching. Constructed by transistors the other two STCBs in the lower FF are P9 P10 N5 N9 N10 and N11 N12 P6 P11 P12. PMOS P6 cuts off the paths connected to P11 when the bottom slave latches are clocked and N12 will follow suit.

NMOS N5 is activated when C L K = 1 and the bottom master latches are clocked. The bottom master latch goes to $MID_n$ since Xn will be D″ input D in other words P10 and N10 act as virtual inverters. As was previously mentioned QT is a nonfloating node when C L K = 1 because it has an additional link in the top FF. Here, D has no influence on QT, there is still no duplication transition if it remains at the same value. The clock's PE and NE activates the top and bottom slave latches. The STC-DET may sample input at both CEs using these. The two slave latches are always transparent and opaque, because they are activated by different CE. Consequently, there is no interference when the slave latches' outputs are connected at QT. Its connection to the QTs supply or ground makes it a non-floating node at all times. Enabling signal is added and inputs are scanned on the left-side master latches, STC-DET can also easily implement the DFT. Keepers can be added to the top or bottom FF, to convert it to a single-edge FF design.

## 5. DISCUSSION AND CONCLUSION

Using STCB, a novel LP RT-free FF called STC-DET is developed to completely remove RT in DET FFs. A single clocked transistor is present in both the positive-triggered STCB and negative-triggered STCB that make up the topology DS paths. This eliminates all internal RT between two clocked transistors and clock RT that were previously present in other DET designs. No complaints have been made against the proposed STC-DET either with a 10% switching activity at zero points 4 V and 8 V respectively. STC-DET uses 14% LP than the previous SOTA FN_C DET which uses 9 to 5% less. with different voltages as well (0 with switching activities below 20 percent (4-0 point 8V) the STC-DET takes LP of any DET design. Overall it also consumes the least amount of power alternating between 1 and 10% activity from 0 to 4. At 8V the suggested design performs 53 times better than FN_C-DET 4% and 51%. PDP (CQ) was at zero percent. The recommended STC-DET in the average switching activity range has the lowest PC and PDP of all the existing DET FFs.

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