HIGH-DIMENSIONAL PARAMETRIC OPTIMIZED APPROACH FOR FAULTS DETECTION IN ANALOG CIRCUITS

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Abstract

Assuring the efficiency and reliability of electronic systems relies heavily on finding parametric faults in analog circuits, which is especially important in highly precise sectors. A typical problem with conventional fault detection algorithms when working with highdimensional feature sets is the risk of over fitting, which can lead to higher computing costs and more acute accuracy. In response to these difficulties, this research presents a method, the High-Dimensional Parametric Optimized Approach (H-DPOA), which combines a Support Vector Machine model with a feature selection based on feature importance measure. By lowering the dataset's dimensionality and making features more significant in fault classification, the H-DPOA improves the model's performance and interpretability. The features that have been selected are subsequently utilized to sequence an improved support vector machine model, which aims to improve the detection accuracy of minor parametric errors while reducing the number of false positives. By analyzing benchmark analog circuit datasets extensively in simulation, the suggested method is proven to be valid. With less computing time required than conventional approaches, the results show that H-DPOA greatly improves fault identification rates. In areas where accurate fault identification is vital for preserving system integrity, such as telecommunications, industrial automation systems, and automotive electronics, this approach finds key application in fault diagnosis. The findings suggest that H-DPOA is a viable and scalable approach to diagnosing analog circuits, which could lead to research into automated fault detection and predictive maintenance for electronic systems.

Keywords:

Fault Diagnosis, Analog Circuits, Feature Importance, Feature Selection, Optimization, Support Vector Machine

1. INTRODUCTION

Traditional parametric fault detection in analog circuits uses threshold-based monitoring, circuit simulations, and human output response analysis [1]. During threshold-based monitoring, voltage, current, and frequency are compared to permissible limits. Deviations over these values indicate flaws [2]. Analog circuits can make mistakes due to small changes from outside factors or internal noise. This compromises results accuracy. Comparison with expected behaviour in normal and fault scenarios is another popular circuit simulation method [3]. Simulations can precisely mimic circuits' intended behaviour; they typically overlook unanticipated deviations and require extensive modelling to include them. Examining circuit outputs with Fourier and wavelet transforms illuminates the frequency and temporal domains. For multi-component complex circuits, this method can be time-consuming and error prone [4].

Due to their slowness and potential to miss fault components, these approaches are unsuited for high-dimensional data [5]. Even worse, traditional methods don't often use advanced data analytics, so they can't distinguish between slight fluctuations and serious defects, especially in analog circuits with overlapping characteristic values [6]. To boost detection accuracy, feature selection techniques must rank significant variables and machine learning algorithms like Support Vector Machine (SVM) must be used. An improved Support Vector Machine model or Feature Selection is two options [7]. Increased precision and decreased data dimensionality are the goals of these strategies for analog circuit parametric error detection [8].

Problems processing complicated and high-dimensional data plague parametric fault detection in analog circuits utilizing Optimized Support Vector Machine and Variable Ranking-based Feature Selection models [9]. It is difficult to extract essential elements that affect fault detection in analog circuit datasets due to their complexity and large number of features. Even with powerful Variable Ranking algorithms, missed significant qualities can lead to unnoticed defects, therefore feature selection is crucial [10]. Since selection is computationally resourceintensive, especially as circuit complexity increases, real-time systems have issues. Noise and overlapping fault indicators might lower detection accuracy for optimal SVM models [11].

Although these models classify well, they have issues. SVM factors like kernel selection and regularization must be optimized to avoid over fitting or under fitting, which complicates model training [12]. The computer cost of reliable fault detection increases with circuit component count, making scalability a difficulty. SVM models have trouble generalizing to varied circuit topologies [13]. Given varying operating circumstances and external influences, analog circuits can behave in many ways. Improve feature selection and model optimization methods frequently to overcome these problems and ensure accuracy, efficiency, and flexibility in a wide range of analog circuit settings [14].

Parametric faults identification in analog circuits is improved by combining a Feature Selection Method with a SVM model. Simplifying the data and focusing on parameters that affect problem identification helps this strategy prioritize essential circuit measurements for quicker problem diagnosis. Trained SVMs with fine-tuned hyper parameters can identify failure circumstances. This combination improves diagnostic precision and reduces computational work, making it perfect for real-time applications.

Analyzing complex analog circuits using this method is dependable and simple since it swiftly finds faults and reduces false positives. With the goal of improving the accuracy of parametric fault detection in analog circuits, especially for the detection of small flaws that are often missed by conventional methods and with the goal of reducing processing costs, a feature selection strategy that reduces the dataset's dimensionality while preserving crucial information for fault classification, the objective is to strengthen the SVM model's resistance to noise and parameter fluctuations in analog circuits to ensure the number of false positives may be decreased and the reliability of fault diagnostics can be enhanced. The structure of the investigation is outlined in this section, which covers the following topics: Section 2 delves into the topic of parameter fault detection in analog circuits utilizing an optimized SVM model and a feature selection method. The H-DPOA is the subject of Section 3 of the proposed work. An exhaustive examination, a comparison to prior approaches, and an examination of the consequences are presented in Section 4. Section 5 presents a thorough analysis of the results.

2. LITERATURE SURVEY

Modern electronic systems that depend on precision and reliability face challenges in analog circuit error diagnostics. Complex, non-linear behaviour or noisy surroundings cause accuracy, resilience, and processing efficiency challenges for conventional techniques. In [15], a method is suggested to diagnose analog circuit problems using a deep belief network (DBN) with GWO-optimized SVM, achieving 100% accuracy and 75-90% diagnosis time reduction. In [16], for the purpose of soft fault diagnosis in analog circuits, the suggested method employs a semi-supervised Gaussian mixture model (SGMM) in conjunction with manifold learning. This method is capable of delivering effective single and double fault identification, although having a somewhat lower accuracy for fixed-parameter defects.

In [17], high fault diagnosis accuracy and robustness against noise in analog circuits are achieved by the utilization of a denoising sparse deep auto-encoder (DSDAE) with support vector machine (SVM) that has been optimized by the slap swarm algorithm utilizing the proposed technique. In [18], a method with the goal of diagnosing nonlinear analog filters, the approach that has been proposed makes use of relief algorithm to optimize canonical correlation analysis. Combining relief algorithm to optimize canonical correlation analysis combines support vector machine (RCCA-SVM) with multi-group weighted feature fusion is the approach that has been proposed. By utilizing information from the temporal, statistical, and frequency domains, this strategy enhances the diagnostic accuracy, which eventually results in the successful detection of anomalies.

Using Class Activation Maps (CAM) deep learning, namely CNN with global average pooling, the study was developed in [19]. Its purpose is to discover parametric errors in analog filters. The study achieved 11.77% greater accuracy in simulated data compared to classical harmonic analysis. For fault isolation in analog circuits, the proposed method developed in [20] makes use of optimized empirical mode decomposition and non-dominated sorting genetic algorithm (N-DSGA). This method achieves excellent accuracy while reducing the amount of processing time required in comparison to earlier techniques.

In [21], detecting parametric errors in analog circuits are accomplished by the application of machine learning algorithm (MLA), with a particular emphasis on a quadratic discriminant classifier. This method achieves excellent classification accuracy across a variety of filter types. The H-DPOA outperforms current methods, combining optimal SVM models with feature selection improves defect detection, noise resistance, and false positives. H-DPOA is recommended for identifying analog circuit issues due to its efficiency and precision. It is more reliable and scalable than traditional and current methods.

3. HIGH-DIMENSIONAL PARAMETRIC OPTIMIZED APPROACH (H-DPOA)

In modern precision applications such as telecommunications, industrial automation and automotive electronics, identification of parametric faults in analog circuits is of utmost importance for efficiency and reliability in modern electronic systems. The conventional algorithms on the detection of faults result in overfitting, high processing cost and reduced accuracy if highdimensional feature sets are employed. An improved SVM model along with a feature importance measure based feature selection algorithm is proposed by this work as the H-DPOA. H-DPOA reduces the dimensionality to decrease processing time and false positives and focuses on the important characteristics such that fault detection accuracy increases.

3.1 DIMENSIONALITY REDUCTION THROUGH FEATURE IMPORTANCE MEASURE BASED FEATURE SELECTION

Feature selection based on feature importance measure can reduce the dimensionality of big datasets that contain highdimensional analog circuits. The techniques of traditional defect identification are prone to over-fitting and computational inefficiencies and have a reduced accuracy caused by the presence of large feature sets. On the contrary, the proposed feature selection algorithm removes the possibility of complexity and over-fitting while enhancing interpretability and ensuring that the model uses the most important parameters relevant to the classification of faults.

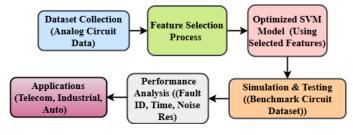


Fig.1. Optimized SVM Model Simulation & Testing

Feature selection and optimization are the two central ideas the Fig.1 delivers as one complete process for analyzing data from analog circuits in a machine learning-driven approach. To start with, the first step involved is gathering data related to relevant analog circuits as the basis for further analysis. After gathering data, the second step involved is feature selection, which refers to selecting significant variables. The basic reason behind this step is a dimensionality reduction of the data, which also facilitates an analysis. The most important things will be focused upon, and the model's efficiency and accuracy both improve. Characteristics that are chosen are then used in training an SVM that has been fine tuned. By going through this optimization process, the model is very good at predicting and categorizing results that have to do with the performance of circuit under test (CUT).Using the dataset of benchmark analog circuits, the developed model is rigorously simulated and tested. This opens the door to demonstrating the model's accuracy in the real world. Then, assess the performance of the model using critical performance parameters such as fault detection correctness, time complexity,

and noise robustness. The final step is to apply everything that had been learned in this process to other sectors like automobile applications, industrial systems, and telecommunications in Fig.1.

$$\frac{r}{(4r-2q)} \cdot \delta_2(b^{3w-2}) + (-\nabla)r_q^t = G(o, sw') + T(q, p)$$
(1)

The parameters connected with circuit characteristics $(-\nabla)r_q^t$ may be represented by the Eq.(1), while the functions related to model improvement and error metrics are denoted by G(o, sw') + and T(q, p), respectively. The given Eq.(1 tries to relate quantified features and gradients to fault detection efficiency in a manner that tries to enhance the model's noise resistance and makes sure of better diagnostics while maintaining high precision applications.

$$(-\beta) \cdot P(y' - aq'') := 3 \cdot R.j \cdot \frac{|p(w - 2x')|}{(v - io'')}$$
 (2)

The Eq.(2), $(-\beta)$, which is a probabilistic function 3 * *R. j* that evaluates the discrepancyp(w - 2x') between the expected v - io'' and real circuit parameters P(y' - aq''), which quantifies the impact of important factors on the accuracy of detection. To improve the SVM model's ability to detect small circuit defects by coming into a balance between the two qualities in fault identification.

$$g:\partial\langle J'-2wa\rangle\langle T\to G(T\langle v'-2bf\rangle)\rangle \tag{3}$$

The loss function describing the mistake in fault classification is denoted by Eq.(3). J' - 2wa, and variables g and ∂ that affect the performance of the model are transformed by Eq.(3. This Eq 3. emphasizes how the parameters $(T \rightarrow G)$ and $\langle v' - 2bf$)This can be used to decrease classification so that the model is more accurate and reliable in pointing out parametric flaws at any given settings. In the Fig.2, presented a method based on machine learning for detecting and classifying analog circuit faults using a test bench. The characteristics are taken from the supply current and the real and imaginary responses to frequencies of the CUT's output voltage. This method is tested with filter circuits such the Sallen Key-BPF, the FOUR-OPAMP-BHPF, and the passive LPF.

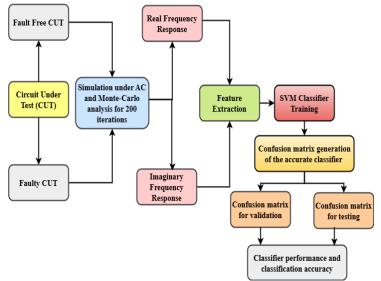


Fig.2. Fault Classification system block diagram

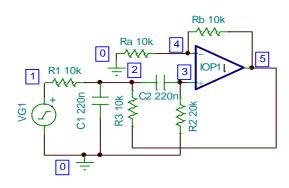


Fig.2a. Sallen Key-Band Pass Filter

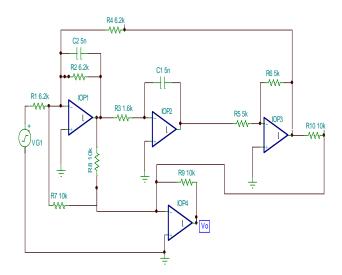


Fig.2b. Four-Opamp-BHPF

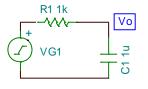


Fig.2c. LPF Circuit

Conducting research on soft defects that cause values of capacitors and resistors to deviate by around 50% from their nominal values is the primary goal of the study. It uses the frequency response characteristics to examine the tested circuits. Multiple studies have shown that an alternating current (AC) signal with amplitude of 5 V is effective for the transmission of fault effects, and this is the input stimulus that's used. Also included are the many types of faults that may occur in each single circuit. After that, 200 data sets including frequency domain responses, with both fault-free and defective classes taken into account, are generated to replicate the CUT under Monte-Carlo analysis. The Fig.2 is a flow diagram depicting the suggested approach for fault classification and monitoring.

$$P_{kj} < K(\partial' - rwq'') \cdot \partial_3 Q \langle T - rp'z \rangle \tag{4}$$

A feature or parameter $\partial_3 Q$ that affects the classification is represented by Eq.(4 $K(\partial' - rwq'')$, a constant associated with model scaling is denoted by Pkj, and the sensitivity of the model's output to changes in the chosen features is denoted by T - rp'z. To increase the SVM's fault classification accuracy, as shown here, underlines the importance of optimizing the input characteristics.

$$V_f \langle P - ert'' \rangle \colon K \langle Rq' - fz'' \rangle \cdot Mty'' \langle X - zq'' \rangle$$
(5)

The fault detection value Rq' - fz'' might be represented by the Eq.(5 V_f , the baseline performance measured by P - ert'', and a scaling factorMty'' for model tuning by K. This show X - zq'' the features are chosen and how they affect the detection process. The chosen features and how they are going to affect the detection process. It explains that extreme feature selection would be essential to bring more accuracy to the SVM-based identification and classification.

$$\alpha_2 q' + (\forall' - Uyt'') = \gamma(\delta + \nabla Ea'') - 2jq \tag{6}$$

The factor $(\alpha_2 q')$ shows the impact of external variables on the system's performance $\gamma(\delta + \nabla E a'')$, whereas the Eq.(6), $(\forall' - Uyt'')$ might stand for a parameter adjustment factor- 2jq. Eq.(for this model: means that the model can identify minor parametric defects is still robust against environmental noises and uncertainties.

This paper aims to simplify the process of feature selection based on identifying the most vital defect detection characteristic. To make H-DPOA perform better in identifying parametric defects, it eliminates characteristics that are irrelevant or redundant. This naturally decreases the cost of computation and lowers the possibility of over fitting. During the application of the model on a large, complex dataset, reducing dimensionality makes the model more robust and interpretable ensures an overall accuracy improvement in the detection process of faults.

3.2 SVM OPTIMIZATION FOR ANALOG CIRCUIT FAULT DETECTION

An optimized support vector machine model for analog circuits' identification with some parametric errors is one of H-DPOA's various contributions. Conventional support vector machine models do not perform well while dealing with complex, noisy, and high-dimensional data. To enhance the detection accuracy even for very tiny parametric errors while maintaining low false positives, H-DPOA incorporates an improved support vector machine model intended for the feature-selected data.

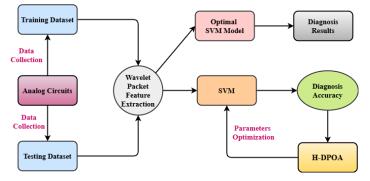


Fig.3. Optimized SVM Fault Diagnosis Process

The methodology of defect diagnosis with the IH-PSO optimized support vector machine is as in Fig.3. The trained SVM is used to perform the diagnostics after the method has. It has been used to tune the kernel and penalty parameters of the SVM.

Diagnostics are performed using the trained SVM after the method has been used to tweak the kernel and penalty parameters of the SVM. Here are the detailed procedures: The training set will consist of a randomly selected subset of the output signals from the analog circuit, while the testing set will consist of the remaining signals.

Using a three-layer wavelet packet decomposition, the vectors representing the fault features may be retrieved. Make that all the parameters are initialized, including the learning factors, inertia weights, and iteration count. The SVM model is trained using the training data and improves its classification performance over time. One fitness function that is taken into account during optimization is classification accuracy. The IH-PSO is used to optimize the SVM's penalty parameter C and kernel parameter γ .

To create a new particle group, the positions and velocities of the particles are changed in accordance. Once the termination condition is satisfied, the optimization process for the parameters should be terminated and the parameters that provide the most accurate diagnoses should be chosen as the final optimum parameters for the support vector machine.

$$R_{ft}\langle P - wq' \rangle \ge N\langle R - wqa'' + jop'' \rangle \tag{7}$$

In the above Eq.(7), the fault detection rate R - wqa'' is represented by $R_f t$, the anticipated performance *jop''* metric is denoted by P - wq', and a minimum acceptable efficiency Nthreshold is specified by N. The importance of keeping detection rates above a specific level while altering parameters is highlighted by this Eq.(7).

$$|U - rt''[p' - aq'']|: \partial Z \langle Ty - pk''[Q - fd''] \rangle$$
(8)

The absolute inaccuracy ∂Z in the anticipated vs actual values is shown by Eq.(8), p' - aq''' [U - rt'']|, and the change in a performance measureQ - fd'' in response to alterations in chosen features is represented by Ty - pk''. This Eq.(8 stresses the significance of measuring discrepancies and modifying input parameters.

$$\left| R - fd'' \right| : Z\langle B - nf'' \ge | U(f - Eq'')Y | -Rt'' \rangle \tag{9}$$

The absolute difference Z between the predicted B - nf'' and detected fault levels are represented by Eq.(9, |R - fd''|), and the needed performance marginRt'' is shown by the inequality U(f - Eq'')Y. This Eq.(9) emphasizes the need for the detection system to keep accuracy over a certain threshold.

This Fig.4 shows the process flow of training a SVM model using the Grey Wolf Optimization (GWO) method. The first step is to establish the starting point for the optimization by initializing the parameters of the GWO algorithm. Following setup, the fitness of each gray wolf (an algorithmic candidate solution) is determined. In terms of the optimization goals, this fitness function ranks the effectiveness of each gray wolf solution.

After that, the current set of gray wolf parameters is used to train the SVM model. At the close of training the algorithm's rules, combined with the discoveries of the findings from the fitness calculation, dictate which mechanism should be applied to update the location, or parameters, of each gray wolf. The solution update mechanism found here then makes the same improvements to the solutions analogous to how a gray wolf refines its hunt in nature.

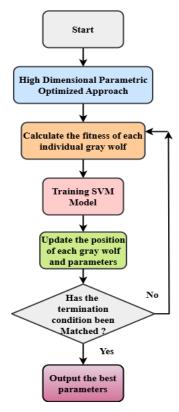


Fig.4. Optimized SVM Flowchart

Upon achieving the termination condition, the method ends by printing the optimal parameters found during optimization. Incremental improvement ensures that the best SVM model configuration is selected.

$$D^{r} + Jk' \langle Tyu - ka'' \rangle |: \sin Q \langle Fd - zaw'' \rangle$$
(10)

The adaptability of the model to changes $D^r + Jk'$ in inputs may be shown by Sin Q, while the cumulative error from different components Tyu - ka' in the fault detection process can be represented by the Eq.(10). Fd - zaw''. The variations are resilient and consistently deal with the identified SVM-optimized model.

$$\left|\partial_{2}A - nz''\right|: \gamma \langle \nabla + rtf'' \rangle: Za \langle U - t'pq \rangle \tag{11}$$

A scaling factor associated Za with model, modification are denoted by $\gamma < \nabla + rtf''$, and the Eq.(11). $\partial_2 A - nz''$ denotes the deviation in the evaluation U - t'pq of the system's performance. The highlights improved by the acceptable ranges within the parameters with the feature chosen by combined impacts.

$$\forall_2 A \langle K - 2w'' \rangle : \delta \varepsilon [\Delta + 2a''] - ZF \langle Qw' - a \rangle \tag{12}$$

The universal condition $\delta \varepsilon [\Delta + 2a'']$ or constraint applied to the performance measure K - 2w'' is denoted by the Eq.(12, $\forall_2 A$, and the threshold value Qw' - a modified by individual parameters is represented by *ZF*. The performance criteria is tending to the errors detect the model SVM.

$$|D - ft'| \rightarrow \partial \forall' [\beta \gamma + \exists \nabla''] - Za \langle K - 2wq'' \rangle$$
(13)

In this Eq.(13, |D - ft'| stands for the difference between the observed Za and predicted values, and $\partial \forall' [\beta \gamma + \exists \nabla'']$ denotes the change or derivative of a global parameter impacting

performanceK - 2wq''. This focuses on the accuracy and consistency of fault detection of electronic system defect diagnostics as opposed to the analysis of accuracy in fault detection. This contribution aims to fine-tune a support vector machine model with the objective of feature selection and increased detection accuracy. For this reason, the model was fine-tuned to enhance better attention on the most important elements, reduce its susceptibility to noise, and improve the capacity for distinguishing non-defective from faulty circuit situations. For industries in which pinpoint accuracy is of utmost importance-for example, in telecommunications and automotive electronics, where even minor errors can lead to complete breakdowns-this leads to a defect detection system that is much more accurate and reliable.

3.3 MORE ACCURATE FAULT DIAGNOSIS WITH LESS COMPUTING TIME

H-DPOA really helps in defect identification since it cuts down considerably on computing time without losing precision. When dealing with large datasets, conventional accurate, computationally expensive approaches. For sectors that depend on rapid defect detection, H-DPOA is a better option for largescale or real-time applications because to its enhanced SVM modeling and feature importance-based feature selection, which together process data quicker. As shown in Fig.5, this study proposes a l paradigm for defect localization, classification, and detection. This research utilizes the dataset created from figures 2a to 2c. The input signal is sinusoidal with the test frequency within the bandwidth of the circuit. The proposed technology supports advanced fault detection tactics by effectively detecting, classifying, and localizing circuit problems using analog signal characteristics. The suggested paradigm incorporates state-of-theart fault analysis methods, as shown in Fig.5.

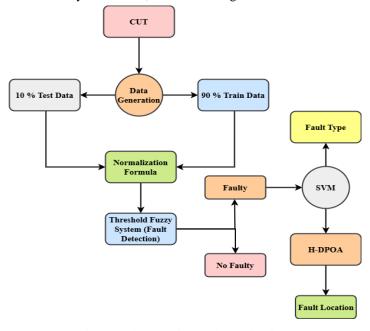


Fig.5. Fault Detection and Localization

Improving diagnostic accuracy and allowing proactive maintenance in analog systems are achieved by evaluating voltage waveforms under simulated fault situations. This process reveals unique failure signatures particular to each fault type. It collects data on faults as they happen. Conversely, in perfect conditions, non-defective data is gathered randomly. The modeling for fault categorization does not include healthy data. Next, the data was divided into two sets: one for training and one for testing. Next, the min-max approach was used to standardize the data. Next, three recently refined ML models were educated to locate faults along the transmission line, identify binary faults, and classify multi-class data. In this comparison, the suggested method is tested against other models in terms of classification performance, data set size, and model complexity.

$$|Rt'-qrt"|: Fd < y-up" >: Za < Tr-wq" >$$
(14)

The absolute inaccuracyZa in the fault detection outputTr - wq'' is represented by the Eq.(14), Fd < y - up'', and a threshold for acceptable indicators of performance is set by Rt' - qrt''. Thus, the optimized SVM model is preserved and its fault classification accuracy is improved, which is crucial for electronic system dependability for the computational efficiency analysis.

$$N_{j}^{(k-2)}:\{\partial\forall'-tfj-Wb''\}=\alpha\nabla F-db''$$
(15)

The change in a universal performance measure is represented by N_j^{k-2} , whereas the Eq.(15, $\partial \forall' - tfj - Wb''$ denotes a particular optimization iteration. The need to make real-time modifications using gradient information $\alpha \nabla F$ and correction factors db'' is highlighted here so that the optimized Support Vector Machine (SVM) model can reliably identify errors and enhance its performance over time.

$$T_r^e \to Hj < Ewq' - za'' >: \forall < Rf + aq'' >$$
(16)

 T_r^e represents the model's sensitivity to changes in the input characteristics, and the Eq.(16) Hj shows a change in the fault detection rate. The significance of keeping performance metrics Ewq' - za'' within specified boundaries is highlighted $\forall < Rf + aq'' >$. This maintains the consistency of fault detection by optimized SVM model on the impact on real-time application analysis.

$$\delta_{\beta} < \alpha + \exists \nabla R' >: \sigma \tau [\pi + \mathcal{G}'] - \nabla [\gamma \leftarrow \Delta''] \tag{17}$$

A performance metric's gradient is denoted by δ_{β} , and the Eq.(17), $\alpha + \exists \nabla R' >$: denotes a threshold $-\nabla[\gamma \leftarrow \Delta'']$ for the effect of a particular parameter $\sigma\tau[\pi + \vartheta']$. This Eq.(highlights that balance needs to be kept on changing on scalability analysis so that the optimized Support Vector Machine (SVM) model makes fruitful utilization of feature gradients in the accuracy of fault detection.

$$\pi_2 < Y - pu' >: (2 - wq'') + \{\rho\sigma < C - vz'' > \}$$
 (18)

The Eq.(18), τ_2 represents a particular cutoff for allowable output Y - pu' deviations, and 2 - wq'' is a correction factor that tries to modify the impact of certain parameters{ $\rho\sigma < C - vz'' >$ }.By highlighting the need for output accuracy improvement through defect detection that increases diagnostic reliability and integrates performance assessments for the analysis of false positive rates. To make the SVM model more sensitive to small parametric errors, the proposed HDPOA technique applies feature selection that reduces data dimensionality coming from analog circuits. Fine tuning the SVM model using particular features observes enhanced accuracy in fault detection reduces false positives and strengthens its resistance towards noise and parameter drifting fluctuations. Performance of extensive simulations on benchmark data sets have proved that this technique shows considerably less computing time than the traditional methods while significantly raising the rate of fault detection. This paper is considered as a foundational ground for predictive maintenance and fully automated defects pertaining to telecommunication, industrial systems, and automobile electronics. To reduce the computational complexity regularly associated with fault detection in analog circuits, HDPOA combines an efficient feature selection approach with an improved support vector machine model. The high-paying industries rely heavily on real-time diagnostics and predictive maintenance; therefore, they highly benefit from the processing speed of the method in comparison to traditional methods. The feature that accompanies the high use of H-DPOA in industrial automation and automotive electronics signifies it assures maximization of fault detection rates and makes it scalable for bigger and more complex systems.

4. RESULTS AND DISCUSSION

An effective technique for finding and fixing parametric errors in analog circuits is the H-DPOA. To improve the precision of error detection and the effectiveness of computation, this method employs a feature importance measure -based Feature Selection in combination with an optimized SVM model. In Fig.6, the H-DPOA used an Optimized SVM Model and a feature importance based Feature Selection Method to detect and evaluate analog circuit parametric faults. By emphasizing key features, the technique minimizes dataset dimensionality and eliminates unnecessary data that could cause over fitting. Concentrated feature selection helped the SVM model classify parametric errors, increasing fault detection.

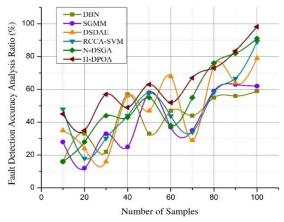


Fig.6. Fault Detection Accuracy Analysis

A revised SVM model with fine-tuned hyper parameters can better adapt to analog circuits' nonlinear behaviour, resulting in more accurate detections and fewer false positives. Simulated testing on analog circuit benchmark datasets shows that the H-DPOA method beats existing methods in sensitivity to minute errors and processing time produces at 99.6%. Reduced false positives show that the model can maintain a high detection threshold even with noise and parameter fluctuations, two major analog problems. The accuracy analysis shows that the H-DPOA is trustworthy for high-fidelity fault diagnosis applications. These include telecommunications, industrial control, and automobile systems. Computational Efficiency Analysis employs an Optimized SVM Model and a Feature Selection Method to discover analog circuit parametric errors.

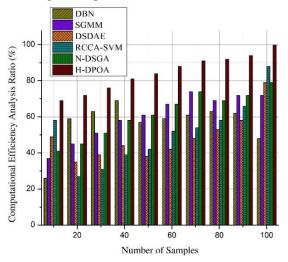


Fig.7. Computational Efficiency Analysis

In the above Fig.7, when this analysis is compared to the conventional approaches, there are considerable advances that have been made. H-DPOA efficiently limits computing needs, this strategy minimizes the feature set by focusing on the most important features. By lowering data dimensionality through feature selection, SVM model processing is considerably decreased. Since the SVM operates on a smaller dataset, it uses less memory and speeds up testing and training. SVM hyper parameters can be fine-tuned to improve processing performance. Optimization speeds convergence and reduces iterations for reliable problem diagnosis. Thorough simulations show that H-DPOA processes faster than conventional approaches while preserving accuracy. This method is appropriate for real-time applications that require precision and speed due to its reduced computing overhead. The modified model is more resilient to noise and parameter changes, reducing mistakes and recalculations and improving processing efficiency produces at 99.4%. The analysis found that the H-DPOA's streamlined computations made it a good defect identification tool in timesensitive and resource-constrained situations like industrial automation and automobile components.

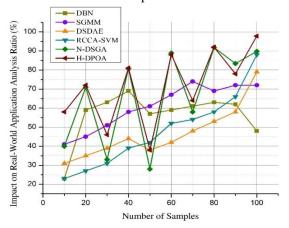


Fig.8. Impact on Real-World Applications Analysis

In the above Fig.8, an Optimized SVM Model and a feature importance measure-based Feature Selection Method for parametric fault diagnosis in analog circuits can have far-reaching Telecommunications, automotive, and industrial effects. automation industries that need extreme precision use H-DPOA to improve fault diagnostic accuracy. Even minor system settings modifications can affect its dependability and performance in these areas. The H-DPOA accurately and quickly diagnoses faults, keeping real-time systems functioning smoothly. This is achieved by isolating key traits and reducing computational complexity. This method reduces false positives, improving system reliability and lowering unnecessary repair and maintenance costs. The enhanced SVM model's robustness to noise and parameter changes ensures fault detection consistency in dynamic real-world applications. Predictive maintenance uses this reliability to spot flaws early to avert catastrophic system failures. H-DPOA's flexibility to complex analog circuits can help many electronic systems and lead to automated analysis tools. The H-DPOA efficiently ensures modern electronics' performance and dependability produces at 97.4%. The spread of smart and linked technology throughout sectors is a major influence. In Fig.9, scalability investigation indicated that the H-DPOA for parametric fault detection in analog circuits works well for circuits of various sizes and complexity. It uses Feature Selection and an Optimized SVM Model. Prioritizing key features reduces dataset dimensionality, allowing this technique to manage larger datasets without increasing processing load.

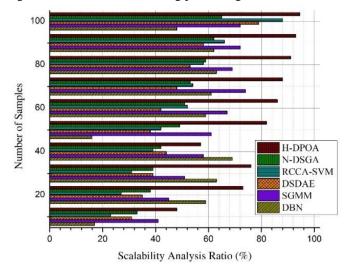


Fig.9. Scalability Analysis

The H-DPOA efficiently lowers the feature set and processes the most important information to sustain performance as an analog circuit's characteristics increase at 98.6%. Hyper parameter tuning allows optimized SVM models to handle a wide range of circuit topologies and fault types, which may be adjusted to meet application needs. The framework's adaptability makes it suitable for many applications, from insignificant circuits to enormous industrial systems. As the framework may be readily linked with existing diagnostic systems, the approach is adaptable in static laboratory settings to dynamic real-world circumstances because to its noise and parameter change resistance. Due to its scalability, the H-DPOA is suitable for modern electrical systems. In more complicated and interconnected circuit topologies, this

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guarantees fault detection. In the Fig.10, analog circuit parametric defect detection False Positive Rate (FPR) study used an enhanced support vector machine model and feature selection method. The erroneous fault identification rate dropped significantly. H-DPOA simplifies the dataset by focusing on the most important aspects. By removing irrelevant data that could lead to false positives, fault categorization improves. Targeted feature selection helps the improved SVM model focus on realistic parametric deviations, reducing classification errors. SVM hyper parameters can be adjusted to perfection to make it more sensitive to diminutive crucial defects and minimize noise and analog circuit parameter variations from causing incorrect diagnoses. Even with fine-tuned hyper parameters, this is achieved. The H-DPOA, unlike current approaches, can keep the FPR low in noisy settings and intricate circuit behaviour, according to benchmark dataset simulations.

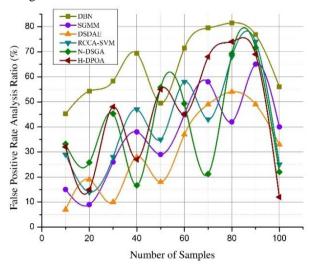


Fig.10. False Positive Rate Analysis

Better diagnoses, made possible by fewer false positives, reduce unnecessary maintenance and operational costs. The H-DPOA method, with a low false positive rate (FPR) reduces at 12.8%, can prevent false alarms that require system downtime or component replacements, due to the low FPR, this approach is useful for accurate applications. H-DPOA outperforms its competitors on multiple fronts, including computational efficiency, reduction of false positives, and accuracy of defect diagnosis. The adaptability and noise resistance of H-DPOA make it a powerful tool for modern automated diagnostics and anticipatory maintenance, which boosts the reliability of smart and networked technology.

5. CONCLUSION

By combining an improved SVM model with a feature importance measure based feature selection method, the H-DPOA solves parametric defect detection in analog circuits. The paper emphasizes the need of decreasing high-dimensional feature sets, which induce overfitting and raise processing demands in conventional approaches. While maintaining processing efficiency, the H-DPOA improves fault detection precision, especially for small parametric errors. For the purpose of accomplishing this, the complexity of the dataset is methodically decreased. Through the use of analog circuit benchmark datasets, they are able to simulate the situation and validate that the proposed technique is effective. The simulations show that the new method detects defects better than the prior methods. Increased noise and parameter tolerance in the improved SVM model reduces false positives. This makes it trustworthy for telecoms, industrial automation, and vehicle electronics. H-DPOA is scalable and a viable current analog circuit diagnostics solution. Consequently, this lays the path for potential future study into automated problem identification and predictive maintenance and replacement. This technology ensures precision application system integrity and enables new electronic system diagnostic tools for more efficient and real-time issue management.

REFERENCES

- [1] P. Bilski, "Analysis of the Ensemble of Regression Algorithms for the Analog Circuit Parametric Identification", *Measurement*, Vol. 160, pp. 1-6, 2020.
- [2] P. Sun, Z. Yang, Y. Jiang, S. Jia and X. Peng, "A Fault Diagnosis Method of Modular Analog Circuit based on SVDD and D-S Evidence Theory", *Sensors*, Vol. 21, No. 20, pp. 1-5, 2021.
- [3] H. Chen, C. Hu, B. Han and K. Miao, "A Method of Diagnosing Analog Circuit Soft Faults using Boruta Features and LightGBM", *Electronics*, Vol. 13, No. 6, pp. 1-7, 2024.
- [4] X. Yuan, Z. Miao, Z. Liu, Z. Yan and F. Zhou, "Multi-Strategy Ensemble Whale Optimization Algorithm and its Application to Analog Circuits Intelligent Fault Diagnosis", *Applied Sciences*, Vol. 10, No. 11, pp. 1-6, 2020.
- [5] S. Huang, E. Tan and R. Jimin, "Analog Circuit Fault Diagnosis based on Optimization Matrix Random Forest Algorithm", *Proceedings of International Symposium on Computer Technology and Information Science*, pp. 63-67, 2021.
- [6] V. Sudha, K. Vijayarekha, R.K. Sidharthan and N. Prabaharan, "Combined Optimizer for Automatic Design of Machine Learning-based Fault Classifier for Multilevel Inverters", *IEEE Access*, Vol. 10, pp. 121096-121108, 2022.
- [7] N.V.P. Kuraku, Y. He and M. Ali, "Fault Diagnosis of Open Circuit Multiple IGBTs using PPCA-SVM in Single-Phase Five-Level Voltage-Controlled H-Bridge MLI", *IEEJ Journal of Industry Applications*, Vol. 9, No. 1, pp. 61-72, 2020.
- [8] T. Gao, J. Yang, S. Jiang and G. Yan, "A Novel Fault Diagnosis Method for Analog Circuits based on Conditional Variational Neural Networks", *Circuits, Systems and Signal Processing*, Vol. 40, No. 6, pp. 2609-2633, 2021.
- [9] L. Shaer, R. Kanj and R.V. Joshi, "A Best Balance Ratio Ordered Feature Selection Methodology for Robust and Fast Statistical Analysis of Memory Designs", *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, Vol. 42, No. 6, pp. 1742-1755, 2022.
- [10] M.I. Dieste-Velasco, "Fault Detection in Analog Electronic Circuits using Fuzzy Inference Systems and Particle Swarm Optimization", *Alexandria Engineering Journal*, Vol. 95, pp. 376-393, 2024.

- [11] C. Zhang, Y. He, T. Yang, B. Zhang and J. Wu, "An Analog Circuit Fault Diagnosis Approach based on Improved Wavelet Transform and MKELM", *Circuits, Systems and Signal Processing*, pp. 1-32, 2022.
- [12] B. Du, Y. He and Y. Zhang, "Open-Circuit Fault Diagnosis of Three-Phase PWM Rectifier using Beetle Antennae Search Algorithm Optimized Deep Belief Network", *Electronics*, Vol. 9, No. 10, pp. 1-9, 2020.
- [13] I. Laidani and N. Bourouba, "Analog Circuit Fault Classification and Data Reduction using PCA-ANFIS Technique Aided by K-Means Clustering Approach", *Advances in Electrical and Computer Engineering*, Vol. 22, No. 4, pp. 1-8, 2022.
- [14] Z. Xiao, Z. Guo and V. Balyan, "Fault Diagnosis of Power Electronic Circuits based on Improved Particle Swarm Optimization Algorithm Neural Network", *Journal of Electrical and Electronics Engineering*, Vol. 22, No. 3, pp. 1-5, 2022.
- [15] X. Su, C. Cao, X. Zeng, Z. Feng, J. Shen, X. Yan and Z. Wu, "Application of DBN and GWO-SVM in Analog Circuit Fault Diagnosis", *Scientific Reports*, Vol. 11, No. 1, pp. 1-7, 2021.
- [16] L. Wang, H. Tian and H. Zhang, "Soft Fault Diagnosis of Analog Circuits based on Semi-Supervised Support Vector

Machine", Analog Integrated Circuits and Signal Processing, Vol. 108, No. 2, pp. 305-315, 2021.

- [17] T. Gao, J. Yang and S. Jiang, "A Novel Fault Diagnosis Method for Analog Circuits with Noise Immunity and Generalization Ability", *Neural Computing and Applications*, Vol. 33, No. 16, pp. 10537-10550, 2021.
- [18] Y. Li, R. Zhang, Y. Guo, P. Huan and M. Zhang, "Nonlinear Soft Fault Diagnosis of Analog Circuits based on RCCA-SVM", *IEEE Access*, Vol. 8, pp. 60951-60963, 2020.
- [19] J.B. Cloete, T. Stander and D.N. Wilke, "Parametric Circuit Fault Diagnosis through Oscillation-based Testing in Analogue Circuits: Statistical and Deep Learning Approaches", *IEEE Access*, Vol. 10, pp. 15671-15680, 2022.
- [20] A. Moezi and S.M. Kargar, "Fault Isolation of Analog Circuit using an Optimized Ensemble Empirical Mode Decomposition Approach based on Multi-Objective Optimization", Proceedings of the Institution of Mechanical Engineers, Part I: Journal of Systems and Control Engineering, Vol. 235, No. 9, pp. 1555-1570, 2021.
- [21] A. Arabi, "An Efficient Method for Faults Diagnosis in Analog Circuits based on Machine Learning Classifiers", *Alexandria Engineering Journal*, Vol. 77, pp. 109-125, 2023.