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IMPLEMENTATION OF SEGMENTED CURRENT STEERING DIGITAL TO ANALOG CONVERTER USING MEMORY LESS PIPELINE DYNAMIC DESIGN TECHNIQUE

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Abstract

In the era of 5g technology, it is needed to improve speed of the circuitry used in analog and digital hardware. Digital to analog conversion is an essential process, DAC is a vital circuitry utilized for the same in the electronic systems. Our proposed current-steering DAC (CS-DAC) offers suitability for both high speed and high-resolution requirements. This work claims memory less dynamic pipeline design technique and implementation of CS-DAC using pipeline technique. CS-DAC with and without memory-less dynamic pipeline design technique is implemented using 180nm Berkeley Short-Channel IGFET Model (BSIM) version 3.3 model file. The simulation results of CS-DAC with and without pipeline design technique also compared as well.

Keywords:

Digital to Analog Converter (DAC), Current-Steering DAC (CS-DAC), System on Chip (SOC), Differential Non-Linearity (DNL), Integral Non-Linearity (INL), Spurious-Free Dynamic Range (SFDR) and Signal-to-Noise and Distortion Ratio (SNDR)

1. INTRODUCTION

In the era of 5G, high speed demands of data need to improve speed of the electronics hardware and hence circuitry used in it. Analog and digital circuitry has to improve its performance as far as speed as concern. Performance of the high-speed Data processing unit like microcontroller and microprocessor is restricted by the convertor circuitry like DAC and ADC. Hence it is equally concerned to improved speed of DAC and ADC

The need for DAC interfaces for System on Chip (SOC) applications has grown as communication technology has advanced. With so many different options for technology and architecture, CMOS Current Steering (CS) architectures are ideally suited for these kinds of applications because of their low power consumption and inherent speed.

CS-DACs architecture contain array of matched current sources. A proportionate quantity of current flows to the differential output resistive load based on the applied input digital code. A CS architecture may be unary, binary, or segmented, depending on how the current source array is organized. Every architecture has its own benefits and drawbacks. Unary DAC contains binary to thermometer converter and current sources of equal values. Although it produces a linear result, it has high area requirements. However, in contrast, Binary DAC which contains currents sources of binary weightage values and provide output current based on binary input. It requires less space but has poor linearity. The third one, the segmented architecture utilise advantages of both the architecture and suitable for high-speed, high-resolution applications. To obtain the best features from both architectures, the segmented DAC trades off between the unary and binary DACs. A balanced performance measure like static and dynamic performances have been found also It gives reasonable decoder power, area and complexity.

Static and Dynamic errors measure performance of the Converters. Mismatch of the components, output impedance and noise lead to static error. Differential and Integral nonlinearities, (DNL and INL) measures static performance of the converters. These measurements are not specifically employed for DAC characterisation in high-speed applications. Rather, because dynamic error rise with increasing sample rates and signal frequencies, they take on greater significance. These errors include settling errors, glitches, etc. [1-3]

The effect of errors can be easily measures in frequency domain analysis. The frequency domain measures are Spurious-Free Dynamic Range (SFDR) and Signal-to-Noise and Distortion Ratio (SNDR). [7]

Following is the framework for the remaining portion of the paper. Section 2 provides brief of segmented CS-DAC architecture. Section 3 provides memoryless pipeline dynamic circuit design technique and its pros and cons. Section 4 proposed architecture of DAC and simulation results of segmented 8-bit CS-DAC and proposed architecture. Section 5 gives final conclusion and future scope of the work.

2. SEGMENTED CS-DIGITAL TO ANALOG CONVERTER ARCHITECTURE

Different topologies used to construct DACs. Numerous factors, such as INL and DNL, monotonicity, chip area (relative to die size), settling time, and matching requirements, demonstrate the benefits and drawbacks of each topology. In this section segmented CS-DAC architecture is discussed.

Mainly DAC architecture classifies based on current scaling, voltage scaling, and charge scaling and current steering architecture. In a Current, voltage and charge scaling DAC, a current, voltage or charge scaled and added based on the given digital input. R-2R ladder binary weighted DAC and Binary weighted DAC are the example of current scaling DAC. A large value spread of resistors in binary weighted DAC least attractive choice for DAC. Also, all other architecture suffers from low monotonicity.

Current steering DACs indeed gained popularity as a prevailing architecture for D/A conversion since the late 1980s.This is because the current steering architecture can deliver significant currents (10-20mA) to a 50Ω load without the need for buffering. Unlike resistor-string and switched-capacitor D/A converters, which are governed by the gain bandwidth product (GBW) of the buffer circuitry, a current-steering converter's operating speed is determined by its ability to drive the gates of the switches. Therefore, it is possible to achieve sample rates of

several hundred million samples per second. This establishes the current-steering D/A converter as the most fitting architecture for digital IF transmitters and direct digital synthesizers. Moreover, only transistors are utilized to deliver the output current, permitting the utilization of the standard CMOS process, whereas resistor-string or switched-capacitor converters mandate high-accuracy resistors and capacitors. The current steering DAC comes in three versions: (1) Binary, (2) Unary, and (3) Segmented [4-6].

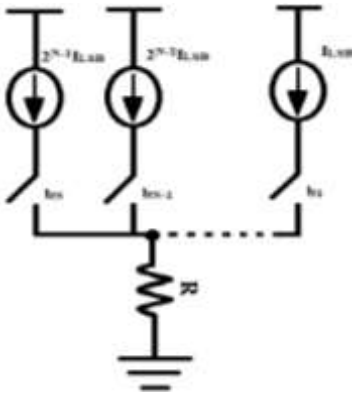

Fig.1. Current steering DAC using binary weightage sources

In the binary weighted CS-DAC, the current sources with binary weight are switched to output according to binary input data as shown in Fig.1. In the unit-element version (unary), 2^n number of equal value's current sources is needed. One current source is turn on as input increase by 1 LSB. As it is required 2^n current sources which consume much larger area, although it does have higher monotonicity. Binary weighted DAC, can suffer from higher glitch as input changes from mid-code. There are multiple switches can be turn ON or OFF as input changes in either direction from mid code. For example, when there is binary 011 to 100 transitions, which translate to decimal 3 to 4 transitions, the output may vary by significantly more than 1 LSB, possibly leading to a significant glitch. Therefore, in situations where monotonicity is a crucial criterion, a binary array is not a smart solution.

Uniformity is another advantage of unary architecture over binary weightage architecture. Equal value current sources in the unary architecture yields a DNL of less than 0.5 LSB even if there is a mismatch of 50% in current sources. In binary-weighted architecture, the intensity of the uniformity is depended on the weight of the bit.

Unary architecture is using Thermometer code. Advantage of thermometer code is that glitches does not lead to irregularities. The magnitude of glitch in thermometer coded Unary architecture DAC correlates with the quantity of switches that activate during a specific sampling instance. The glitch increases with increasing step size and decreases with decreasing step size. However, the amount of the glitch is exactly proportional to the amplitude of step since the number of switches that change is proportional to the size of the signal step. Thus, the glitch does not impact on any nonlinearity in the DAC analog output. [10,11]

From above discussion it is sure that unary architecture has several advantages over binary-weighted architecture although, it does have major drawback of huge amount of area consumption. The unary architecture required 2^N number array of current source for N bit resolution DAC. Therefore, a Segmented architecture which is the hybrid of binary-weighted architecture and unary architecture is preferred for high resolution, good linearity and monotonicity application. [10,11]

2.1 SEGMENTED DAC ARCHITECTURE

Segmented architecture is hybrid of binary architecture and unary architecture. Thermometer-coded unary architecture indeed exhibits significantly better Differential Non-Linearity (DNL), ensuring higher accuracy in DAC. On the other hand, binary-weighted converters are known for their ability to utilize less area. To take advantage of this, MSBs are designed by thermometer coding and LSBs are designed by binary weighted coding. In this paper an 8-bit segmented DAC is implemented, where the 6 Most Significant Bits (MSBs) is implemented using unit element sources, while the 2 Least Significant Bits (LSBs) is implemented using the binary-weighted current sources. [9,12]

To transform the array into a rectangular shape (rather than a lengthy, one-dimensional 64 current sources), one raw and one column 3 to 8 binary to thermometer decoders are employed, resulting in a matrix of current sources. Output from current sources is fed to node Iop from array as well as from binary weightage current sources. Output current can be converter to voltage by using trans-impedance amplifier.

The natural query that emerges is the extent of segmentation for the converter (i.e., the allocation of bits to be represented by a unit-element array versus binary-weighted elements). As shown in Fig.2 [10] diverse percentage of segmentation vs area requirement is plotted. In this figure, full binary DAC corresponds to 0% segmentation and Full unary DAC corresponds to 100% segmentation. The analog space needed for an optimal Differential Nonlinearity (DNL) range from 4096 times Aunit for binary architecture to Aunit for the unary architecture DAC. The analog space needed for an optimum Integral Non-Linearity (INL) less than or equal to 0.5 LSB is 1024 times Aunit. The digital space varies from 2n*Ad to Ad for n bits in the thermometer segment.

Assuming that Aunit and Ad are roughly identical, the entire region results in a graph where the digital area dominates for thermometer DACs, the analog area for optimal INL dominates for mild segmentation, and the analog area for ideal DNL dominates for binary DACs.As shown in Fig.2, the ideal segmentation point is chosen so that the analog region and the digital region are equal in order to improve static performance without unduly increasing the area. As the number of bits in the unary section increases, the dynamic performance decreases. Additionally, extra bits in the thermometer segment led to a larger digital area, increased output capacitance, and heightened design complexity.

These factors consequently result in increased timing inaccuracies, synchronization and matching issues, and greater charge feed through. Furthermore, a higher decoder complexity increases critical path delay, which lowers DAC's operating speed. Better performances can only be achieved from higher segmentation if timing precision is ensured. Using additional thermometer bits also results in a decrease in the DAC's conductance at low frequencies. [9,12]

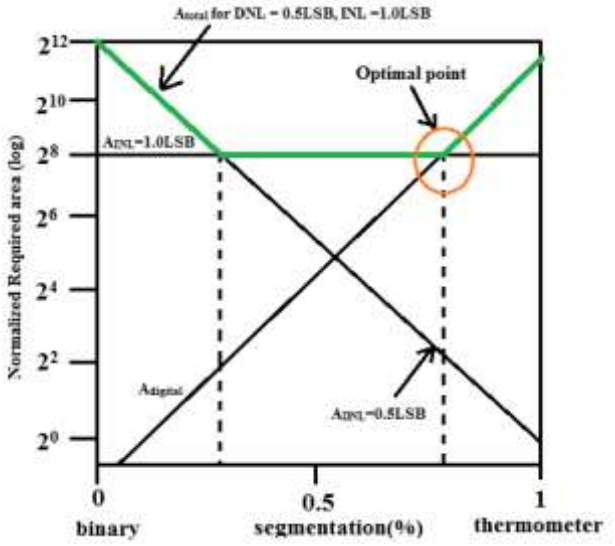

Fig.2. Normalized required area verses % of segmentation [10]

3. MEMORY LESS PIPELINE DESIGN TECHNIQUE

3.1 PIPELINE DYNAMIC CIRCUIT

Pipeline dynamic structure is shown in Fig.3 [13]. In a pipeline dynamic design technique, every gate level (pipeline stage) undergoes the consecutive phases of precharge, evaluate, and memory sequentially as shown in Fig.4 [13]. Precharge step prior to evaluation phase at each gate level guarantees logic high at the dynamic gate's output before evaluation phase commences [8]. Memory phase follows evaluation phase and guarantees that the values computed during evaluation phase are held for a designated period [8, 13] The correlation between the operational stages within a particular pipeline level and those of the preceding and succeeding levels is illustrated in Table.1, as exemplified.

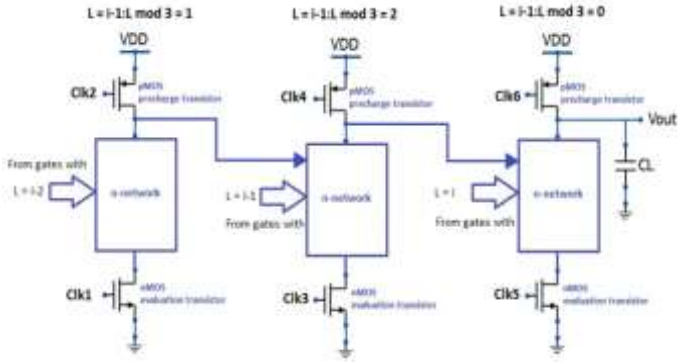

Fig.3. Pipeline structure [13]

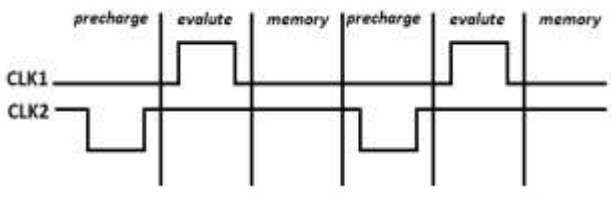

Fig.4. Clock signal 's waveform [13]

Table.1. The pipeline phases [13]

	Gate level		
Cycle	**Level 1**	**Level 2**	**Level 3**
1		-	-
2	Evaluation1		-
3	Memory1	Evaluation1	
4		Memory1	Evaluation1
5	Evaluation2		Memory1
6	Memory2	Evaluation2	
7		Memory2	Evaluation2
8	Evaluation3		Memory2
9	Memory3	Evaluation3	
10	-	Memory3	Evaluation3
11	-	-	Memory3

The Table.1 shows 3 level of design and 3 input data sets. Cycle is defined by phase time duration in the pipeline operation. With this configuration, it is assured that while evaluating in a stage, the antecedent stage is in memory phase. It guarantees that throughout evaluation phase gate's inputs remain steady as they represent outputs from the preceding level in the memory phase. Furthermore, while a level L_i is in the precharge or evaluation stages (where outputs can change), the pipeline's next level L_{i+1} is in memory or precharge phases respectively, where there are no limitations on the input's condition (whether stable or not). The arrangement outlined above also assures the appropriate operation of pipeline architecture. The pipeline's evaluated output at level L_i at the n^{th} clock cycle remains same for the duration of the [n+1] clock cycle (level L_i stays in memory phase) and it is used as input at for the next level gate L_{i+1} during [n+1] clock cycle. To accomplish the pipeline operation, appropriate clocks are required at each gate level. Three clock along with their complements are utilized as illustrated in Fig.3.

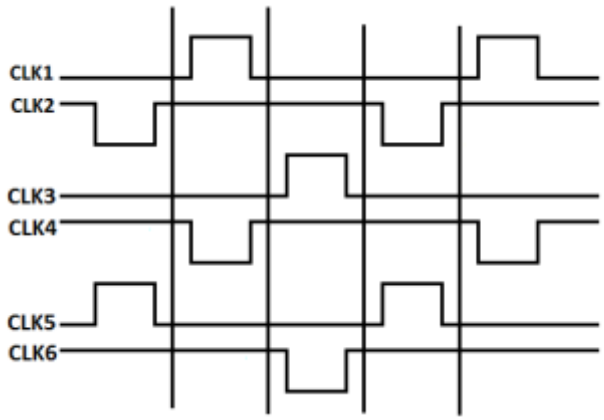

Fig.5. Three phases clocking scheme [13]

The clock1, clock3 and clock5 along with its complement clock2, clock4 and clock6 respectively and its distribution at different level of gate is outlined in Table.2. Two clock signals at level L_{i+1} are postponed by a third of the clock period of level L_i, or, in other words, a phase time. The setup of the pipeline design with suitable clock signals for individual gates, in accordance with their level in the design, is showcased in Fig.5.

Table.2. Clock signal to the gate at different level [13]

Level	Evaluation (NMOS) transistor	Precharge (PMOS) transistor
Level 1	CLK1	CLK2
Level 2	CLK3	CLK4
Level 0	CLK5	CLK6

3.2 PROS AND CONS

Compared to conventional domino logic, pipeline dynamic design technique can implement both noninverting and inverting gates and that without memory components. [8]

A drawback of the suggested method is the requirement for additional clock signals. However, regardless of circuit complexity, there is a one-time cost associated with creating these clock signals.

Furthermore, in pipeline architecture where each level is provided with a different clock, the distribution of the clock is not challenging or costly design problem. Especially in well-organized circuits like ALU ones, this expense is rather minimal. Lastly, clock skew problems can be addressed by applying well-known skew protected dynamic design techniques.

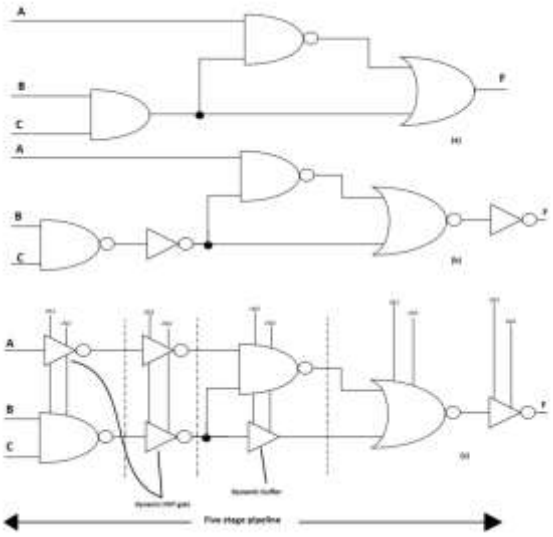

Fig.6. (a) Gate level circuit, (b) CMOS level circuit. (c) Memory-less pipeline dynamic circuit [13]

Each of the pipeline design contains a characteristic that level L_{i+1} inputs are level L_i outputs; to hold output of level L_i cascaded memory elements are inserted between level L_{i+1} and L_i. total number of memory elements are equal to number of intermediary levels. This raises a circuit design's hardware cost. However, the aforesaid restriction can be readily and affordably met with the help of the design technique mentioned above. In this design method it is needed to add even number of inverter or even number of inverter and one buffer to do synchronisation for each level as shown in the Fig.5. if an output of level L_i gate is connected to a level L_{i+k} gate, then k number of intermediate level is needed. If a k is even number then add even number of dynamic inverter and if it is odd then add (k-1) even number of dynamic inverter and one dynamic buffer to unaltered the functionality of the circuit. An example of the above design approach is shown in Fig.5 [8,13].

4. PROPOSED ARCHITECTURE AND SIMULATION RESULTS

8-bit Current steering DAC with segmentation of 2bit binary architecture and 6-bit unary architecture is implemented as shown in Fig.6. To convert linear one dimensional 64 current sources in to two-dimensional array of current source 6 bit is divided in to 3*3. Two 3 bits binary to 8-bit thermometer decoder is implemented using memory less pipeline dynamic circuit design technique. Proposed Segmented current steering memory less pipeline dynamic design architecture is shown in Fig.6.

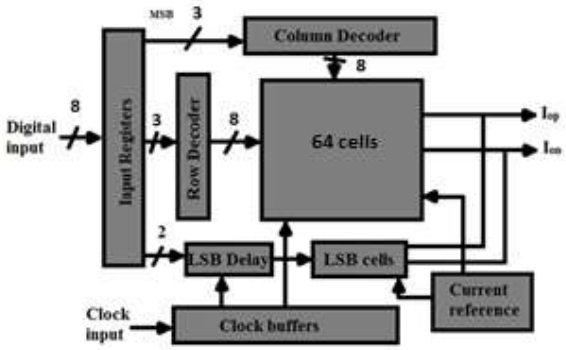

Fig.7. Segmented architecture of CS-DAC [3]

4.1 SIMULATION RESULTS OF SEGMENTED 8-BIT CS-DAC

The segmented 8-bit CS-DAC is implemented using 180nm Berkeley Short-Channel IGFET Model (BSIM) version 3.3 in NG-SPICE tool. The DAC is simulated at 2V power supply. The maximum output current provided is 20mA for the 50Ω load resister, to get maximum analog output voltage of 1V with respect to ground. The simulated double ended ramp output is show in Fig.8(a) and its partial part is sown in Fig.8(b). Simulated sine wave output is shown in Fig.9. The simulated DNL, INL and SFDR of this DAC are within ±0.18LSB, ±0.08LSB and 45.74dB respectively as shown in Fig.10-Fig.12.

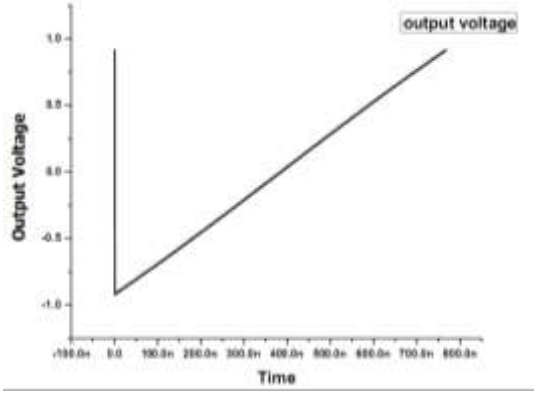

Fig.8. (a) simulated ramp output voltage

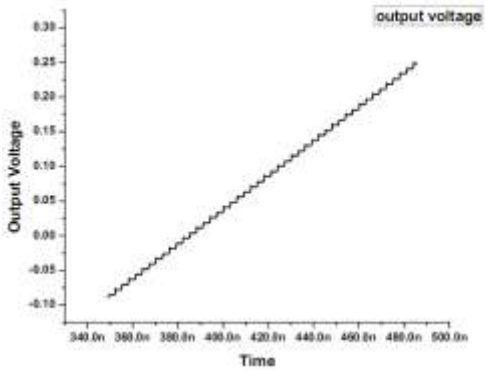

Fig.8. (b) Simulated partial output voltage

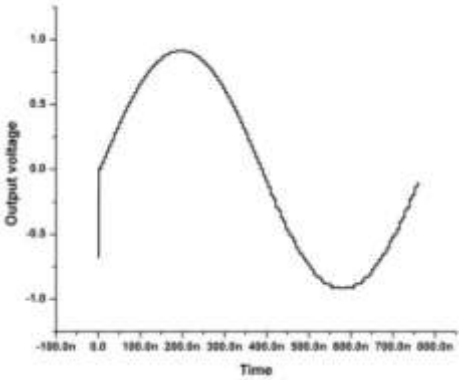

Fig.10. Simulated Sine wave output voltage

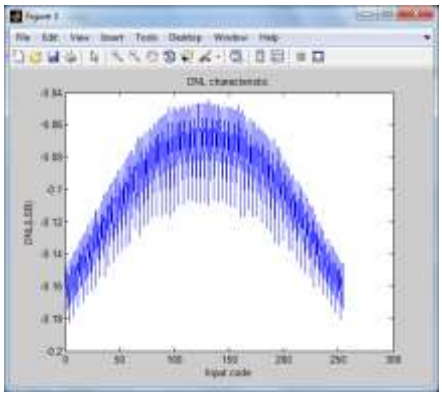

Fig.11. DNL characteristic

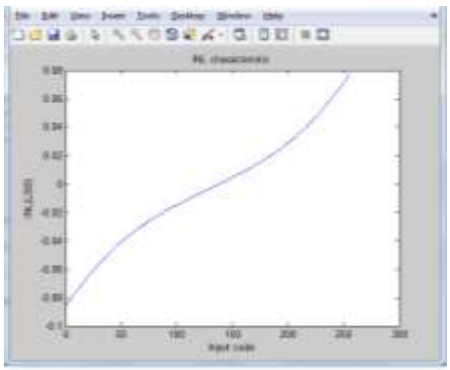

Fig.12. INL characteristic

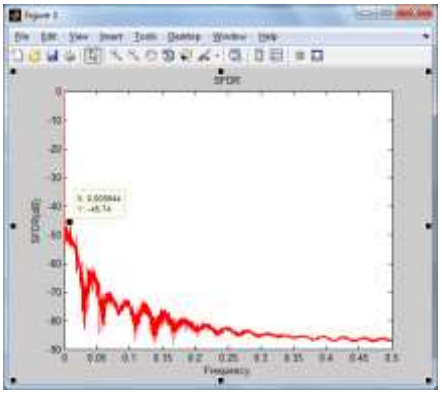

Fig.13. Output Spectrum of the DAC

4.2 SIMULATION RESULTS OF PROPOSED ARCHITECTURE

The segmented 8-bit CS-DAC using pipeline dynamic technique is implemented using 180nm BSIM version 3.3 model file in NG-SPICE tool. The DAC is simulated at 2V power supply. The simulated double ended ramp output is shown in Fig.14(a) and its partial part is shown in Fig.14(b). Simulated sine wave output is shown in Fig.15. Simulated DNL, INL and SFDR are within ±0.18LSB, ±0.08LSB and 42.39dB respectively as shown in Fig.16-Fig.18.

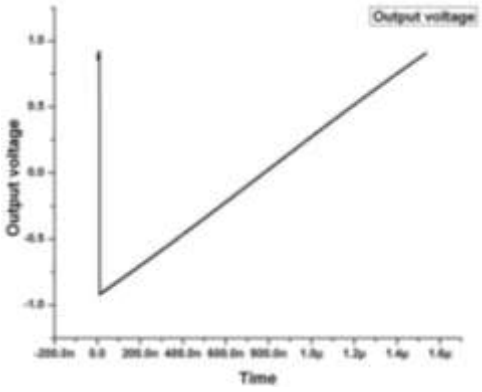

Fig.14. (a) Simulated ramp output voltage

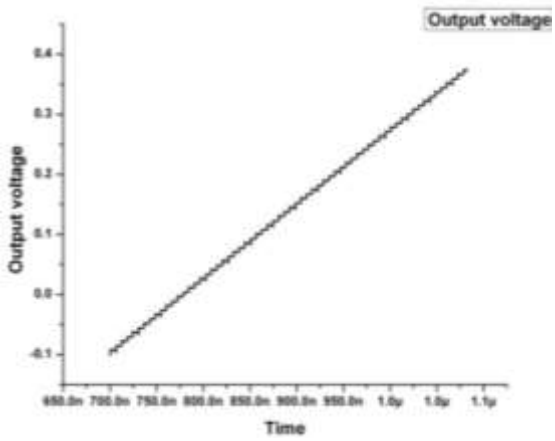

Fig.14. (b) Simulated partial output voltage

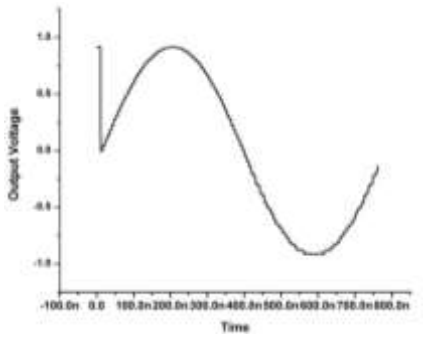

Fig.15. Simulated Sine wave output voltage

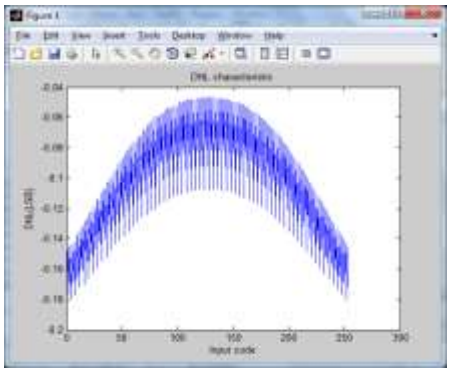

Fig.16. Differential nonlinearity characteristic

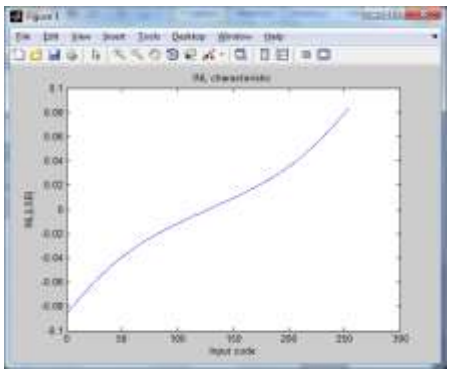

Fig.17. Integral nonlinearity characteristic

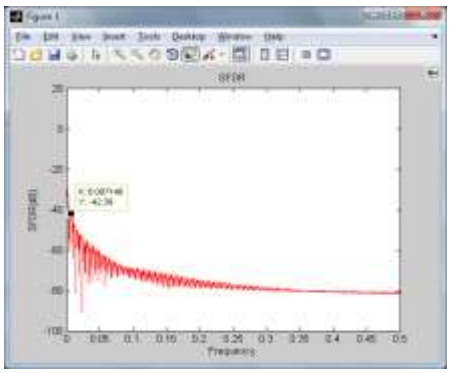

Fig.18. Output Spectrum of the Pipeline DAC

4.3 COMPARISON SUMMARY

The simulated comparison of segmented 8-bit CS-DAC and proposed architecture are summarized in the Table.3.

Table.3. Simulated performance of DACs

	Segmented 8bit CS-DAC	**Proposed DAC**
Resolution	8-bit	8-bit
DNL	±0.18LSB	±0.18LSB
INL	±0.085LSB	±0.085LSB
Voltage	2V	2V
SFDR	45.74dB	42.39dB
Sampling frequency	1.21 GSPS	2.78 GSPS
Power consumption	19.3mW	39.7mW
No of transistor	1766	1912
Latency	1	5
Process	180nm	180nm

5. CONCLUSION AND FUTURE SCOPE

In this paper memory-less dynamic design pipeline technique has been elaborate. Using the foundations of pipeline design without the use of memory elements is known as a memory-less dynamic pipeline design technique. Because there is no memory element involved, the memory-less dynamic pipeline design technique operates more quickly than the standard pipeline technique. It is discovered that the memory-less dynamic pipeline design technique can be used to implement any combinational circuit. A memory-less dynamic pipeline design technique has routing and clock screw issues because of different non-overlapping clocking techniques.

8-bit segmented CS-DAC with and without memory-less pipeline concept. The segmented DACs have been implemented in 180 nm CMOS technology. The simulation result of segmented 8bit CS-DAC shows a maximum DNL of 0.18 LSB and an INL of 0.085 LSB. The simulated SFDR is 45.74 dB. Sampling frequency of the DAC is observed 1.21 GSPS. Total power consumption is 19.3mW. The simulation result of proposed DAC shows a maximum DNL of 0.18 LSB and an INL of 0.085.

LSB. The simulated SFDR is 42.39 dB. Sampling frequency is observed 2.78 GSPS. Total power consumption is 39.7mW. Sampling frequency of pipeline CS-DAC is improved 2.3 times than the sampling frequency of CS-DAC. While power consumption is approximately 2 times more in pipeline CS-DAC than CS-DAC. It is concluded that the pipeline CS-DAC can be used in the high-speed demand system like wireless telecommunication application, video application, RADAR, etc. In future enhancement, power consumption in pipeline CS-DAC is approximately 2 times more than the CS-DAC. Low power circuit design technique can be useful for reduce power consumption of CS-DAC.

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