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A LOW POWER AND AREA REDUCTION MULTIPLIER IMPLEMENTATION USING VEDIC MATHEMATICS IN 16NM FINFET TECHNOLOGY

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Abstract

Signal processing application circuits are being used in various instruments and devices. The implementation of these algorithms is done in various devices. For ASICs CMOS were used for several decades, but these devices suffer from second order effects which will affect the overall system performance. To overcome this, the paper presents the design and implementation of a 4 bit Vedic multiplier using 16nm FinFET technology which removes the issues with second order effects. By integrating Gate Diffusion Input (GDI) logic, the proposed method significantly reduces transistor count while enhancing speed and power efficiency. The results demonstrate that the Vedic multiplier achieves superior performance, making it well-suited for high-speed digital signal processing applications.

Keywords:

CMOS, FinFET, DSP, Vedic, Multiplier, Adder, Low Power

1. INTRODUCTION

In Earlier stages, multiplication processes are carried out in different manner. But these methods have many complex operations in programming it to software or code in micro-code of a machine. The Design structure should have to concentrate on parameters such as cost, Resource allocation and area consumption. Digital signal processing algorithms are more dependent on their multipliers because of their faster computational results.

The Vedic Mathematics sutras are the most popular methodology. It has 16 Sutras (or aphorisms) to deal various fields in science and other related fields. The Efficiency of a multiplier can be raised with FinFET technology along with Vedic multiplier. The FinFET devices are selected over traditional MOSFETs due to various advantages of FinFET over CMOS. If computational power increases it leads computational density to higher range. By using FinFET the number of transistors used, and the area required for each transistor is reduced. To achieve maximum computational power, it is necessary to concentrate on transistor size. When the dimension of the transistor is reduced, the proximity between the drain and the source reduces and it results in the gate electrode capability to control the current in the channel regions. This causes large, short-channel effects in MOSFET. Gate length (Lg) shrink plays a vital role in designing efficient multipliers. The gate length below 90nm results in leakage current and 28nm results in excessive leakage leading to worthless transistor. Hence it is important to scale the gate length to suppress the off-state leakage. The computational power can also be increased by choosing suitable materials during the manufacturing of chips. But this point doesn't seem to be economical. In short, a FinFET device establishes a greater short-channel behavior at minimum switching times. Also, it has maximum current density over MOSFET devices.

In earlier stages, multiplication processes were carried out using conventional arithmetic methods like shift-and-add algorithms or Booth's algorithms. However, these methods involve several complex operations, which result in challenges when programming them in software or micro-coding in hardware. As digital signal processing (DSP) applications require high-speed and efficient multipliers, significant attention is given to optimizing multiplication techniques. Critical design parameters such as cost, resource allocation, and area consumption must be considered when developing such circuits.

Vedic Mathematics, particularly its sutras, provides an efficient alternative to traditional multiplication methods, improving computational speed and reducing complexity. The application of Vedic multiplication algorithms in hardware implementation, such as multipliers, offers advantages in reducing computational overhead. Among different technologies, FinFET has emerged as a preferred choice over CMOS for modern ASIC designs due to its ability to suppress short-channel effects and enhance performance. FinFET transistors offer higher current density, reduced leakage, and lower area consumption, making them ideal for high-performance DSP applications like Vedic multipliers.

2. LITERATURE SURVEY

M. Shoba et al. [1] had used CslA and Binary to Excess 1 Converter (BEC) for minimizing the computation delay of hierarchy multiplier. The Vedic multiplier encloses a reduced area and operates with minimum delay. This Experiment has been done with Gate Diffusion Input (GDI) logic and simulated in Cadence SPICE simulator. P. Gulati et al. [2] designed a Vedic multiplier using adaptable Manchester Carry Chain adders (MCC) in a hierarchical manner. This Experiment was performed using 45nm CMOS technology and simulated in Cadence SPICE simulator. Deergha et al. [3] presented a Vedic real multiplier in reference to Urdhva Tiryakbhyam. This Experiment can be utilized for four and three Vedic real multipliers. This Experiment has been simulated with Xilinx ISE 13.4 and Modelsim 5.6 tool. Sayali Shembalkar et al. [4] implemented a Vedic multiplier based on Vedic Mathematics Sutra for real time applications. The Vedic Multiplier provides efficient parameters such as maximum speed, minimum area and lower delay of multiplier. Korra Ravi Kumar et al. [5] designed a 2T XOR gate based full adder with GDI technique. The 2T XOR gate design utilizes 180nm technology. This Experiment has been simulated using LT spice, Xilinx 14.7 ISE, Basys3 Artix7 device. Nehru Kandasamy et al. [6] investigated performance measures of gate diffusion input technique (GDI) on self-check, carry select adder encloses a self-resetting logic (SRL) GDI technique and carry look-ahead adder (CLA) for various word lengths. This Investigations analysis of CSA and CLA has been designed with 180nm technology and

simulated with Cadence tool. D. K. Kahar et al. [7] revised Vedic multiplication algorithm by utilizing Vedic mathematics sutras based on Urdhava Tiryakbhyam. The Vedic multiplication algorithm has a larger speed computation within minimum combinational path delay than other existing multipliers with other algorithms. S. Akhter et al. [8] developed a new binary multiplier by applying Vedic mathematics. The Simulation waveforms have been carried out for 4-bit multiplication process. This Method requires larger bit size but has provided maximum speed in computation. P.A.I. Khan et al. [9] had used Vedic multiplier for rapid Multiplication. The Vedic Multiplier provides maximum speed and minimum power consumption and delay. This Multiplier utilizes technique known as GDI (Gate Diffusion Input) for obtaining efficient results.M. Bansal et al. [10] presented Vedic multiplier circuit with the GDI technique. The Experiment on Vedic multiplier circuit has used 18 nm FinFET technology. The Simulation of this experiment has been done on Cadence Virtuoso tool. A. S. Thakur et al. [11] implemented a FIR filter architecture out of complex Vedic multiplier. It uses common Boolean logic (CBL) and simulated with Xilinx device. P. Saritha et al. [12] developed Vedic multiplier with GDI logic. By GDI logic transistor count of the circuits can be minimized. The circuit of Vedic multiplier is made up of AND gate, half adder, Full adder and 4-bit Ripple carry circuits based GDI logic. M. Yuvaraj et al. [13] implemented a "Sampoornam" alias "Absolute Vedic" multiplier. The Vedic multipliers are also used for modeling a 4-bit Multiplier accumulator unit (MAC) unit and it can be expanded up to 64-bit using Vedic scaling technique. The 4-bit MAC unit had efficient results such as 25 % compression in time delay. A. Jain et al. [14] designed an improved algorithm for multiplication by the combination of Vedic mathematics and Booth-Wallace tree multiplier. This Improved multiplier has been implemented with 8×8 multiplier with VHDL coding support. This Experiment has been simulated with ModelSim and Xilinx ISE 14.1. A. Eshack et al. [15] constrained a Pipeline approach based minimum power systems with higher speed. The Algorithm of this system has been designed with Verilog Hardware Description Language. This Algorithm was constructed on spartan 3E series of Field Programmable Gate Array (FPGA). A. Jain et al. [16] simulated 16-bit multiplier with Vedic multiplication technique. The simulation of this design is carried out with Verilog HDL and Synthesized on Xilinx ISE 14.2i on xc3s500e-5pq208 device. Chandrashekara et al. [17] designed an 8-bit Vedic multiplier. A Modified Carry Save Adder (MCSA) was additionally used for this purpose. The coding for 8-bit Vedic multiplier has been done with VHDL. This Experiment has been stimulated with XILINX 14.7 software and verified with Spartan-6 FPGA. The Simulation result described that 8-bit Vedic multiplier has been used 14.219ns time for multiplication. Akhter et al. [18] coined a Vedic mathematics-based multiplier. This Vedic multiplier design has been designed with various standard cell libraries at 32/28 nm. The Simulation result shows that the 64-bit VM with SQRT-CSA adder was 5% rapid when compared to RCA-CSA and BEC. G. V. Nikhil et al. [19] constrained a barrel shifter and Vedic multiplier with kogge-stone adder for low power applications by reversible logic gates. The Reversible Vedic Multiplier uses 0.621 % minimum power and reversible Barrel Shifter utilized 26.49 %. Lad et al. [20] investigated and compared Vedic mathematics sixteen sutras for obtaining faster processing blocks required for various real time applications. All sixteen sutras of Vedic mathematics are analyzed in 16 sutras of Vedic mathematics and was simulated in Vivado 2017.1 tool.

Traditional multiplication techniques using CMOS technology face significant challenges as transistor sizes shrink below 90nm. As the gate length decreases, short-channel effects become prominent, leading to increased leakage currents and reduced gate control. This results in degraded performance and power inefficiencies, particularly for complex arithmetic operations like multiplication. Furthermore, the high transistor counts in conventional multipliers, such as those designed using CMOS technology, increase power consumption and area, limiting scalability and computational efficiency. The use of FinFET technology helps mitigate these issues. FinFET devices offer better electrostatic control over the channel, minimizing leakage current and improving switching speed. However, existing methods using FinFET technology often do not fully leverage the advantages of advanced logic design techniques such as Gate Diffusion Input (GDI). GDI logic reduces the number of transistors required for operations like AND, XOR, and adders, further enhancing the efficiency of the multiplier. By integrating GDI logic with FinFET technology, it is possible to design high-performance, low-power multipliers for DSP applications.

3. BACKGROUND METHODOLOGY

3.1 VEDIC MULTIPLIER

The building blocks of most of the digital systems are multipliers. So there are many investigations carrying on for designing a high speed multiplier. It is found that Vedic multiplier is one of the efficient types of high speed multiplication. In this paper the design of Vedic multiplier is implemented. The implementation of Vedic multiplier can be done using three algorithms. Of the existing design of the Vedic multiplier only one is used in all applications and the rest two will be used in some special operations. Urdhva Triyabhyam is the algorithm of Vedic multiplier. It is the basic formula used for multiplication and it works vertically and crosswise in a process.

Vedic multiplier uses the principle of Vertically and Crosswise and finally adding the obtained results together. This operation of Vedic multiplier can be well understood by considering the following example in Fig.1. The multiplication of two 2-digit numbers 46 and 33 using Vedic multiplier is done as given in Fig.1.

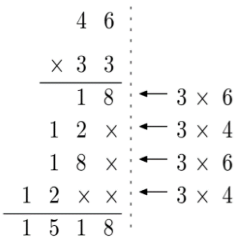


Fig.1. Operation of Vedic multiplier

In a similar way to the above example shown in Fig.1, the binary multiplication can be carried out as shown in Fig.2.

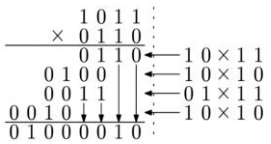


Fig.2. Binary multiplication using Vedic multiplier

In view of existing high-speed multipliers, Vedic multiplier is one of the fastest multiplier since it employs minimum hardware and delay. The 2-bit Vedic multiplier is composed of two half adder blocks and four AND gates and it is shown in Fig.3.

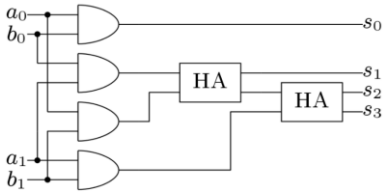


Fig.3. Block diagram of 2-bit Vedic multiplier

The 4-bit Vedic multiplier can be designed using four 2-bit Vedic multipliers and it is shown in Fig.4. In this implementation three adder blocks are used. The adder block may be a high-speed adder like CLA, or CSA or conditional adders. The concatenation block is denoted in circles.

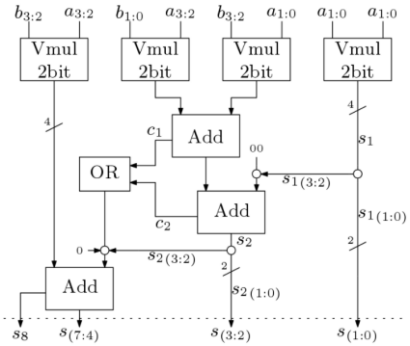


Fig.4. (a) Block diagram of 4-bit Vedic multiplier using 2-bit Vedic Multiplier.

Like this 4-bit Vedic multiplier can be designed with AND gate, Full adder and Half adder in a more simplier way compared to the one in Fig.4.

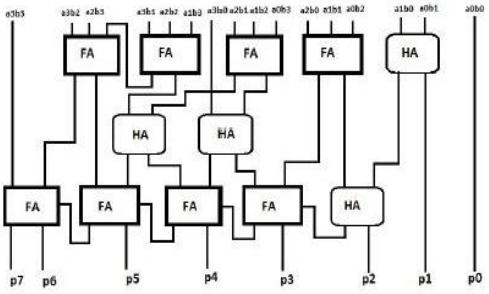


Fig.4. (b) Block diagram of 4-bit Vedic multiplier using AND gate, Full adder and Half adder

It can be seen from Fig.4(a) and Fig.4(b) that the design using AND gate, Full adder and Half adder will be simpler. Our proposed method employs the design algorithm of Fig.4(b) to make it more efficient and simpler by minimizing the components and delay of the circuit.

3.2 FINFET

FinFET is a multi-gate MOSFET device. It is developed at the University of Berkley, California by Chenming Hu and his colleagues. Multi-gate devices are one that consists of more than one gate within the single device. The body of the FinFET is made of a thin silicon film. FinFET gets its name as its structure looks like a set of fins. It can deal effectively with sub-threshold leakage, poor short-channel electrostatic behavior, and high device parameter variability that plagued planar CMOS as it scaled down to 20 nm. Also, its greater advantage is that it can operate at a considerably lower supply voltage by allowing voltage scaling. It also deals greatly with static and dynamic power leakages and saves power. This device is the most favorable technology for making Moore's law possible.

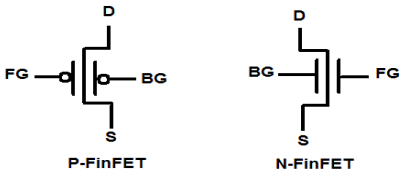
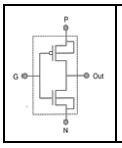


Fig.5. FinFET structure

With the view of numerous advantages in terms of performance, intra-die variability, power leakages, low voltage operation and mainly its lower retention voltage for SRAMs FinFETs are used in place of planar CMOS as the device of choice.

3.3 GDI LOGIC

The GDI is a simple cell as given in Fig.6(a). It can implement complex functions in a simpler way with the use of two transistors. The design of various functions using GDI is given in Fig.6(b). The implementation of GDI will thus give rise to a fast, low power circuit since it uses a very less number of transistors when compared to CMOS and PTL methods.



N	P	G	Out	Function
'0'	B	A	$\overline{A}B$	F1
B	'1'	A	$\overline{A}+B$	F2
'1'	B	A	$A+B$	OR
B	'0'	A	AB	AND
C	B	A	$\overline{A}B+AC$	MUX
'0'	'1'	A	$\overline{A}$	NOT

	CMOS	GDI
AND	6	2
OR	6	2
XOR	12	4

Fig.6. (a) GDI logic, (b) Logic diagram of GDI, Fig.6(c) Transistor utilization in CMOS and GDI logic

The proposed method utilizes a combination of GDI logic and 16nm FinFET technology to design a highly efficient 4-bit Vedic multiplier. GDI logic simplifies the implementation of digital circuits by using fewer transistors to achieve the same functionality as conventional CMOS designs. This approach not only reduces the overall transistor count but also enhances

switching speeds and minimizes power consumption. FinFET technology further optimizes the design by addressing the shortcomings of traditional MOSFETs, such as short-channel effects and leakage currents, which become significant at smaller dimensions. By employing FinFETs, the proposed method ensures better electrostatic control over the channel, enabling the use of lower supply voltages while maintaining high performance. The synergy between GDI logic and FinFET technology results in a compact and power-efficient design for the Vedic multiplier, significantly improving computational efficiency and making it suitable for high-speed digital signal processing applications. This combination allows for more effective resource utilization, ultimately leading to advancements in the performance of integrated circuits.

4. IMPLEMENTATION AND RESULTS

The implementation of 4-bit Vedic multiplier is done using LTspiceXVIII by use of 16nm FinFET technology with GDI logic. The results and the observations of the various gates are given below.

4.1 AND GATE

The two input AND gate are designed and simulated with the use of 2 FinFET transistors instead of 4 transistors in CMOS implementation.

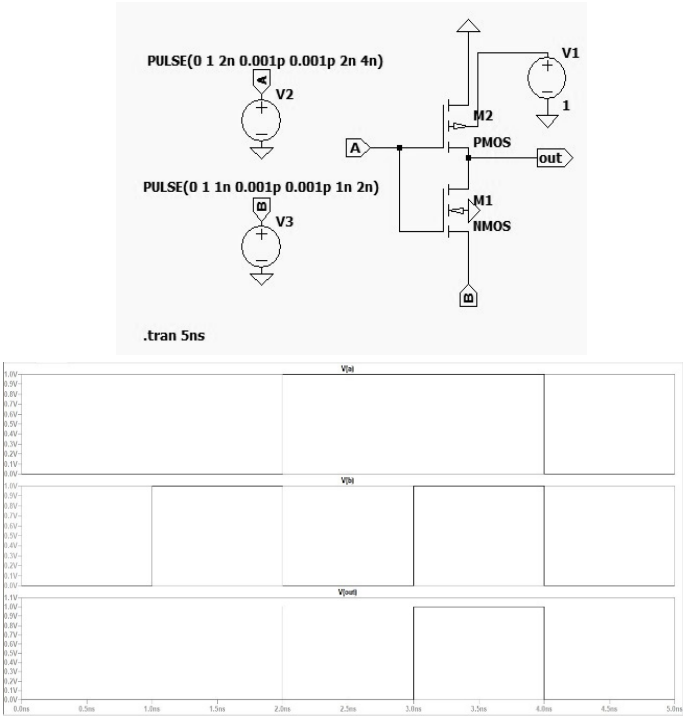


Fig.7. (a) AND gate schematic and (b) AND gate waveform

4.2 XOR GATE

The two input XOR gates are designed and simulated with the use of 4 FinFET transistors instead of 12 transistors in CMOS implementation.

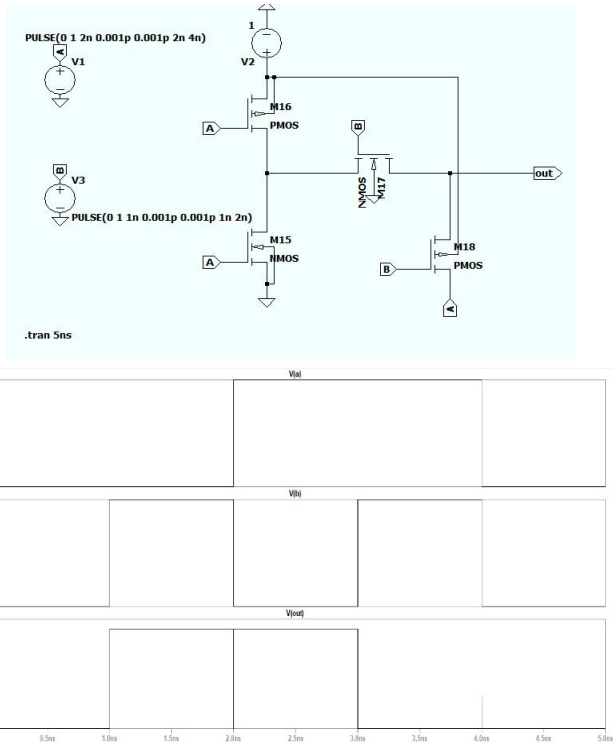


Fig.8. (a) XOR gate schematic and (b) XOR gate waveform

4.3 HALF ADDER

The two input Half adder is designed and simulated with the use of 6 FinFET transistors instead of 18 transistors in CMOS implementation.

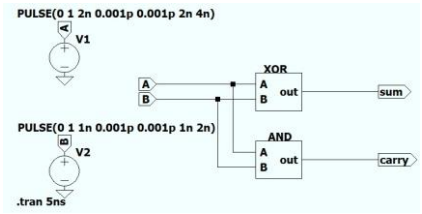


Fig.9. (a) Half adder schematic and (b) Half adder waveform

4.4 FULL ADDER

The three input Full adders are designed and simulated with the use of 10 FinFET transistors instead of 28 transistors in CMOS implementation.

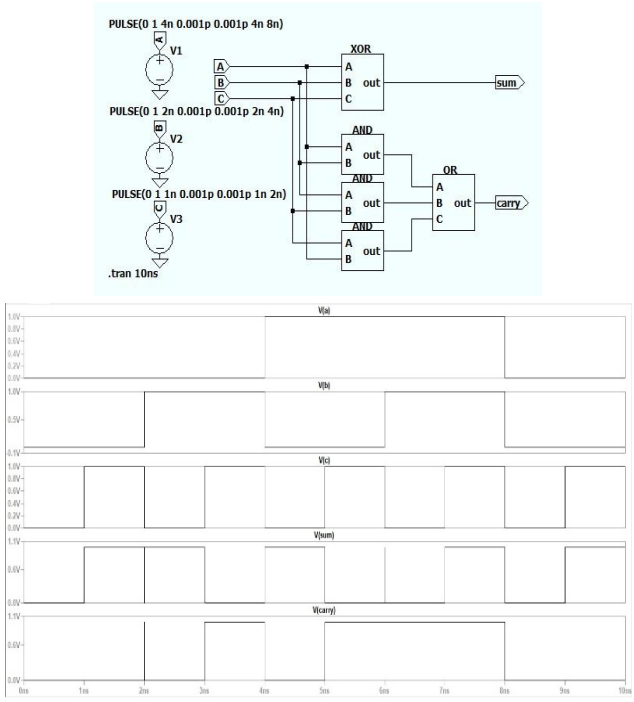


Fig.10. (a) Full adder schematic and (b) Full adder waveform

4.5 RCA

The four bit RCA is designed and simulated with the use of four GDI full adders and it requires only 40 FinFET transistors instead of 92 transistors in CMOS implementation.

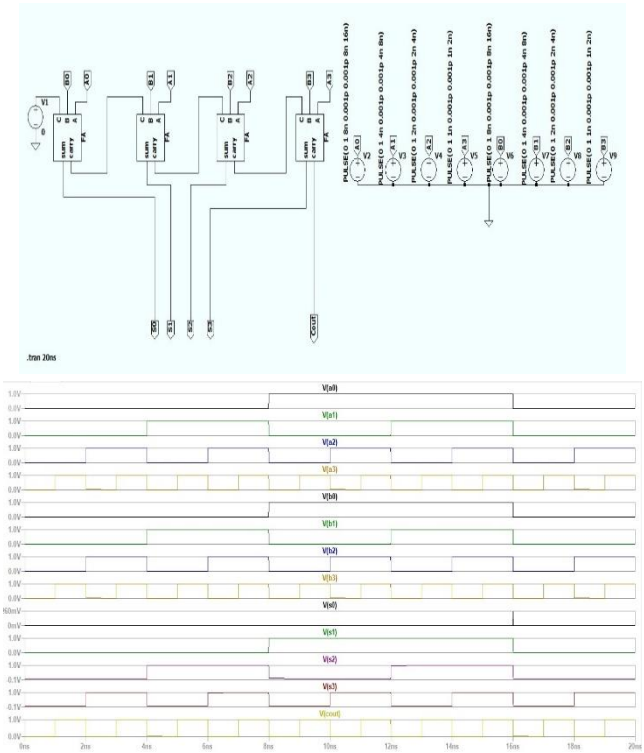


Fig.11. (a) RCA schematic and (b) RCA waveform

4.6 2-BIT VEDIC MULTIPLIER

The 2-Bit Vedic multiplier is designed and simulated with the use of GDI AND gate and GDI half adder with 20 FinFET transistors instead of 52 transistors in CMOS implementation.

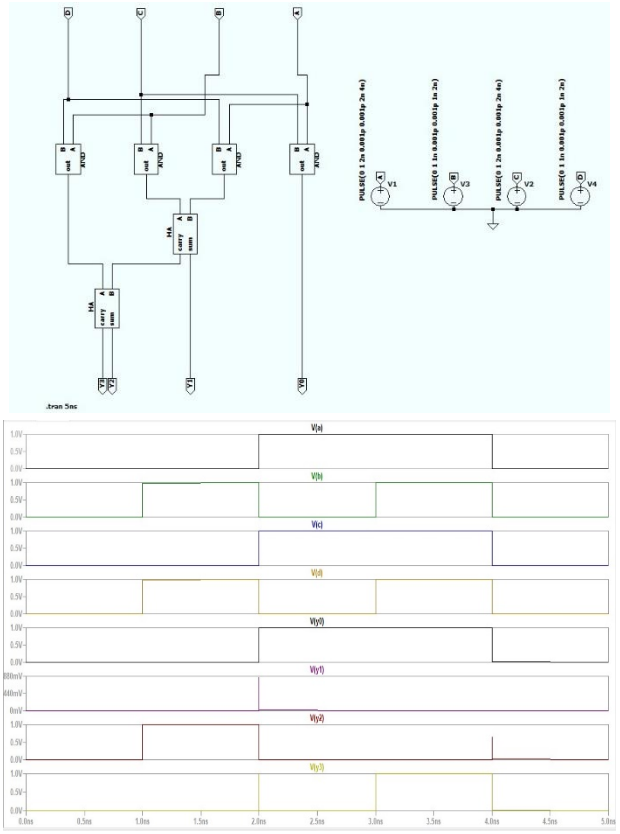
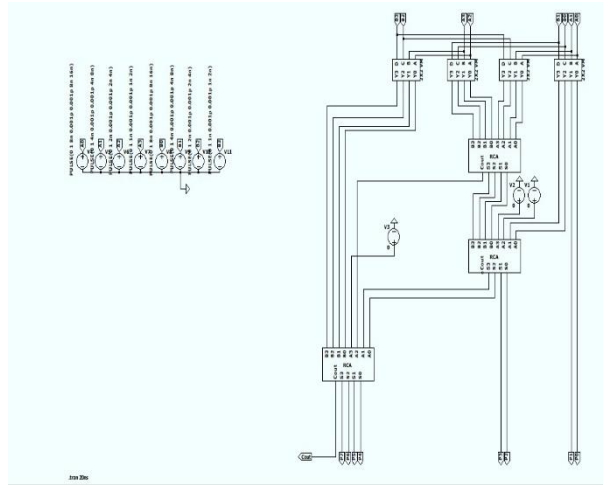


Fig.12. (a) 2-Bit Vedic Multiplier schematic and (b) 2-Bit Vedic Multiplier waveform

4.7 4-BIT VEDIC MULTIPLIER

The four bit Vedic multiplier is designed and simulated with the use of 2 bit GDI Vedic multiplier and 4-bit GDI RCA with 200 FinFET transistors instead of 484 transistors in CMOS implementation.



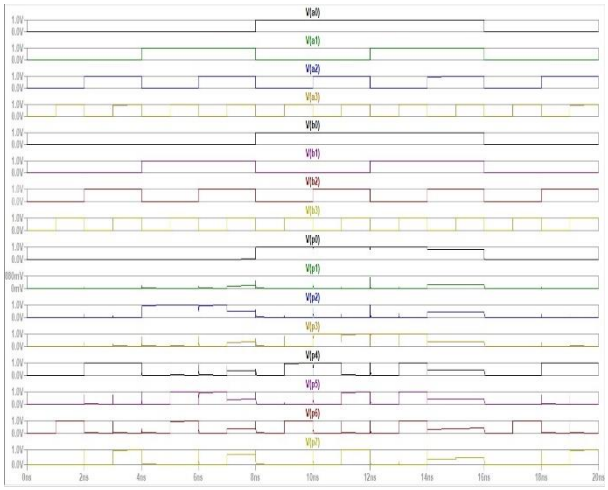


Fig.13. (a) 4-Bit Vedic Multiplier schematic and (b) 4-Bit Vedic Multiplier waveform

The proposed method in this paper focuses on improving the design and efficiency of a 4-bit Vedic multiplier by utilizing 16nm FinFET technology along with Gate Diffusion Input (GDI) logic. The primary motivation behind this approach is to reduce the overall transistor count and improve the performance in terms of power, area, and speed compared to conventional CMOS technology. GDI logic is used to simplify the design of basic logic gates, while FinFET devices address the second-order effects common in CMOS, such as short-channel effects, leakage current, and high-power consumption. In this implementation:

- AND Gate is designed using 2 FinFET transistors instead of 4 in CMOS.
- XOR Gate is implemented with 4 transistors, reducing the count from 12 in conventional CMOS.
- Half Adder is built using 6 transistors instead of 18, while the Full Adder uses only 10 transistors compared to 28 in the traditional CMOS approach.
- A 4-bit Ripple Carry Adder (RCA), essential in the Vedic multiplier design, requires only 40 FinFET transistors, compared to 92 in its CMOS counterpart.
- 2-bit Vedic Multiplier employs GDI AND gates and GDI Half Adder, reducing transistor count from 52 to 20.
- 4-bit Vedic Multiplier is constructed using 2-bit Vedic multipliers and a 4-bit RCA, significantly reducing the number of transistors from 484 in CMOS to 200 using the proposed method.

By integrating FinFET technology with GDI logic, this method demonstrates a substantial reduction in the transistor count and achieves improved performance metrics.

The implementation of the 4-bit Vedic multiplier using the proposed method shows remarkable improvement over conventional CMOS designs. The following key points highlight the results:

- **Transistor Count**: The transistor count in various circuit components such as AND, XOR, Half Adder, Full Adder, RCA, and Vedic multipliers is drastically reduced, as summarized in Table 1. This directly correlates with lower area consumption and reduced power requirements.
- **Efficiency**: The pictorial representation in Fig.14 demonstrates the overall efficiency gain by employing FinFET technology and GDI logic. The transistor count reduction is consistent across all components, leading to a more compact design with lower power consumption.
- **Performance**: FinFET devices offer better short-channel control, lower leakage current, and reduced power dissipation, which enhances the overall computational performance. The use of GDI logic further optimizes the design, making the proposed method highly suitable for high-speed digital signal processing applications.

In conclusion, the proposed 4-bit Vedic multiplier using 16nm FinFET technology with GDI logic proves to be a more efficient alternative to the traditional CMOS-based designs, with significant improvements in power, area, and speed.

4.8 EFFICIENCY

The Efficiency in terms of the number of transistors used in the conventional and proposed method is expressed in following table and it is pictured in the chart as follows.

Table.1. Number of transistors used in conventional and proposed methodology

Circuit	Conventional	Proposed
AND	4	2
XOR	12	4
Half Adder	18	6
Full adder	28	10
RCA	92	12
2 Vedic Multiplier	52	20
4 Vedic Multiplier	484	200

The Table.1 illustrates the comparison between the conventional CMOS-based design and the proposed method (using FinFET technology and GDI logic) in terms of transistor count for various components in the design of a Vedic multiplier.

- **AND Gate**: In the conventional method, an AND gate requires 4 transistors. However, using GDI logic in the proposed method, this is reduced to only 2 transistors, making the design simpler and more efficient.
- **XOR Gate**: The XOR gate, which typically uses 12 transistors in a conventional CMOS design, is optimized to require just 4 transistors in the proposed method due to the efficiency of GDI logic.
- **Half Adder**: A conventional Half Adder, which uses both AND and XOR gates, requires 18 transistors. The proposed method simplifies this design to only 6 transistors, greatly reducing the hardware complexity.
- **Full Adder**: The Full Adder in the conventional design uses 28 transistors. The proposed method reduces this number to 10 transistors, achieving significant savings in transistor count.
- **Ripple Carry Adder (RCA)**: A 4-bit RCA, which is composed of multiple Full Adders, uses 92 transistors in the conventional design. With the proposed method, this is

reduced to only 12 transistors, reflecting the impact of the GDI logic and FinFET efficiency.

- **2-bit Vedic Multiplier**: The conventional design of the 2-bit Vedic multiplier uses 52 transistors. By employing the proposed design with GDI logic, this number is reduced to 20 transistors.
- **4-bit Vedic Multiplier**: The conventional 4-bit Vedic multiplier, which combines multiple 2-bit multipliers, uses a substantial 484 transistors. The proposed method reduces this to 200 transistors, offering a significant improvement in both transistor count and design efficiency.

The proposed method, combining GDI logic and FinFET technology, leads to a substantial reduction in the number of transistors required for various logic circuits. This reduction directly results in improvements in power consumption, area efficiency, and speed, making the proposed design highly efficient for high-speed and low-power digital applications.

5. CONCLUSION

In this paper, 4-bit Vedic multiplier is designed using 16nm FinFET technology and GDI logic. The results from this implementation showed that there is a tremendous decrease in the use of transistors when compared to the conventional implementation of Vedic multiplier. The use of GDI decreases the transistor count and the use of FinFET eliminates the second order effects that are usual in CMOS implementation. Hence the efficiency of Vedic multiplication is considerably increased. While this paper demonstrates a significant reduction in transistor count and power consumption with the proposed 4-bit Vedic multiplier using 16nm FinFET technology and GDI logic, there is room for further optimization. Future work can focus on expanding the multiplier design to higher bit-widths, such as 8-bit and 16-bit Vedic multipliers, to address more complex DSP applications. Additionally, exploring the use of emerging materials, such as carbon nanotubes or graphene, could further enhance the performance of FinFET-based circuits. Another area of interest would be integrating the proposed design into larger systems, such as FFT processors or digital filters, to evaluate the overall impact on DSP system performance. Finally, optimizing the design for low-voltage operation can help in developing energy-efficient multipliers for battery-powered devices and IoT applications.

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