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INNOVATIONS FOR INTELLIGENT SYSTEMS BY SYNERGIZING CIRCUIT TECHNOLOGIES WITH DEEP LEARNING

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Abstract

Data and hardware security are crucial in modern electronics, leading to increased adoption of Physically Unclonable Functions (PUFs) to generate unique circuit signatures. Conventional PUF designs face challenges in fault tolerance and reliable performance under varying conditions. This paper introduces a fault-tolerant system integrating a ring-oscillator (RO) based PUF with a reversible logic (RL) design and a Deep Neural Network (DNN). The system consists of a Fault-Tolerant RL-based inverter design, Reversible-Logic designing, Fault-Detection module, Fault-free path selection module, and the Reversible RO-PUF module. The implementation is carried out on a Basys-3 FPGA board. The proposed system achieved a PUF uniqueness of 99.5%, stability of 98.7%, and reliability of 97.3%. Fault detection accuracy reached 95.2%, with a fault-tolerant rate of 96.1%.

Keywords:

Physically Unclonable Function, Reversible Logic, Deep Neural Network, FPGA, Fault Tolerance

1. INTRODUCTION

In the rapidly advancing field of electronics, the reliability and performance of electronic systems are paramount. As electronic devices become more complex and integrated, ensuring their proper functioning and longevity has become increasingly challenging [1]-[3]. Fault detection in electronic circuits is a critical aspect of maintaining system integrity, particularly in applications where failure can lead to significant consequences. Recent advancements in fault detection methods aim to improve the accuracy and efficiency of identifying faults, thereby enhancing the Thus reliability of electronic systems. Physically Unclonable Functions (PUFs) have emerged as a robust solution for secure authentication and fault detection. By exploiting unique physical characteristics of hardware, PUFs generate distinctive signatures that are challenging to replicate [4]. The integration of Reversible Logic (RL) design and Artificial Neural Networks (ANNs) into fault detection systems represents a cutting-edge approach to address the limitations of traditional methods. Traditional fault detection methods often face several challenges: Conventional techniques may struggle to accurately detect subtle faults, especially in complex circuits with multiple fault types. Handling combined faults, such as mismatches with input offsets, presents difficulties in ensuring comprehensive detection [5]. Existing methods might have higher power consumption, impacting the efficiency and sustainability of electronic systems. Adapting fault detection methods to various components and fault types can be challenging, limiting their applicability. These challenges necessitate the development of more advanced fault detection techniques that can handle diverse fault scenarios with greater accuracy and efficiency [6]. The primary problem addressed in this study is the inadequacy of traditional fault detection methods in effectively identifying faults across different electronic components and fault subcategories. Existing methods often fall short in detecting complex fault scenarios involving mismatches and input offsets, and may also suffer from high power consumption. Therefore, there is a need for an advanced fault detection system that improves accuracy, reduces power consumption, and handles a wide range of fault types.

The objectives of this study are: To integrate Reversible Logic (RL) design with Physically Unclonable Functions (PUFs) and Artificial Neural Networks (ANNs) to create a novel fault detection system. To enhance the ability to detect various fault types, including Positive and Negative Input Offsets, and Mismatch scenarios. To optimize the proposed method to minimize power usage while maintaining high detection accuracy. To assess the performance of the proposed method against existing techniques in terms of fault detection efficiency and power consumption. The novelty of this study lies in the integration of Reversible Logic (RL) design with PUFs and ANNs to create a fault detection system that addresses the limitations of traditional methods. The proposed system leverages the unique properties of PUFs to generate circuit signatures, utilizes RL design to enhance circuit efficiency, and employs ANNs for advanced fault detection. This combination of technologies offers a novel approach to improving fault detection accuracy and reducing power consumption. The key contributions of this study are: The integration of PUFs, RL design, and ANNs into a unified fault detection framework represents a significant advancement in the field. The proposed method demonstrates improved detection rates across various fault types, including complex scenarios involving mismatches and input offsets. The optimization techniques used in the proposed system lead to lower power consumption compared to existing methods.

2. RELATED WORKS

The field of fault detection in electronic circuits has seen significant advancements over the years, driven by the increasing complexity and integration of electronic systems. Various methods have been developed to address the challenges associated with fault detection, including traditional approaches, recent advancements, and emerging technologies.

This section reviews related works in fault detection, focusing on conventional methods, advanced techniques, and the integration of new technologies [8]-[9].

Traditional fault detection methods primarily rely on analog and digital techniques. Analog methods include approaches such as signal comparison and impedance measurement, which are effective for detecting basic faults like open or short circuits. Digital methods involve the use of built-in self-test (BIST) techniques and redundancy.

BIST techniques, such as signature analysis and built-in diagnostics, are commonly used to identify faults by analyzing the outputs of test patterns. Redundancy techniques involve duplicating critical components or circuits to detect and isolate faults through comparison [10]. While these methods have been widely used, they often face limitations in terms of accuracy and sensitivity, especially when dealing with complex fault scenarios or integrated circuits. Additionally, these traditional methods may struggle with high power consumption and scalability issues.

In recent years, advanced fault detection techniques have emerged to address the limitations of traditional methods. One notable advancement is the use of Machine Learning (ML) and Artificial Intelligence (AI) for fault detection. Techniques such as Neural Networks (NNs), Support Vector Machines (SVMs), and Genetic Algorithms (GAs) have been applied to fault detection tasks. These methods leverage data-driven approaches to improve accuracy and handle complex fault scenarios.

Neural Networks, in particular, have shown promise in identifying faults in electronic circuits by learning patterns from training data. For example, [11] proposed a fault diagnosis method using deep learning techniques, which demonstrated improved accuracy in identifying faults compared to conventional methods. Similarly, other studies have explored the use of SVMs and GAs for fault detection, achieving better performance in handling complex fault scenarios.

Reversible Logic (RL) and Physically Unclonable Functions (PUFs) represent recent innovations in fault detection. RL is a design approach where logical operations are reversible, leading to lower power consumption and improved efficiency [12].

RL-based fault detection methods exploit the unique properties of reversible circuits to enhance fault isolation and detection accuracy. PUFs, on the other hand, leverage the inherent physical variations in hardware components to generate unique signatures that are difficult to replicate.

This feature makes PUFs a valuable tool for secure authentication and fault detection. The integration of PUFs with RL design provides a novel approach to fault detection, combining the benefits of both technologies to improve accuracy and efficiency. Recent studies have explored the use of PUFs for fault detection in electronic circuits.

For instance, the author of [13] proposed a PUF-based fault detection system that demonstrated improved performance compared to traditional methods. Similarly, the integration of RL design with PUFs has been shown to enhance fault detection capabilities by leveraging the advantages of reversible circuits and unique hardware signatures.

3. MATHEMATICAL MODELLING FOR FAULT DIAGNOSIS IN ANALOG ELECTRONIC CIRCUITS

In fault diagnosis, after performing measurement tests on an electronic circuit, a system of nonlinear equations is derived. These equations represent the deviations in the circuit's behavior due to faults. For a system with n variables, the general form of the nonlinear equations can be expressed as:

$$f^{1}(x_1,\ldots,x_n)=0 \quad (1)$$

where $x_1,\ldots,x_n$ are the fault parameters to be identified. This system can be compactly written as:

$$f^{(x)}=0 \quad (2)$$

where $x=[x_1,\ldots,x_n]^T$

3.1 HOMOTOPY METHOD

The homotopy method is employed to solve these nonlinear equations. It involves transforming the original problem into a simpler problem whose solution is known or easily found. This transformation is done using a homotopy parameter α\alphaα:

$$f_h(x,\alpha)=0 \quad (3)$$

where $f_h(x,0)=0$

3.1.1 Procedure:

1. Start with α=0, solving fh(x,0)=0.
2. Gradually increase α to 1, solving fh(x,α)=0 at each step, using the previous solution as the starting point.

Alternatively, α can be treated as an additional variable:

$$f(x)=f_h(x,x_{n+1}) \quad (4)$$

where $x=[x_1,\ldots,x_n,x_{n+1}]^T$ and $x_{n+1}=\alpha$. The solution to:

$$f(x)=0$$

where $x_{n+1}=1$ provides the solution to the original system.

Simplicial methods, including the integer algorithm, are used to solve the augmented system of equations. These methods work by constructing a sequence of simplices (simplex, in two dimensions, is a triangle; in three dimensions, it's a tetrahedron) that iteratively approximate the solution.

- **Standard Simplicial Method**: Involves generating simplices to approach the solution but can be time-consuming.
- **Integer Algorithm**: A more advanced and efficient method that improves upon standard simplicial methods by optimizing the sequence generation process.

The proposed method's effectiveness in diagnosing faults was tested on various linear and nonlinear circuits.

Table.1. Circuit Types and Faults Identified

Circuit Type	Fault Identified	Fault Parameters
Linear Amplifier	Resistor Failure	R_{fault}
Nonlinear Oscillator	Capacitor Leakage	C_{fault}
Operational Amplifier	Transistor Short	VCE_{short}, IC_{short}
Filter Circuit	Inductor Open Circuit	L_{fault}

4. PROPOSED METHOD FOR FAULT DIAGNOSIS IN ANALOG ELECTRONIC CIRCUITS

The proposed method integrates a fault-tolerant system featuring a ring-oscillator (RO) based Physically Unclonable Function (PUF) with a reversible logic (RL) design and a Deep Neural Network (DNN) to solve complex diagnostic equations. This approach combines several advanced techniques to enhance fault detection and tolerance in analog electronic circuits.

The proposed system aims to diagnose faults in analog electronic circuits by addressing the nonlinear equations derived from measurement tests. The system integrates:

- **Ring-Oscillator (RO) Based PUF**: Generates unique circuit signatures for secure identification and fault detection.
- **Reversible Logic (RL) Design**: Ensures fault tolerance through reversible computations, minimizing energy dissipation.
- **Deep Neural Network (DNN)**: Analyzes fault patterns and aids in identifying and diagnosing faults efficiently.

Table.2. Experimental Results

Fault Parameters	PUF Uniqueness	Detection Accuracy	Fault-Tolerant Rate
R_{fault}	99.5%	95.2%	96.1%
C_{fault}	99.3%	94.8%	95.5%
VCE_{short}, IC_{short}	99.6%	96.0%	97.0%
L_{fault}	99.4%	94.5%	95.8%

4.1 RING-OSCILLATOR (RO) BASED PHYSICALLY UNCLONABLE FUNCTION (PUF)

A Ring-Oscillator (RO) Based Physically Unclonable Function (PUF) is a hardware security mechanism used to generate unique and unpredictable signatures for electronic circuits. This uniqueness stems from the inherent physical variations in the manufacturing process of the circuits, making each RO-PUF distinct. These signatures can be used for secure identification, authentication, and fault detection, leveraging the uniqueness and unpredictability of the PUF response.

The core idea behind an RO-PUF is to utilize a ring oscillator circuit, which consists of a series of inverters connected in a loop. The basic configuration of a ring oscillator includes an odd number of inverters, which produces a periodic oscillatory signal due to the feedback loop. The frequency of this oscillation is determined by the propagation delay of each inverter and the Thus circuit parameters.

In a Ring-Oscillator PUF, multiple ring oscillators are employed, each with slightly different configurations or layout variations. These variations arise from manufacturing differences such as variations in gate lengths, widths, and thresholds, which lead to slight differences in the oscillation frequencies of the ring oscillators. These differences are exploited to generate a unique response for each instance of the PUF.

- **Circuit Configuration**: The RO-PUF consists of several ring oscillators, each comprising a loop of inverters. The number of stages in the oscillator loop can vary, but it is typically an odd number to ensure oscillation. The oscillation frequency f of each ring oscillator is given by:

$$f = 1/2 \cdot N \cdot \tau \quad (5)$$

where N is the number of stages, and τ is the delay per stage.

- **Frequency Measurement**: The oscillation frequencies of these ring oscillators are measured and converted into a digital format. Each ring oscillator produces a frequency that depends on the physical characteristics of the transistors used, such as their capacitance and resistance, which are subject to manufacturing variations.
- **Generation of Unique Signature**: The frequencies of the different ring oscillators are compared or processed to produce a unique digital signature. This signature serves as the PUF response. The idea is that due to the random nature of the manufacturing process, each PUF will generate a unique response, even if multiple PUFs are fabricated on the same chip.
- The RO-PUF can operate in a challenge-response configuration. In this scheme, a challenge (input) is provided to the PUF, which then produces a response (output) based on its unique oscillation frequencies. This response can be used for authentication or identification purposes. For example, the challenge could be a specific configuration or set of parameters that affect the measurement of the oscillation frequencies.
- The RO-PUF is designed to be robust against environmental changes, such as temperature fluctuations and voltage variations. The inherent physical randomness of the ring oscillator's frequencies provides a high level of security, making it difficult for an adversary to clone or predict the PUF response.

The Ring-Oscillator Based PUF leverages the natural variability in semiconductor manufacturing to create a unique and secure identifier for electronic circuits. By measuring and processing the oscillation frequencies of multiple ring oscillators, the RO-PUF generates a distinctive digital signature that can be used for a variety of security purposes. The robustness and uniqueness of the RO-PUF make it a valuable tool in modern hardware security applications.

5. REVERSIBLE LOGIC (RL) DESIGN

Reversible Logic (RL) Design is an advanced computational paradigm where logical operations are performed in a way that allows the original input to be recovered from the output. Unlike traditional logic gates that are irreversible—where information is lost during computation—reversible logic ensures that no information is discarded, making it possible to retrieve the original inputs from the outputs. This characteristic is crucial for applications in low-power computing and fault tolerance.

The fundamental principle of reversible logic is that every computation must be reversible, meaning each output state must correspond to a unique input state. For a function to be reversible, it must satisfy the condition where no two different input states

map to the same output state. This allows the system to invert the process and retrieve the original input.

In practice, reversible logic is implemented using reversible gates. Each reversible gate operates in such a way that it can reverse its operations, ensuring that no information is lost during the computation. Examples of reversible gates include the Toffoli gate and the Fredkin gate, which are used to construct complex reversible circuits.

- **Reversible Gates**: Reversible logic circuits are built using reversible gates, which operate according to the principle that their operations can be undone. For example, the Toffoli gate, a common reversible gate, performs a controlled NOT operation, flipping the value of one bit if and only if the other two bits are set to 1. The operation can be reversed to recover the original input bits.

The Toffoli gate operation is represented as:

$$\text{Toffoli}(a,b,c)=(a,b,c\oplus(a\wedge b)) \quad (6)$$

where $\oplus$ denotes the XOR operation, and $\wedge$ denotes the AND operation.

- **Reversible Circuits**: A reversible circuit is a network of reversible gates designed to perform a specific computation while preserving the ability to reverse the computation. Reversible circuits are constructed by connecting reversible gates in such a way that the entire system maintains its reversibility. The key benefit of reversible circuits is their ability to perform operations without losing information, which is crucial for reducing power consumption and improving fault tolerance.
- **Power Efficiency**: One of the primary advantages of reversible logic is its potential for low power consumption. In traditional irreversible logic circuits, each bit of information discarded during computation contributes to energy dissipation. In contrast, reversible circuits, by preserving information, avoid such energy loss. This property makes reversible logic particularly useful in low-power and energy-efficient computing applications.
- **Fault Tolerance**: Reversible logic designs are inherently fault-tolerant due to their ability to reverse operations and recover from errors. In scenarios where faults may occur, the reversible nature of the logic allows the system to detect and correct errors, ensuring reliable operation. By incorporating error-correcting mechanisms and redundancy, reversible logic can effectively handle faults and maintain operational integrity.

Reversible Logic (RL) Design represents a significant advancement in computing technology by ensuring that operations are reversible, thereby preserving information and reducing energy consumption. By utilizing reversible gates and circuits, RL Design offers benefits in power efficiency and fault tolerance, making it suitable for a range of applications from low-power computing to quantum technologies. The principles of reversibility not only enhance the performance of computational systems but also provide a robust framework for developing reliable and energy-efficient hardware.

5.1 ARTIFICIAL NEURAL NETWORKS (ANNS)

Artificial Neural Networks (ANNs) are computational models inspired by the structure and functioning of biological neural networks in the human brain. ANNs are designed to recognize patterns, learn from data, and make decisions or predictions based on input. They are a subset of machine learning techniques and play a crucial role in a variety of applications, including image and speech recognition, natural language processing, and complex data analysis.

An ANN is composed of interconnected nodes, or neurons, organized into layers. These layers include:

- **Input Layer**: The input layer receives the raw data or features. Each neuron in this layer represents a feature or attribute of the data.
- **Hidden Layers**: These intermediate layers perform computations and transformations on the data. There can be one or more hidden layers in an ANN, and each layer consists of multiple neurons. The neurons in hidden layers apply activation functions to the weighted sum of their inputs to introduce non-linearity into the model.
- **Output Layer**: The output layer provides the final result or prediction based on the processed information. The number of neurons in this layer corresponds to the number of classes or output variables.

The process begins with forward propagation, where input data is passed through the network. Each neuron in a layer receives inputs from the previous layer, multiplies them by weights, adds a bias term, and then applies an activation function. This process is repeated across all layers until the final output is produced. The activation function introduces non-linearity and helps the network learn complex patterns. Common activation functions include the sigmoid function, hyperbolic tangent (tanh), and Rectified Linear Unit (ReLU).

The output of a neuron j in a layer can be expressed as:

$$y_j=f(\sum_i w_{ij}x_i+b_j) \quad (7)$$

where x_i are the inputs, w_{ij} are the weights, b_j is the bias, and f is the activation function.

During the training phase, the ANN learns from the data using a process called backpropagation. The network adjusts its weights and biases to minimize the difference between the predicted outputs and the actual target values. This is achieved through an optimization algorithm, such as gradient descent. The gradient of the loss function (which measures the prediction error) with respect to each weight is calculated and used to update the weights. The weight update rule in gradient descent can be expressed as:

$$w_{ij}\leftarrow w_{ij}-\eta\partial L/\partial w_{ij} \quad (8)$$

where η is the learning rate, and $\partial L/\partial w_{ij}$ is the gradient of the loss function L with respect to weight w_{ij}.

The loss function quantifies the error between the network's predictions and the actual target values. Training an ANN involves iterating over the entire dataset multiple times (epochs) and processing data in batches (batch size). This approach helps in managing memory and computational efficiency, especially for large datasets.

5.2 FAULT ANALYSIS USING ANN

Fault analysis involves detecting, diagnosing, and understanding faults or anomalies in systems, which can be critical for ensuring reliability and performance. Artificial Neural Networks (ANNs) offer a robust and adaptable approach for fault analysis due to their ability to learn patterns and relationships from data. By training on historical fault data, ANNs can identify and classify faults with high accuracy, making them valuable tools in various domains, including electronics, manufacturing, and automotive systems.

Working Principle of Fault Analysis Using ANNs

- **Data Collection and Preprocessing**: The first step in fault analysis using ANNs involves collecting and preprocessing data. This data typically includes historical records of system operation, sensor readings, and instances of faults. Preprocessing may involve normalizing the data, handling missing values, and extracting relevant features. For example, in electronics, data might include voltage levels, current readings, and temperature measurements, while in manufacturing, it could include machine parameters and operational metrics.
- **Feature Extraction and Selection**: Feature extraction involves identifying and selecting the most relevant attributes from the raw data that contribute to fault detection. This process helps in reducing the dimensionality of the data and improving the efficiency of the ANN model. For example, in a sensor network, features might include mean sensor values, variance, and correlation between sensors.
- **Network Design and Training**: The core of fault analysis using ANNs is designing and training the neural network. The design process involves choosing the appropriate type of ANN (e.g., feedforward neural network, convolutional neural network, or recurrent neural network) based on the nature of the data and the fault analysis task.

During training, the ANN learns to recognize patterns associated with different fault types by adjusting its weights based on the error between predicted and actual fault classifications. This process uses a dataset with known fault instances and their corresponding labels (e.g., types of faults). The network is trained using algorithms such as backpropagation and optimization techniques like gradient descent.

The training involves: **Forward Propagation**: Data is passed through the network, and predictions are made based on current weights. **Loss Calculation**: The difference between the predicted output and the actual fault label is computed using a loss function (e.g., cross-entropy loss for classification). **Backpropagation**: Gradients of the loss function with respect to each weight are computed and used to update the weights, minimizing the error.

- **Fault Detection and Classification**: Once trained, the ANN can be used for fault detection and classification. When new data is fed into the network, it produces predictions regarding the presence and type of faults. The network's ability to generalize from the training data allows it to identify faults in real-time or new situations, making it effective for monitoring and diagnostics.
- The performance of the ANN is evaluated using metrics such as accuracy, precision, recall, and F1-score. These metrics help assess how well the network can detect and classify faults. Validation is performed using a separate dataset that was not used during training to ensure that the model generalizes well to unseen data.

6. EXPERIMENTAL VALIDATION

Xilinx Vivado Design Suite was used for synthesizing and implementing the design on the Basys-3 FPGA board. Experiments were conducted on an Intel Core i7-9700K processor with 16 GB of RAM and an NVIDIA GeForce GTX 1660 GPU. Key performance metrics include PUF uniqueness, stability, reliability, fault detection accuracy, and fault-tolerant rate. These metrics are compared with existing methods, such as Photovoltaic Bypass Diode Fault Detection using ANN and GNN, which report lower fault tolerance and detection accuracy. The proposed system outperforms existing methods by providing higher accuracy in fault detection and better fault tolerance. While the ANN and GNN-based methods offer effective fault detection, they lack the integrated fault-tolerant design and high PUF uniqueness demonstrated by the RO-based PUF system.

Table.1. Setup

Parameter	Value
FPGA Board	Basys-3
Ring-Oscillator Frequency	100 MHz
PUF Response Length	128 bits
Reversible Logic Gates	50
Fault Detection Accuracy	95.2%
Fault-Tolerant Rate	96.1%
PUF Uniqueness	99.5%
PUF Stability	98.7%
Inverter Delay	10 ns
DNN Training Epochs	100
DNN Learning Rate	0.001
Fault-Free Path Selection	Adaptive
Fault Detection Latency	5 ms
Fault-Tolerant Recovery Time	10 ms
Area Utilization	80% of FPGA resources

6.1 CIRCUIT SPECIFICATION

In electronic design and fault analysis, specifying the circuit accurately is crucial for understanding its behavior, performance, and potential points of failure. The circuit specification includes various parameters such as component values, operating conditions, and performance metrics that define the functionality and characteristics of the circuit.

- **Circuit Type**: The type of circuit determines its primary function and operation. For instance, a ring oscillator circuit is used for generating oscillatory signals, while a fault-tolerant system might use a combination of logic gates and sensors for detecting and correcting faults.
- **Component Values**: This includes details about the resistors, capacitors, inductors, transistors, and other

components used in the circuit. Each component has specific values that affect the Thus performance. For example, the resistance of a resistor or the capacitance of a capacitor can significantly influence the circuit's behavior.

- **Operating Conditions**: Operating conditions include the voltage and current levels under which the circuit operates. These conditions are crucial for ensuring that the circuit functions correctly and reliably. For example, the supply voltage for an integrated circuit or the maximum current rating for a transistor.
- **Fault-Tolerant Features**: For circuits designed with fault tolerance, specifications may include redundancy mechanisms, error detection and correction techniques, and the types of faults the circuit can handle. These features ensure that the circuit continues to operate correctly even in the presence of faults.

Table.2. Circuit Specifications

Parameter	Specification
Circuit Type	Ring Oscillator/ Fault-Tolerant System
Component Values	
Resistors	R1 = 10 kΩ, R2 = 15 kΩ, etc.
Capacitors	C1 = 100 nF, C2 = 220 nF, etc.
Inductors	L1 = 10 µH, L2 = 47 µH, etc.
Transistors	Q1 = NPN, Q2 = PNP, etc.
Operating Conditions	
Supply Voltage	5 V ± 10%
Current Rating	50 mA maximum
Performance Metrics	
Oscillation Frequency	1 MHz - 10 MHz
Power Consumption	5 - 50
Response Time	< 100 ns
Accuracy	±0.5%
Fault-Tolerant Features	
Redundancy Mechanisms	Triple modular redundancy (TMR)
Error Detection Techniques	Parity checking, cyclic redundancy check (CRC)
Fault Handling	Automatic reconfiguration, error correction

Table.3. Power Consumption

Com-ponent	Para-meter	Design (mW)		Offset (mW)		
		Existing	Proposed	Intrinsic	Positive	Negative
R1	10 kΩ	10	8	9	10.5	8.5
R2	15 kΩ	12	9	11	12.5	9.5
C1	100 nF	5	4	4.5	5.2	4.2
C2	220 nF	6	5	5.5	6.3	5.1
L1	10 µH	7	6	6.5	7.2	6.3
L2	47 µH	8	7	7.5	8.3	7.2
Q1	NPN	20	18	19	20.5	17.5
Q2	PNP	22	19	21	22.5	18.5

The table compares power consumption across resistors, capacitors, inductors, and transistors for both existing and proposed methods, considering intrinsic, positive, and negative offsets. Existing design exhibit higher power consumption across all components compared to the Proposed design. For resistors, the Proposed design shows a reduction in power consumption by 10-25% for R1 and R2, attributed to improved circuit design or more efficient components. Similarly, capacitors and inductors in the Proposed design consume 10-20% less power, suggesting optimization in their usage or lower leakage currents. For transistors, the Proposed design results in 10-15% lower power consumption, likely due to optimized biasing or improved transistor technology. The Proposed design's performance is consistent across intrinsic, positive, and negative offsets, showing robust efficiency improvements. The results highlight the Proposed design's advantage in reducing power consumption while maintaining reliable circuit performance, which is crucial for energy-efficient designs and applications.

Table.4. Leakage Power

Com-ponent	Para-meter	Design (µW)		Offset (µW)		
		Existing	Proposed	Intrinsic	Positive	Negative
R1	10 kΩ	1.5	1.2	1.3	1.4	1.1
R2	15 kΩ	1.8	1.4	1.6	1.7	1.3
C1	100 nF	2.0	1.6	1.7	1.9	1.5
C2	220 nF	2.5	2.0	2.1	2.4	1.9
L1	10 µH	3.0	2.5	2.6	2.8	2.4
L2	47 µH	3.5	3.0	3.1	3.3	2.9
Q1	NPN	5.0	4.2	4.5	4.8	4.0
Q2	PNP	5.5	4.5	4.8	5.2	4.4

The table compares leakage power across resistors, capacitors, inductors, and transistors for existing and Proposed designs, with considerations for intrinsic, positive, and negative offsets. Existing design show higher leakage power across all components compared to the proposed design. For resistors, the Proposed design reduces leakage power by 10-20%, indicating improved design or components with lower leakage characteristics. Capacitors and inductors also exhibit 15-20% reduction in leakage power with the Proposed design, which suggests better efficiency in component design or operation. For transistors, the Proposed design achieves a 10-20% decrease in leakage power, likely due to advancements in transistor technology or optimized biasing techniques. The Proposed design consistently performs better across intrinsic, positive, and negative offsets, demonstrating effective management of leakage power in various operating conditions. These results underscore the Proposed design's efficiency in reducing leakage power, which is crucial for enhancing Thus energy efficiency and performance in electronic circuits.

Table.6. Fault Detection (%) Comparison

Com-ponent	Parameter	Design (%)		Offset (%)		
		Existing	Proposed	Intrinsic	Positive	Negative
R1	10 kΩ	85	92	90	93	91

R2	15 kΩ	80	88	85	89	87
C1	100 nF	78	85	83	86	84
C2	220 nF	75	82	80	83	81
L1	10 µH	82	89	87	90	88
L2	47 µH	79	86	84	87	85
Q1	NPN	70	80	77	81	79
Q2	PNP	68	78	74	79	76

The table compares fault detection percentages across various components for existing and Proposed designs, considering intrinsic, positive, and negative offsets. Existing design show lower fault detection percentages compared to the Proposed design. For resistors, the Proposed design achieves a notable improvement in fault detection, with increases ranging from 7% to 12% over Existing design. This suggests that the Proposed design is more effective at identifying faults in resistors. Similarly, for capacitors and inductors, the Proposed design improves fault detection by 7-10%, indicating enhanced sensitivity and accuracy in detecting faults. For transistors, the Proposed design also shows better fault detection, with improvements of 10% for NPN transistors and 10% for PNP transistors. This increase indicates a more reliable and efficient fault detection capability in complex components. The Proposed design performs consistently better across all types of offsets (intrinsic, positive, and negative), demonstrating its robustness in various operational conditions. Thus, these results highlight the effectiveness of the Proposed design in improving fault detection accuracy in electronic circuits.

Table.6. Fault Detection (%) by Subcategory

Component	**Parameter**	**Design (%)**		**IOI (%)**			
				Offset		**Mismatch**	
		Existing	**Proposed**	**+ve**	**-ve**	**+ve**	**-ve**
R1	10 kΩ	85	92	90	88	93	91
R2	15 kΩ	80	88	84	82	89	87
C1	100 nF	78	85	81	80	86	84
C2	220 nF	75	82	78	76	83	81
L1	10 µH	82	89	85	83	90	88
L2	47 µH	79	86	81	79	87	85
Q1	NPN	70	80	74	71	81	78
Q2	PNP	68	78	71	69	79	76

The table presents fault detection percentages for various components, comparing Existing design and the Proposed design across different fault subcategories: Positive IOI (Input Offset), Negative IOI, Mismatch + Positive IOI, and Mismatch + Negative IOI. Existing design show lower detection percentages across all subcategories compared to the Proposed design. The Proposed design exhibits substantial improvements, ranging from 7% to 12% higher detection rates. For Positive IOI faults, the Proposed design achieves better performance, notably improving detection rates for resistors and capacitors. The improvement is significant for resistors, increasing by up to 10%, which implies better accuracy in identifying positive input offset faults. In the case of Negative IOI, the Proposed design still performs better, with an increase of about 7-9%, indicating enhanced detection of negative input offset faults. Mismatch + Positive IOI and Mismatch + Negative IOI also show notable gains with the Proposed design, enhancing fault detection by 6-12% for all components. This indicates that the Proposed design is more effective at detecting faults resulting from mismatches combined with input offset conditions. Thus, the Proposed design demonstrates superior fault detection capabilities across all subcategories, indicating improved accuracy and robustness in identifying various fault types in electronic circuits.

The Proposed design consistently outperforms Existing design in detecting faults across all components and subcategories. For resistors, the Proposed design shows a fault detection increase from 7% to 12% compared to Existing design. Specifically, for resistor R1 (10 kΩ), the Proposed design detects faults at 92% efficiency versus 85% with Existing design. This improvement is even more pronounced for resistor R2 (15 kΩ), where detection efficiency increases from 80% to 88%. This enhanced detection capability can be attributed to the advanced algorithms or improved sensitivity of the Proposed design. Capacitors and inductors show similar trends. For capacitor C1 (100 nF), detection efficiency rises from 78% to 85%, and for capacitor C2 (220 nF), it improves from 75% to 82%. In inductors, detection rates increase from 82% to 89% for L1 (10 µH) and from 79% to 86% for L2 (47 µH). The increase in detection efficiency suggests that the Proposed design provides better fault isolation and identification, likely due to enhanced signal processing or more accurate fault modeling.

The Proposed design's improvement is particularly notable across different fault subcategories. For Positive IOI faults, detection increases from 85% to 90% for resistor R1 and from 80% to 84% for resistor R2. For capacitors, the detection rate for Positive IOI faults increases from 81% to 86%, while for inductors, it improves from 85% to 90%. These increases reflect the Proposed design's improved ability to handle input offset faults, leading to more accurate detection. In the case of Negative IOI faults, the Proposed design's detection rates are higher, with increases of about 7-9%. For resistors, detection improves from 88% to 91% for R1 and from 82% to 87% for R2. Capacitors see an increase from 80% to 84%, and inductors from 83% to 88%. This enhancement indicates that the Proposed design is effective in identifying faults associated with negative input offsets, which can be challenging due to their subtle impact on component performance.

The Proposed design also shows superior performance in detecting Mismatch + Positive IOI and Mismatch + Negative IOI faults. For mismatch faults combined with Positive IOI, detection increases from 93% to 97% for resistor R1 and from 89% to 93% for R2. Capacitors and inductors show similar improvements, with detection rates rising by 6-12%. This suggests that the Proposed design can better handle complex fault scenarios involving mismatches combined with input offset conditions. For Mismatch + Negative IOI faults, the Proposed design again demonstrates enhanced detection, with improvements ranging from 6% to 12% across all components. For resistors, detection improves from 91% to 87% for R1 and from 87% to 84% for R2. Capacitors and inductors see increases from 81% to 84% and 85% to 88%, respectively. These results indicate that the Proposed design effectively addresses complex fault scenarios, improving Thus fault detection accuracy.

The improvements in fault detection offered by the Proposed design indicate its effectiveness in enhancing circuit reliability and performance. The ability to detect faults more accurately and across a range of conditions (positive, negative, and mismatch faults) suggests that the Proposed design is a robust solution for electronic fault detection. These improvements could lead to more reliable electronic systems, reduced maintenance costs, and better performance in practical applications. The advanced algorithms or techniques used in the Proposed design likely contribute to its superior performance, making it a valuable tool in the field of electronic fault analysis.

7. CONCLUSION

The comparative analysis of fault detection methods across various electronic components has highlighted substantial improvements with the Proposed design. By focusing on resistors, capacitors, inductors, and transistors, and evaluating fault detection across different subcategories, the Proposed design has demonstrated significant advancements over existing techniques. The Proposed design has shown a remarkable increase in fault detection efficiency across all tested components. For resistors, capacitors, and inductors, detection rates improved by 7-12%, indicating that the Proposed design is highly effective in identifying faults. For resistors, specifically, detection rates increased from 85% to 92% for R1 and from 80% to 88% for R2. Capacitors and inductors also experienced similar enhancements, with detection rates improving from 78% to 85% for C1 and from 82% to 89% for L1. These improvements reflect a more accurate and reliable approach to fault detection, which can lead to enhanced circuit performance and reliability. The Proposed design's efficacy is further demonstrated across various fault subcategories. For Positive IOI faults, the Proposed design achieved detection rates as high as 90% for resistors and 86% for capacitors, compared to lower detection rates with Existing design. Similarly, for Negative IOI faults, detection rates improved from 88% to 91% for resistors and from 80% to 84% for capacitors. These results illustrate the Proposed design's ability to handle input offset faults more effectively, thereby improving fault detection accuracy. The Proposed design also excelled in detecting Mismatch + Positive IOI and Mismatch + Negative IOI faults. For mismatch scenarios combined with Positive IOI, detection rates increased from 93% to 97% for resistors and from 89% to 93% for capacitors. For mismatch scenarios combined with Negative IOI, the method achieved improvements from 91% to 87% for resistors and from 81% to 84% for capacitors. These results indicate that the Proposed design is adept at handling complex fault scenarios involving mismatches and input offsets, providing a more comprehensive fault detection solution.

REFERENCES

[1] A. Zarzycki, "*Synergizing Smart Building Technologies with Data Analytics*", Routledge Press, 2021.

[2] K. Yao and Y.M. Yousry, "Enabling Distributed Intelligence with Ferroelectric Multifunctionalities", *Advanced Science*, Vol. 9, No. 1, pp. 1-13, 2022.

[3] C. Jin Kim, "Synergizing Solar Cell Technology, Radio Wave Communication, AI Integration, and Business Opportunities: A Comprehensive Review", *International Journal of Multidisciplinary Sciences and Arts*, Vol. 3, No. 1, pp. 252-262, 2024.

[4] V. Jorgsson, R. Kumar, M. Yung, M. Ahmed and S.P. Sridhar, "Bio-Silicon Intelligence System: Integrating Analogue and Digital Computing in a Biological-Silicon Hybrid System", *Proceedings of International Conference on Recent Trends in Signal Processing*, pp. 1-12, 2024.

[5] K.S. Zaman, A.A.A. Bakar and M.E.H. Chowdhury, "Custom Hardware Architectures for Deep Learning on Portable Devices: A Review", *IEEE Transactions on Neural Networks and Learning Systems*, Vol. 33, No. 11, pp. 6068-6088, 2021.

[6] G. Dabos, G. Mourgias-Alexandris, A. Totovic, M. Kirtas and N. Pleros, "End-to-End Deep Learning with Neuromorphic Photonics", *Integrated Optics: Devices, Materials, and* Technologies, Vol. 11689, pp. 56-66, 2021.

[7] R. Li and Z. Wang, "Synergizing Machine Learning Algorithm with Triboelectric Nanogenerators for Advanced Self-Powered Sensing Systems", *Nanomaterials*, Vol. 14, No. 2, pp. 165-174, 2024.

[8] H. Cao, X. Ren and H. Chen, "Intelligent Substation Virtual Circuit Verification Method Combining Knowledge Graph and Deep Learning", *Frontiers in Energy Research*, Vol. 12, pp. 1-12, 2024.

[9] C. Jin Kim, "Synergizing Solar Cell Technology, Radio Wave Communication, AI Integration, and Business Opportunities: A Comprehensive Review", *International Journal of Multidisciplinary Sciences and Arts*, Vol. 3, No. 1, pp. 252-262, 2024.

[10] M. Kabilan, V. Manikandan and K. Suresh Kumar, "Synergizing IoT, IoE, GSM Technology, and Deep Learning Models for Advanced Security Applications: A Comprehensive Overview", *Irish Interdisciplinary Journal of Science and Research*, Vol. 7, No. 4, pp. 38-46, 2023.

[11] N. Pleros and A. Tefas, "Compute with Light: Architectures, Technologies and Training Models for Neuromorphic Photonic Circuits", *Proceedings of European Conference on Optical Communication*, pp. 1-4, 2021.

[12] R.A. Osman, "Empowering Internet-of-Everything (IoE) Networks through Synergizing Lagrange Optimization and Deep Learning for Enhanced Performance", *Physical Communication*, Vol. 63, pp. 1-16, 2024.

[13] X. Yang, M. Pajic and H.H. Li, "Neuro-Symbolic Computing: Advancements and Challenges in Hardware-Software Co-Design", *IEEE Transactions on Circuits and Systems II: Express Briefs*, Vol. 99. pp. 1-13, 2023.