

DRAIN CURRENT CHARACTERISTICS OF SILICON NANOWIRE FIELD EFFECT TRANSISTOR

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Abstract

This paper presents the simulation study of characteristics of an 11nm Silicon Nanowire Field Effect Transistor. This architecture is applicable for ultra-scaled devices up to sub-11 nm technology nodes that employ silicon films of a few nm in thickness. The defining characteristics of ultrathin silicon devices such as Short Channel Effects and Quasi-Ballistic transport are considered in modelling the device. Device geometries play a very important role in short channel devices, and hence their impact on drain current is also analyzed by varying the silicon and oxide thickness. The proposed simulation model gives a detailed outlook on the characteristics of the nanowire device in the inversion regime.

Keywords:

Nanowire Transistors, Drain Current Characteristics

1. INTRODUCTION

Silicon CMOS has been the technology of choice of the Nano electronics industry for the past four decades. In this regard, Metal-Oxide-Semiconductor Field-Effect Transistors (MOSFETs) have become the fundamental building blocks of Very Large Scale Integrated circuits (VLSI) due to their excellent properties. The demand for higher integration density, low power consumption, high speed and low cost requires aggressive scaling of the MOSFETs. While scaling down the device, as the channel length of a MOSFET is reduced, departures from long channel behavior are expected to occur. These deviations are called as “Short-Channel Effects” (SCEs), which are the results of a two-dimensional potential distribution and high electric fields in the channel region. Hence, in these conditions, Silicon Nanowire Transistors have garnered a huge attention in the modern semiconductor industry as the alternate option for the conventional MOSFETs due to their highly improved electrical and optical properties. Several works have contributed to the boom of research on nanowire transistors. Nanowires are predicted to be relevant for technology nodes below 11nm implying a silicon film of some nanometers in diameter [1]. The reduction of t_{ox} leads to degradation of the effective carrier mobility has been reported in [2]. A degradation mechanism is remote surface roughness-scattering. Carrier in channel is affected by the surface roughness between gate oxide and poly-silicon interface.

Ramayya [3] reported that the small-diameter SiNWs have high carrier mobility. The high carrier mobility is essential for fabricating high performance FETs. These SiNWs-related nano FETs are quite sensitive because SiNWs have high surface-to-volume ratio which ensures that relatively mass carriers can be controlled easily by weak electrical field applied on the gate. The Concept of multiple gates is to get a greater control over the channel through multiple gate terminals and a better solution for the short channel effects arise in these transistors. The multiple

gate transistors effectively reduce the short channel effects and improve the performance. The available multiple gate transistors are double gate (two gates), tri gate (three gates), Quad Gate, Surrounding gate, Omega gate and Gate all around transistors etc. Double gate transistors are having two gates on the top and bottom of the substrate. In case of a silicon Nanowire transistor, the Nanowire itself acts as the substrate. The nanowires are available in different device geometries like rectangular and cylindrical. And depending upon the shape of the nanowires the transistors are formed accordingly as double gate, cylindrical gate and GAA (gate all around) structures [10] [11].

In addition, dual-gated silicon nanowire transistors that have top and back gates to control the FETs also realized unipolar behavior [4]. The back gate influences the whole of SiNWs channel and the top gate influences part of it. Compared to normal nano-FETs, dual-gated transistors impose an energy barrier by the top gate that affect transport of carriers and become unipolar in some controlled gate voltage regimes. It is demonstrated that the top gate can control the ambipolar conduction in SiNWs-related FETs effectively with an improved on/off current ratio. More recently, researchers have developed gate-all around (GAA) FET [5-7], where the channel body is all covered by gate and thus provide better electrostatic control of the channel. The fabricated GAA nanowire transistors show the best performance among those reported so far in terms of high drive current, near ideal subthreshold slope, lowering drain-induced barrier (DIBL), and high Ion/Ioff ratio. The transistors also exhibit a substrate-bias-independent threshold voltage (V_{th}) as a result of the complete electrostatic shielding of the channel.

In this work, we present the I_{ON} current characteristics on a Silicon nanowire FET's using 2D simulator PADRE [9]. I_{ON} current variation with several important device parameters (oxide and silicon channel thickness, doping concentration) is obtained from simulations. The results are of vital importance for characterizing the transport and variability in emerging research devices.

2. DEVICE STRUCTURE AND SIMULATION

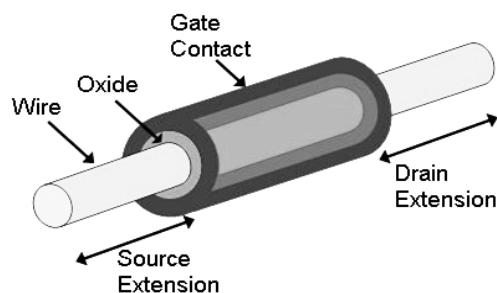


Fig.1. Schematic structure of the Nanowire FET device

Nanowire FETs are considered to be excellent candidates for maintaining the relentless progress in scaling for semiconductor devices. Several things have contributed to the boom of research on nanowire transistors. First, they can be produced in high yield with reproducible electronic properties as per the requirements for ULSI applications. Second, “bottom-up” synthesized nanowire materials offer well controlled size in comparison with the “top-down” nanofabricated device structures; that is at or beyond the limits of lithography. Also, the crystalline structure, smooth surfaces and ability to produce radial and axial hetero structures can reduce scattering drastically. This results in higher carrier mobility in comparison with other nano devices of similar size. Finally, the diameter (body thickness) of nanowires can be controlled down to well below 10nm. Therefore, even as the gate length is aggressively scaled, electrical integrity of nanowire based electronics can be sustained. This is a feature that could not be easily achieved in planar MOSFETs.

The silicon body is surrounded with a very thin layer of an oxide, and the oxide is enclosed either by a metal or polysilicon gate. The source is on the left side, whereas the drain is on the right side. With the superiorly enhanced gate controllability, the device can greatly relax the stringent process requirements with more flexible device design, such as relaxed channel doping design and allowably thicker gate dielectric. This device has the benefits of both reducing the short channel effects and improving the sub threshold slope, as well as potentially higher packing densities. The small vertical electric field and the use of silicon nanowire channels in the device reduce the surface and Coulomb’s scattering, and the electronic transport is very much close to the ballistic regime. With better suppression of the short channel effects, the gate length can be scaled down even to a sub 10nm regime.

Silicon Nanowire FETs, unlike planar MOSFETs, have metal source and drain contacts. That is, the source and drain contacts are made from metals instead of degenerately doped semiconductors. Due to this factor, positive Schottky barriers are formed at the metal/semiconductor interface due to the combination of metal work function and Fermi level pinning by surface states. As a result, the device performance is affected by physical contact properties to a large degree. Hence, application of annealing can lead to the formation of essentially ohmic contacts and dramatically increase ON current and the apparent carrier mobility.

Table.1. Values of parameters used in simulations

Gate oxide thickness t_{ox}	2nm
Silicon body thickness t_{si}	10nm
P ⁺ Source doping N_A	$10^{20}/\text{cm}^3$
N ⁺ Drain doping N_D	$10^{20}/\text{cm}^3$
channel length (L)	11nm

2.1 SIMULATION

MuGFET [9] is a simulation tool for nano-scale multi-gate FET structure. MuGFET users can either use PROPHET or PADRE. It provides self-consistent solutions to the Poisson and

drift-diffusion equation. For this work, we adopt a 2D simulator, PADRE, which was developed at Bell Labs by Mark Pinto, R. Kent Smith, and Ashrafal Alam [8]. PADRE is a 2D/3D simulator for electronic devices, such as MOSFETs and Nanowire transistors. It provides many useful plots for engineers and deep understanding of physics. Many options are provided with respect to the numerical methods and semiconductor device physics. It can simulate physical structures of arbitrary geometry—including hetero-structures with arbitrary doping profiles, which can be obtained using analytical functions or directly from multidimensional process simulators such as Prophet. For each electrical bias, PADRE solves a coupled set of partial differential equations (PDEs). A variety of PDE systems are supported which form a hierarchy of accuracy: electrostatic (Poisson equation) drift-diffusion (including carrier continuity equations) energy balance (including carrier temperature) electro thermal (including lattice heating). The equation used in the simulation tool is based on the drift-diffusion theory and provides self-consistent solution to the Poisson Eq.(1) and drift-diffusion equations. The Poisson and drift diffusion equations are,

$$\frac{\partial^2 \phi(x, y)}{\partial x^2} + \frac{\partial^2 \phi(x, y)}{\partial y^2} = \frac{qN_A}{\epsilon} \quad (1)$$

$$J_n = qn(x)\mu_n E(x) + qD_n \frac{dn}{dx} \quad (2)$$

$$J_p = qp(x)\mu_p E(x) + qD_p \frac{dp}{dx} \quad (3)$$

3. RESULTS AND DISCUSSION

In this section, we have presented some of the numerical results of the output characteristics, the effect of oxide layer thickness, silicon body thickness, I_D - V_{GS} characteristics, I_D - V_{DS} characteristics and conductance efficiency of silicon nanowire transistors in the nanometer region. The Fig.2 shows the drain current I_D and drain voltage V_{DS} characteristics for different gate voltages of the Nanowire FET structure. The oxide thickness is 1nm and length of the channel is fixed as 11nm. As the graph indicates, as the gate voltage increases the drain current also rises gradually. Thus the performance of the device can be controlled by the voltage applied at the gate terminal of the device.

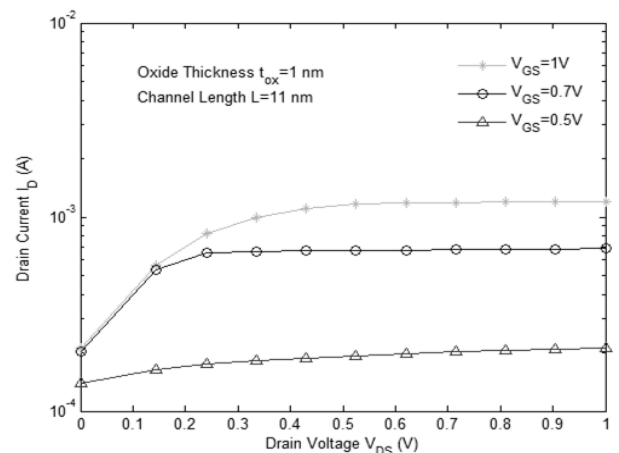


Fig.2. Plot of Drain Current I_{DS} versus Drain Voltage V_{DS} by varying the different gate voltages (V_{GS})

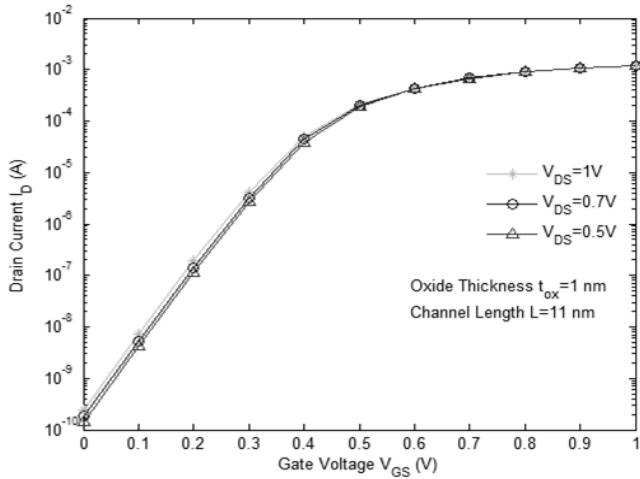


Fig.3. I_{DS} - V_{GS} characteristics of Silicon Nanowire Transistors with Channel length $L = 11\text{nm}$

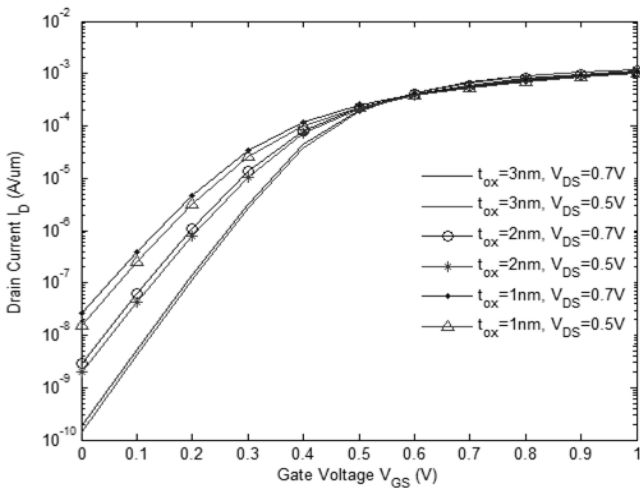


Fig.4. I_{DS} - V_{GS} characteristics of Silicon Nanowire Transistors with various oxide thickness

The Fig.3 shows the transfer characteristics of silicon nanowire FET with different drain voltages 0.5V, 0.7V and 1V respectively. Impact of the drain voltage on the performance of the device is found to be minimum as the graph shows that varying V_{DS} does not change the drain current drastically.

The Fig.4 shows the I_D - V_{GS} characteristics of silicon nanowire FET with various oxide thickness ($t_{ox} = 1\text{nm}$, 2nm and 3nm respectively). From the plot, it is inferred that as the dielectric thickness decreases, the drain current shows an incredible rise and the on current is at maximum.

In Fig.5, the variation of drain current for a fixed Drain bias of 0.5V with various source and drain doping concentration in log scale is presented. One major requirement for the transistor design is the ability to increase and control the carrier concentration, which is normally achieved by doping. When the doping in the Source and Drain is increased, the barrier becomes slightly higher as the Fermi level shifts but also thinner, which leads to a decrease in thermionic emission as well as an increase in the drain current.

The Fig.6 shows the Drain Current I_{DS} versus Gate Voltage V_{GS} by varying the different silicon thickness (t_{Si}). This simple

method for varying the silicon thickness also allows for quantitative measurements of the nanowire FETs drain current efficiency.

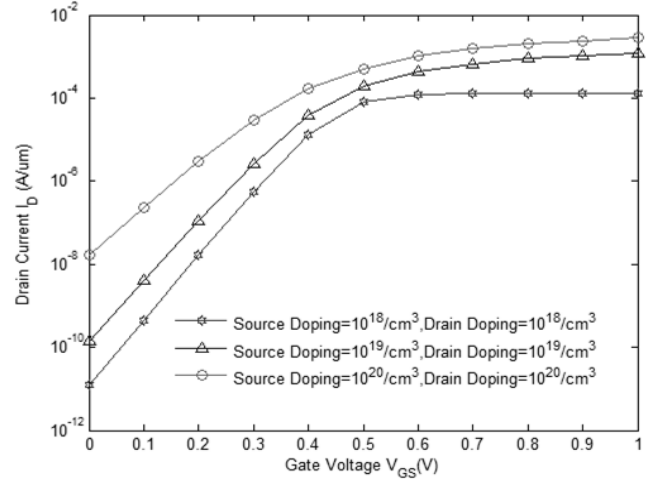


Fig.5. I_{DS} - V_{GS} characteristics of Silicon Nanowire Transistors with various Doping profile

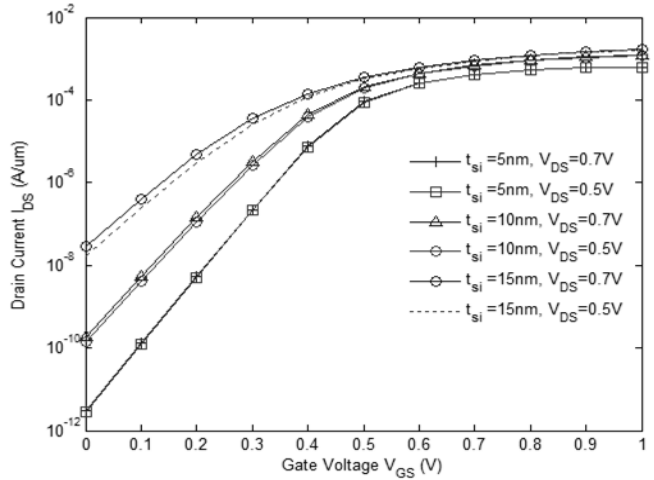


Fig.6. Plot of Drain Current I_{DS} versus Gate Voltage V_{GS} by varying the different silicon thickness (t_{Si})

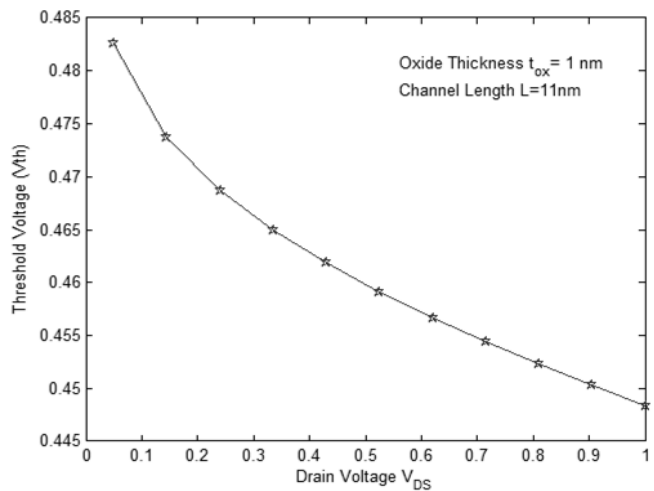


Fig.7. Plot of threshold voltage vs Drain voltage of Silicon nanowire FETs

In Fig.7, the variation of threshold voltage for a fixed channel length of 11nm by varying drain voltage is presented. In wide planar transistors the threshold voltage is essentially independent of the drain voltage and is therefore a well-defined characteristic, however it is less clear in modern nanometer-nanowire FETs.

Furthermore, our simulation results has been compared with 22 nm silicon nanowire transistors [7]. From Fig.3, it is inferred that the I_{ON} current of silicon nanowire transistor is 10^{-4} A ($V_{GS} = 0.5$ V) and the model proposed by Theodore [7] with 22nm silicon nanowire transistor is 10^{-5} A ($V_{GS} = 0.5$ V). From this analysis, it is clear that, the 11nm silicon nanowire transistor has more advantage compare to the other types of devices, in terms of its higher I_{ON} current.

4. CONCLUSION

Due to high fabrication cost of Nanowire FETs, it is desirable to predict their performance by simulation and to improve their design parameters. Simulation results provides insight into the operation of modern semiconductor devices and circuits, and dramatically reduces the fabrication costs and time to- market. This simulation study reveals that the Silicon nanowire transistor is an attractive candidate for CMOS device design for future technology nodes. Nanowire transistors build using Silicon material is providing high I_{ON} current, thus future CMOS devices will be aiming at higher device drive current and faster operation speed. We have presented some of the simulation results of the transfer characteristics, output characteristics, effects of a change in thickness, and conductance efficiency of silicon nanowire transistors in the nanometer region. However, at this time the nanowire transistor still is in its early stage, there is a lot of room to optimize the structure parameters and lots of new phenomenon to be explored by both experimental and computational approach.

REFERENCES

- [1] International Technology Roadmap for Semiconductors, Available at: <http://www.itrs.net>.
- [2] S. Saito, K. Torii, Y. Shimamoto, S. Tsujikawa, H. Hamamura, O. Tonomura, T. Mine, D. Hisamoto, T. Onai, J. Yugami, M. Hiratani, and S. Kimura, "Effects of Remote-Surface-Roughness Scattering on Carrier Mobility in Field-Effect-Transistors with Ultrathin Gate Dielectrics", *Applied Physics Letters*, Vol. 84, pp. 1395-1397, 2004.
- [3] E.B. Ramayya, D. Vasileska, S.M. Goodnick, and I. Knezevic, "Electron Mobility in Silicon Nanowires", *IEEE Transactions on Nanotechnology*, Vol. 6, No. 1, pp. 113-117, 2007.
- [4] S.M. Koo, Li Q, M.D. Edelstein, C.A. Richter and E.M. Vogel, "Enhanced Channel Modulation in Dual-Gated Silicon Nanowire Transistors", *Nano Letters*, Vol. 5, No. 12, pp. 2519-2523, 2005.
- [5] N. Singh, A. Agarwal, L.K. Bera, T.Y. Liow, R. Yang, S.C. Rustagi, C.H. Tung, R. Kumar, G.Q. Lo, N. Balasubramanian, and D.L. Kwong, "High-Performance Fully Depleted Silicon Nanowire (diameter \leq 5nm) Gate-All-Around CMOS Devices", *IEEE Electron Device Letters*, Vol. 27, No. 5, pp. 383-386, 2006.
- [6] N. Balasubramanian, N. Singh, S.C. Rustagi, Kavitha, Ajay Agarwal, Gao Zhiqiang, G.Q. Lo, D.L. Kwong, "Silicon Nanowire Field Effect Devices By Top-Down CMOS Technology", *Proceedings of 65th Annual Device Research*, pp. 47-48, 2007.
- [7] S. Theodore Chandra and N.B. Balamurugan, "Performance Analysis of Silicon Nanowire Transistors Considering Effective Oxide Thickness of High-k Gate Dielectric", *Journal of Semiconductors*, Vol. 35, No. 4, pp. 1-7, 2014.
- [8] Padre, Available at: <https://nanohub.org/resources/padre>, Accessed on 2014.
- [9] MuGFET, Available at: <https://nanohub.org/resources/NANOFINFET>, Accessed on 2014.
- [10] Aryan Afzalian, Matthias Passlack and Yee Chia Yeo, "Atomistic Simulation of Gate-All-Around GaSb/InAs Nanowire TFETs using a Fast Full-Band Mode-Space NEGF Model", *Proceedings of International Symposium on VLSI Technology, Systems and Application*, pp. 1-2, 2016.
- [11] Faraz Najam, Yun Seop Yu, Keun Hwi Cho, Kyoung Hwan Yeo, Dong-Won Kim, Jong Seung Hwang, Sansig Kim and Sung Woo Hwang, "Interface Trap Density of Gate-All-Around Silicon Nanowire Field-Effect Transistors with TiN Gate: Extraction and Compact Model", *IEEE Transactions on Electron Devices*, Vol. 60, No. 8, pp. 2457 -2463, 2013.