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Retraction

Retracted: DESIGN OF LOW POWER VCO ENABLED QUANTIZER IN CONTINUOUS TIME SIGMA DELTA ADC FOR SIGNAL PROCESSING APPLICATION

ICTACT Journal on Microelectronics Retraction Statement:

ICTACT Journal on Microelectronics hereby retracts the article titled "**Design of Low Power VCO Enabled Quantizer in Continuous Time Sigma Delta ADC for Signal Processing Application**," originally published in ICTACT Journal on Microelectronics, Volume 2, Issue 1, pp. 193-197, April 2016, DOI: 10.21917/ijme.2016.0033. This retraction is being issued after careful consideration and investigation by the editorial board.

After thorough examination, it has come to our attention that the same article has been published in multiple journals simultaneously, which is a violation of ethical publishing standards. The duplicate publication undermines the integrity of the scientific literature and violates the policies of ICTACT Journal on Microelectronics.

The editorial board has communicated with the authors regarding this matter. The authors have not responded to correspondence regarding this retraction.

In light of the breach of publishing ethics, the editorial board of ICTACT Journal on Microelectronics has decided to retract the article. The decision to retract has been made in accordance with journal publication Ethics.

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DESIGN OF LOW POWER VCO ENABLED QUANTIZER IN CONTINUOUS TIME SIGMA DELTA ADC FOR SIGNAL PROCESSING APPLICATION

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Abstract

An accurate design of low power Voltage Controlled Oscillator (VCO) enabled quantizer in Continuous Time Sigma Delta ADC in 180nm CMOS technology using Tanner EDA tools is done. The proposed architecture consists of the loop filter, VCO quantizer and the DAC in the feedback side of model. The Operational Amplifier (OPAMP) used in design of loop filters offers 40dB gain, 70 degree phase margin and unity gain bandwidth of 79.06MHz. Even order harmonics of VCO are reduced by VCO quantizer loop structures. The Higher order loop filter is designed using an active Resistance and Capacitive based integrators and VCO quantizer is implemented using 15 multiple stage ring oscillator and register of DFF which provides an added advantage of low phase noise with frequency of 100 KHz rang. Remarkable power dissipation of overall circuit is 3.8 mW.

Keywords:

Analog to Digital Converter (ADC), Operational Amplifier (OPAMP), Nonidealities, Voltage Controlled Oscillator (VCO)

1. INTRODUCTION

Integrated circuit (IC) technology result in many advances and have cover the efficient implementation of digital logic on silicon which moved many types of signal processing to the digital domain. One of the important applications of this phenomenon is in data converters i.e. Digital to Analog converters (DACs),Analog to Digital Converters (ADCs) and Mixed signal community has been actively researching Continuous Time ∑Δ ADC structures. A promising ADC structure called Continuous Time ∑Δ ADC structures has recently become focus of many research activities which provide excellent power efficiency [5]. The major role to perform analog to digital conversion with significantly relaxed matching requirements on analog components.

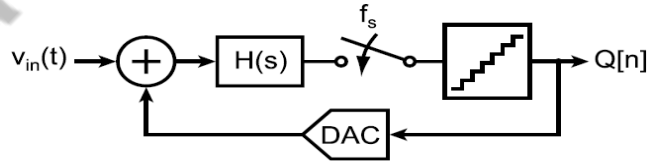
Conventional analog Continuous Time ΣΔ ADC includes a comparator circuit having high speed and low noise in the loop as the quantizer, thus poses a design challenge in deep submicron technology. In deep submicron technology, the design of ADCs become more difficult due to the low supply voltage that comes along the technology scaling and require complex analog buildings blocks [8]. While a Voltage Controlled Oscillator (VCO) based quantization which can be easily realized in a CMOS technology and can be used for high speed application [5].

VCO based quantization has become topic of great interest due to having unique and attractive signal processing features. Several techniques to mitigate distortion caused by the VCO's nonlinear tuning curve have been proposed in recent years. VCO based ADC's using mostly digital circuits which results in technology scaling. Continuous Time ΣΔ ADC are becoming very advance research of implementing ADCs in many of the applications such as radio, wireless receiver, audio, communication etc [6].

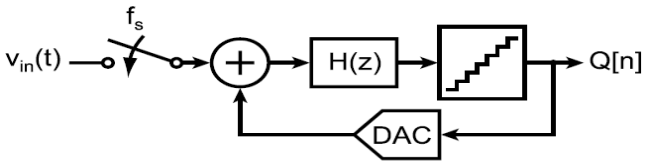
The rest of paper is organized as follows. Section 2 provides the brief about the overview of the VCO based architecture and discuss the importance of various proposed designs. Section 3 presents the basic circuit design and VCO based ADC architectures. Section 4 discussed the proposed VCO based CT ΣΔ ADC topologies. Expected results and outcome of previous proposed work are drawn in Section 5 and conclusion on section 6.

2. A BRIEF OVERVIEW OF CT ΣΔ ADC

The most basic popularity of the CT ΣΔ ADC is from its inherent anti-alias filtering ability. Such ability of filtering is possible as its input analog signal is first applied to CT loop filter before being sampled by the VCO quantizer as shown in Fig.1(a), whereas in DT ΣΔ ADC samples the input analog signal before it applied to loop filter as shown in Fig.1.(b). The same is also true for any other DT ADC (SAR, pipeline, flash, etc) as sampling always occur prior to ADC input.



(a)



(b)

Fig.1. (a). Sampler in CT ΣΔ ADC (b). Sampler in DT ΣΔ ADC

The inherent anti-alias filtering ability of the CT ΣΔ ADC's has also been widely used as a means to simplify baseband filtering and digitization in wireless systems. However a CT ΣΔ ADC could be clocked up to an order of magnitude faster in the same technology without much performance penalty.

Unfortunately designing an anti-alias filter introduces distortion and minimal noise which has the drawback of area consumption and high power dissipation. A recently published CT filters has found that the power dissipation can vary from 10mW to more than 100mW depending on desired noise, linearity and bandwidth. At the same time active filter's area can vary widely from 0.1mm^2 to more than 0.1mm^2, depending on the filter order.

Given the considerable power and area overhead involved in designing of CT ΣΔ ADC as shown in Table.1.

Table.1. Brief survey of recently published CT ΣΔ ADC

Reference	BW(MHz)	Power(mW)	Area(mm^2)
[5]	10	66	-
[6]	10	16	0.36
[9]	20	87	-
[11]	-	20	8.6
[12]	1.1	62	5.76

The survey of the resolution and bandwidth of popular ADC topologies presented as shown in Fig.2. This shows the comparison of different ADC topologies along with its important applications.

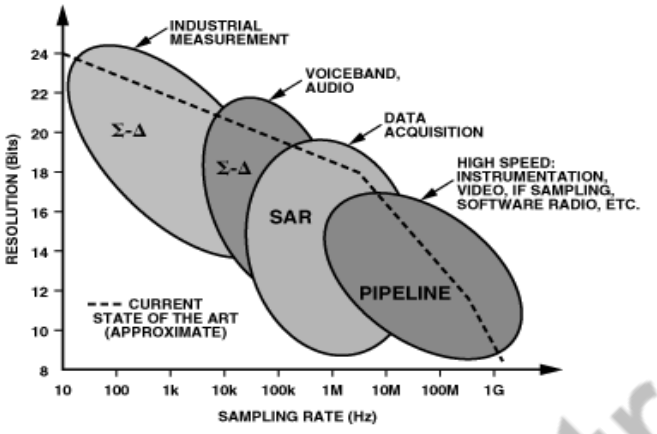


Fig.2. Comparison of ADC Topologies

3. SYSTEM ARCHITECTURES

The architecture of VCO based CT ΣΔ ADC is shown in Fig.3. The ADC consist of loop filter, VCO based quantizer and feedback DAC. Loop filter provides noise shaping and linearity and hence reduces the quantization noise with excellent power efficient characteristics. The VCO converts the analog input voltage into an output frequency and the frequency is a linear function of input voltage. To circumvent the VCO nonlinearity and increase the order of noise shaping, the VCO based ADC is used and thus allowing high speed of operation with small latency.

In the DAC design normally, each phase output is connected to one DAC cell and added together to obtain the feedback signal. The NRZ and RZ DAC are both act as feedback which are connected to VCO quantizer to maintain monotonicity.

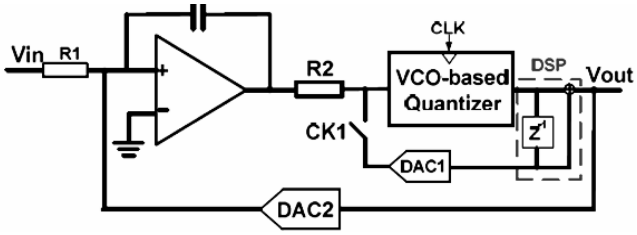


Fig.3. Proposed VCO quantizer based CT ΣΔ ADC

Despite its signal processing advantages, CT ΣΔ ADC's also concerns over the highly architectures sensitivity to clock jitter due to modulation of DAC charge appearing directly at ADC input as shown in Fig.4. The RZ DAC was demonstrated to have far greater jitter sensitivity compared to NRZ DAC due to its modulation more than twice the DAC charge at every sample and hence degrades SNR.

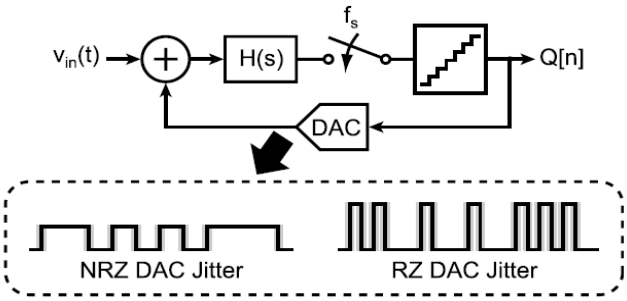


Fig.4. Clock jitters in a 1-bit NRZ and RZ feedback DAC

Recent work has shown that the SNR degradation due to clock jitter can be significantly reduced by pursuing a Multibit quantize rand NRZ feedback DAC implementation [5,10]. The Fig.5 shows that jitter only modulates the DAC charges of the LSB's that change from sample to sample. Increasing the number of DAC bits reduces the error charge it introduces. Thus in these highly digital environment, mixed signal designs of CT ΣΔ ADC will face new challenges as they delivers high resolution, bandwidth and power efficiency in latest and deep sub-micron technologies [3].

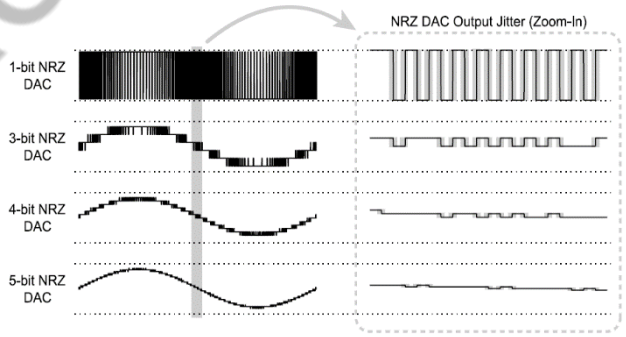


Fig.5. Increasing the number of bits in a Multibit NRZ DAC reduces the error charge modulation

4. PROPOSED CONTINUOUS-TIME ΣΔ ADC TOPOLOGY

Voltage controlled oscillator (VCO) of Analog to digital converter (ADC) has recently become a topic of great interest in a mixed signal community. A prototype VCO quantizer based CT ΣΔ ADC is designed which converts the analog input signal into digital data and hence reduces nonlinearity. The building blocks of loop filter, VCO quantizer and DAC are designed with thick oxide devices operating at 2.5V and 1.8V. The proposed architecture of VCO based CT ΣΔ ADC is shown in Fig.6.

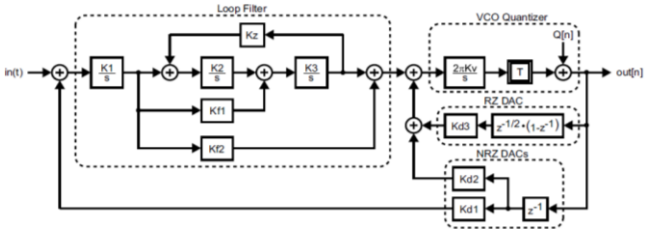


Fig.6. Proposed Loop filter block diagram with VCO quantizer and feedback DAC

4.1 LOOP FILTER

The loop filter of ΣΔ ADC provides the noise-shaping property. Loop filter suppress the VCO nonlinearity to the extent of its gain in the signal bandwidth. Higher order noise shaping can be achieved by increasing the order of loop filter. Here the fourth order loop filter is realized using an active RC integrator as shown in Fig.7.

There are three different types of topology used i.e.

1) Active RC
2) Gm-C
3) MOSFET-C integrator

Active RC integrators have the advantages of better linearity and larger signal swing. Here active RC topology is chosen for its excellent linearity. The amplifier in the integrator is implemented two-stage OPAMP. The first stage is differential stage and the second stage is implemented with the common source. The feed forward path from the input to second stage is implemented as shown in Fig.8.

However the effectiveness of this technique greatly depends on the gain of the loop filter, because VCO quantizer input scans the entire signal range and it exercises the entire nonlinear tuning curve of VCO. As a result, a high gain loop filter is needed to suppress the large amount of distortion introduced by the VCO which causes the ADC performances. The simulated result of two-stage OPAMP with tanner EDA tool with 0.18um CMOS technology is shown in Fig.9. The design requirement of two-stage OPAMP is that the phase margin must be greater than 60^0 in order to perform high stability. The OPAMP achieves a DC gain, phase margin and unity gain bandwidth of 40dB, 70^o and 79.06MHz respectively with power (V_{DD}) 1.8V.

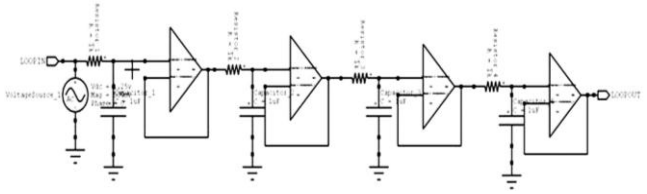


Fig.7. Fourth order loop filter using two stage OPAMP

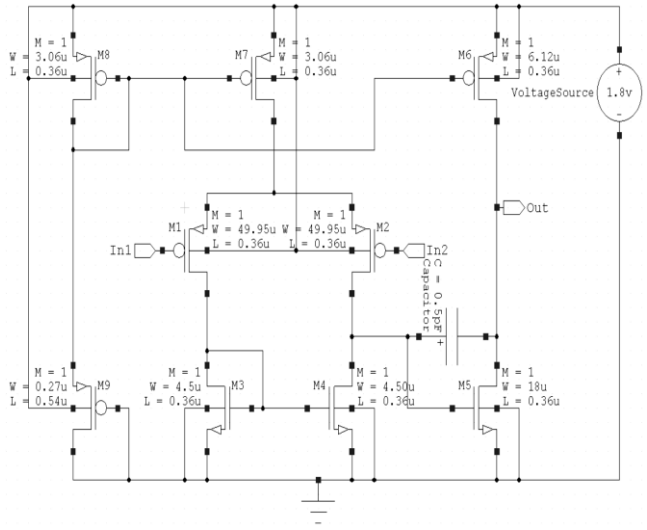


Fig.8. Two stage OPAMP using CMOS Realization

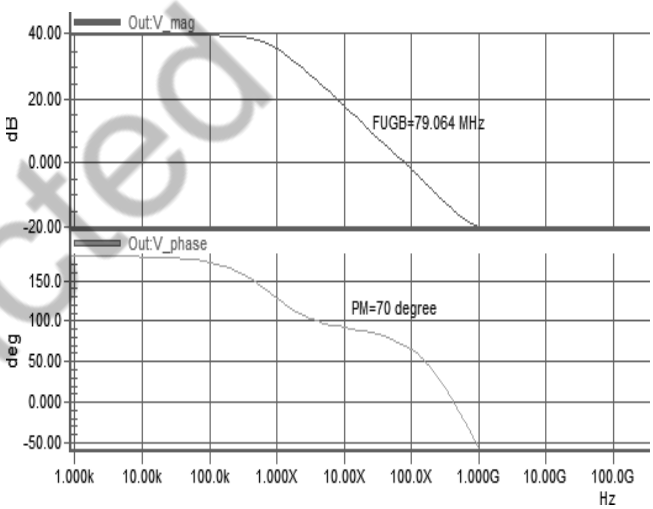


Fig.9. Simulated magnitude and phase response of OPAMP

4.2 VCO QUANTIZER

The time based ADC architecture also called VCO based ADC or VCO based quantizer that converts analog input signal in to digital data. VCO produces a continuous time based signal whose frequency is directly proportional to the average analog input signal. A quantizer that follows the VCO that quantizes the signal on each sampling period and generates the corresponding digital output. Resolution is directly depends on the number of phases of VCO. Hence the drawback of single phase architecture can be rectified by using multiphase VCO based ADC. There are mainly two types of architectures for VCO based ADCs. Counter based architecture and phase detector based architecture. Counter based architecture also facing many issues like reduced noise shaping property due to counter reset issue, high power consumption and area. One method used to avoid counter reset problem is to use 1 bit quantizer instead of counter. The counter is replaced with two D flip flops and an XOR gate, these circuits are enough for performing 1 bit quantization in each phases of VCO.

Generally, a VCO used in VCO-based ADC suffers from high non-linearity, considering that a differential structure could be opted, so that certain non-ideal effects can be inherently reduced.

The control over the frequency of oscillation should be clearly known and the type of control can also vary. However, the VCO should have a wide tuning range in order to have a high resolution VCO-based ADC.

Here the VCO quantizer consists of multistage ring oscillator (RO), two arrays of DFFs and an array of XOR as shown in Fig.10. RO circuits must satisfy some specifications such as area, power, speed and phase noise, posing challenges to circuit and system designers. Also the correct amplitude and low phase noise are two criteria to obtain a suitable performance for VCO in a circuit. The DFFs prevent the previous phase states of VCO. The XOR gate compares these DFFs and determines whether the VCO undergoes a transition. The final output is equal to the number of elements under transition, which control by the control voltage of the VCO. The VCO quantizer is simulated in 0.18um CMOS techniques with the frequency 100 KHz with the input voltage and offset of amplitude 1.25V as shown in Fig.11. The power consumption is 3.8mW.

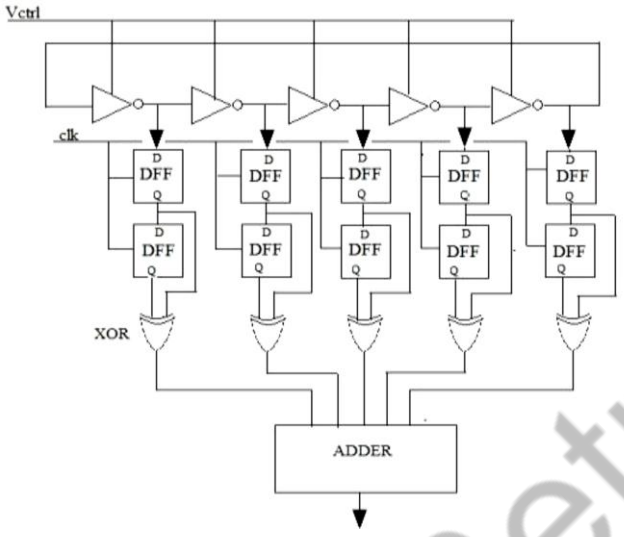


Fig.10. VCO quantizer based on multistage ring oscillator with the arrays of DFFs and XOR

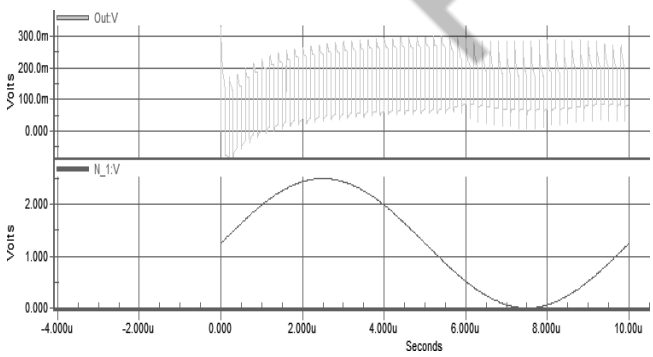


Fig.11. Output of the proposed VCO quantizer

4.3 FEEDBACK DAC

The most important component of feedback path is the 1 bit DAC that converts the output digital streams to analog signal. The main task of DAC is trying to make the digital output of ADC equals to the analog input so the integrator output may result in zero value. A sigma delta convertor uses multi bit quantizer and multibit digital-to-analog (DAC) to reconstruct the analog signal, for such DAC the linearity of the convertor is important. For a high resolution DAC, accuracy is one of the major problems that it encounters, for this a single bit system is used to overcome the accuracy problem. In one bit DAC linearity is determined by the accuracy of switching between the references signals, for high switching accuracy the system will be very linear. The Fig.12 shows the basic schematic structure of one bit DAC with 1.8 supply voltage, the output of one of the invertors is fed as an input of the other inverter, a pulse input is given to the system and get the corresponding analog output, with the low power consumption as shown in Fig.13.

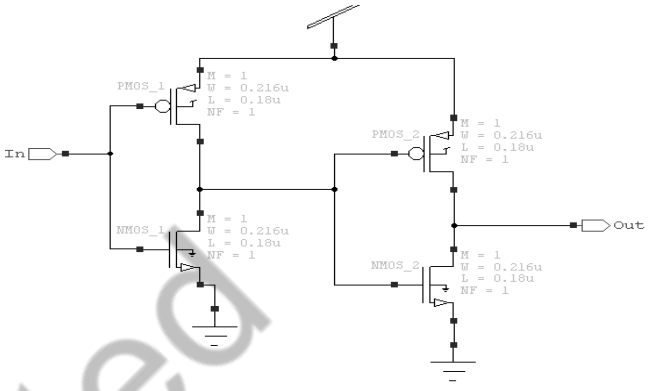


Fig.12. Schematic of DAC

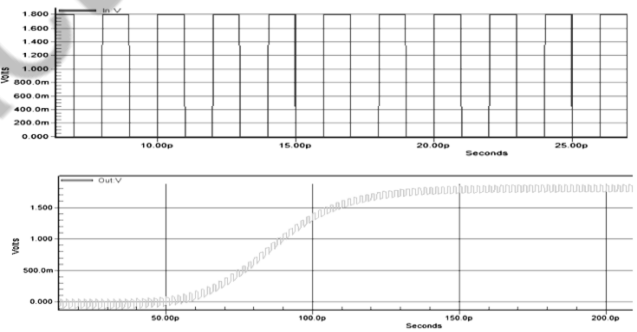


Fig.13. Simulation result of DAC

5. EXPERIMENTAL RESULTS

A Sigma delta Analog to digital Convertor is designed by integrating the components of the system in 0.18μm CMOS technology using Tanner EDA tool. OPAMP which is one of the key components has an open loop gain of 40dB and a phase margin of 70^0, helps in the smooth operation of the integrator circuit. With the help of OPAMP an active RC fourth order loop filter is designed and simulated. Followed by a high speed VCO quantizer is designed using 15-stage Ring oscillator with arrays of DFFs and XOR. Proposed VCO quantizer is implemented at 100 KHz sampling frequency and amplitude of 1.25V with low power dissipation of 3.8mW and hence gives the corresponding result which is then fed to 1 bit Digital to Analog (DAC) circuit at the feedback path of the system. This process is iterated and a pulse of digital signal is achieved at the output of the system. The performance of VCO based architectures is summarized in Table.2 which shows the various comparative results to the previous done works with its line chart shown in Fig.14. We

present a comparison chart between VCO power and different technologies which give quick orientation.

Table.2. Performance summary and comparison with prior works

Ref.	Technology (μm)	Operating frequency of VCO (MHz)	VCO Power (mW)	Gain (dB)	Phase margin (degree)	Supply voltage (V)
[1]	0.18	2.5	-	-	-	1.8
[6]	0.09	0.1-4	1.3	58	55	-
[9]	0.13	225	18	63	55	1.5
[10]	0.13	10	20	50	-	1.2
[11]	0.13	640	20/18	-	-	1.2
This work	0.18	100KHz	3.8	40	70	1.8

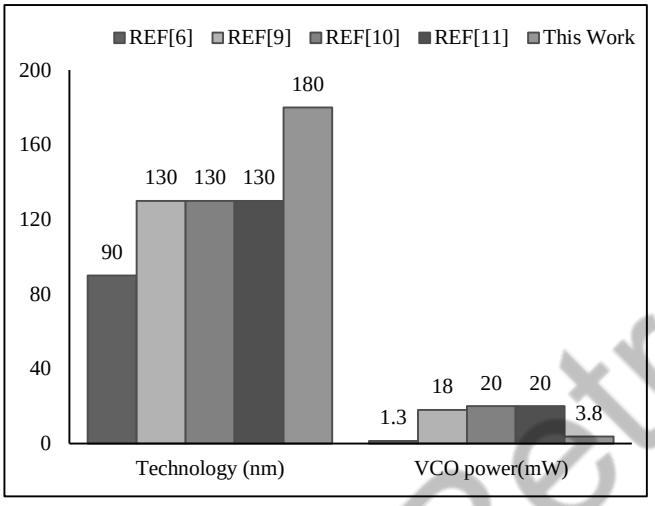


Fig.14. Comparison chart of various results

6. CONCLUSION

It has been observed from above results that high performance low power VCO-based sigma delta ADC architecture is accurately designed in nanometer scale range of the CMOS technology. The amount of distortion which reduced in this approach is by gain of 40dB of the loop filter and hence automatically it improved the VCO nonlinearity. Comparing to the conventional works which focused on high resolution and SNR, above result and discussion shows that the order of noise rejection is highly improved and also enhanced the linearity at 100KHz frequency. Computed power consumption which is 3.8 milliwatts using VCO enabled quantizer in 180nm CMOS technology.

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