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A ROBUST FLIP-FLOP FOR INDUSTRIAL APPLICATIONS

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Abstract

Flip-flops are the basic building blocks of any sequential circuits which occupy the maximum area in a circuit. So the robustness of the system greatly depends on the reliable operation of the flip-flop. In this work the PowerPC 603 flip-flop is simulated and analyzed to measure its reliability against variations in supply voltage and temperature. Performance analysis has been made by having Power, Delay and PDP as Figures of Merit. The acquired simulation results revealed the different sources of power consumption in different scenarios. The simulated results using finer technologies with Synopsys HSPICE prove that PowerPC 603 is a resilient flip-flop for all corners.

Keywords:

PowerPC 603, Flip-Flop, Low Power

1. INTRODUCTION

Large amount of area in any digital system is occupied by memory elements. Flip-flops as serving the purpose of memory elements they are the back-bone of any digital system that we use today. Flip-flops find its applications as memory registers, counters etc. Hence by employing a reliable flip-flop the performance of the system can be improved. Performance of a system or a device is usually outlined in terms of speed or the accuracy in the results. The speed and accuracy depends on the performance of the flip-flop and the number of flip-flops employed respectively. Anyway the most important performance metric of a digital system greatly depends on the type of flip-flop used. When it comes for VLSI, not only speed and accuracy but power also tags with it. Because most of the modern digital equipment used in the industry are running at a remote location and they are powered by a battery source. Hence finding a low power consuming flip-flop attracts great importance today. This work is contributed to identify such a low power consuming flip-flop.

2. LITERATURE REVIEW

As of today an efficient electronic system is said to have low power consumption and sufficient speed. To analyze the speed and power of a system comparatively, Power-Delay Product can be taken as a Figure of merit as mentioned by [1]. Throughout this paper total power consumption is computed as a sum of clock power, data power and latching power [2] i.e. the current drawn from the clock supply and the data signal source and the current offered to the load is taken into account. Latching power implies the output driving capability of the flip-flop. Clock and Data power are the power consumed by the flip-flop from the clock and data supplies respectively. And for the delay measurement usually Clk-Output (Q) time is measured as delay. But this excludes the setup time of the flip-flop input. So in this paper Data (D) – Output (Q) time is measured as delay which includes the setup time margin of the flip-flop [1]. Despite the power and delay measurements the product PDP can serve as a good property to analyze the energy consumed by the flip-flop for the current simulation condition.

As PDP includes the Power and Delay, which implies the power consumed by the flip-flop for a period of time i.e. energy consumption of the flip-flop. PDP measurement enables the designer to select proper operating voltage for the flip-flop at a certain operating conditions.

As stated by [3] the static type of flip-flops are most suitable for the applications where speed is not a concern but power consumption does. In [2], the authors simulated the flip-flops with matured technologies and even though being a static design it had been proven that the PowerPC is robust based on the above said FoMs. It is claimable that dynamic style of flip-flops can be operated at higher speed than the static designs. But they suffer from discharge at the dynamic nodes due to the high reverse leakage current at NP junctions [4]. In [5] the authors proposed a hybrid flip-flop which combines the advantage of static and dynamic design. But the pulsed clock makes it unreliable under low operating voltage conditions. Here the classic PowerPC603 flip-flop used in the RISC processor [6] wins the race between static and dynamic designs. The advantage of PowerPC lies in the low latency direct path and the low keeper structure [7] making it reliable for industrial applications. For industrial applications the flip-flops are expected to operate under more unrealistic operating conditions. At this point the dynamic designs become unsuitable for industrial applications. In this work we made an attempt to prove that PowerPC is still robust in finer technologies with large range of variations in the operating conditions and in all process corners thus saying it suitable for industrial applications where the operating conditions vary in a wide range. For simulations we have used UMC 55nm [9] and SAED 32/28nm [10] technologies.

The paper is organized as follows. Section 3 explains the special qualities of PowerPC-603 flip-flop. Section 4 deals with the performance analysis using UMC 55nm and section 5 deals with the performance analysis using SAED 32/28nm. Section 6 compares the performance of FF in all corners using the above said two technology nodes and discusses Monte-Carlo simulation results. Section 7 presents the conclusions.

3. SPECIAL QUALITIES OF POWERPC 603 FLIP-FLOP

A large number of flip-flops and latches have been proposed in the past few decades. They can be grouped under the static and dynamic design styles. Power PC (Fig.1) - Performance Optimization with Enhanced RISC Performance

Computing is a static type of flip-flop. They dissipate comparatively lower power and have a low clock-to-output (CLK-Q) delay. In a synchronous system, the delay overhead associated with the latching elements is expressed by the data-to-output (D-Q) delay rather than CLK-Q delay. Here, D-Q delay refers to the sum of CLK-Q delay and the setup-time of the flip-flop. But the static designs mentioned earlier lack a low D-Q delay because of their large positive setup time. Also, most of them are susceptible to flow-through resulting from CLK overlap. It has the advantages of having a low-power keeper structure and a low latency direct path. As mentioned earlier, the large D-Q delay resulting from the positive setup time is one of the disadvantages of this design. Despite this shortcoming, static designs still remain as the low power solution when the speed is not a primary concern for e.g. WSNs, applications of IoT etc.

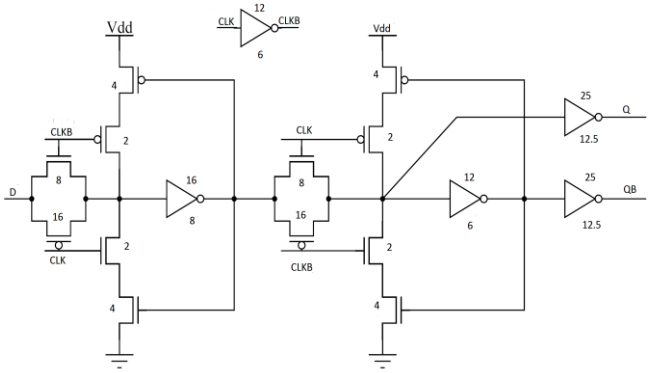

Fig.1. PowerPC 603 flip-flop

This can be operated at moderate speed, but as far as power is concerned Power PC wins the race. Power PC 603 flip-flop does not have any dynamic nodes and also it doesn't precharge the internal nodes which indefinitely cause a surplus amount of power consumption. It has only the clocked transmission gates and inverting buffers and so it consumes lesser power than other structures. As shown in Fig.1 PowerPC FF is one of the simplest FF architecture that occupies lesser layout area.

4. PERFORMANCE ANALYSIS USING UMC 55nm

4.1 ROBUSTNESS AGAINST VARIATIONS IN SUPPLY VOLTAGE

The robustness of PowerPC flip-flop is verified by operating it at various operating voltages ranging from 0.425V to 1V, making it suitable candidate for low power WSNs and IoT processors. The Fig.2 shows a sample output of flip-flop at 1V supply voltage with 500 MHz clock, Fig.3 shows the plot of total power consumption vs. operating voltage. As usual power consumption decreases as the supply voltage is scaled down. It is inferred from Fig.3 that if the flip-flop is operated at low voltage (here 0.425V ~ 0.525V) then it will drive the transistors into sub-threshold region that leads to reduced power consumption with least or negligible degradation in performance. So low power applications such as battery powered applications can employ PowerPC that can operate at sub-threshold region to reduce power consumption.

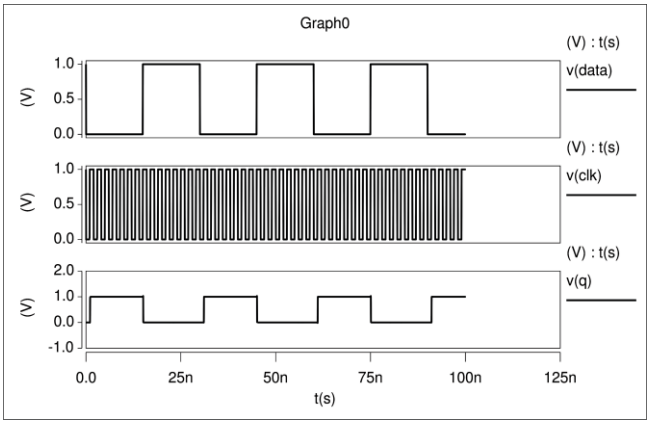

Fig.2. Output of PowerPC 603 flip-flop at VDD = 1V with 500MHz clock

A major constraint in VLSI is that the reduction in supply voltage will cause an increment in delay thus reducing the operating speed and suffer leakage problems. The Fig.4 shows the delay of PowerPC flip-flop against various operating voltages.

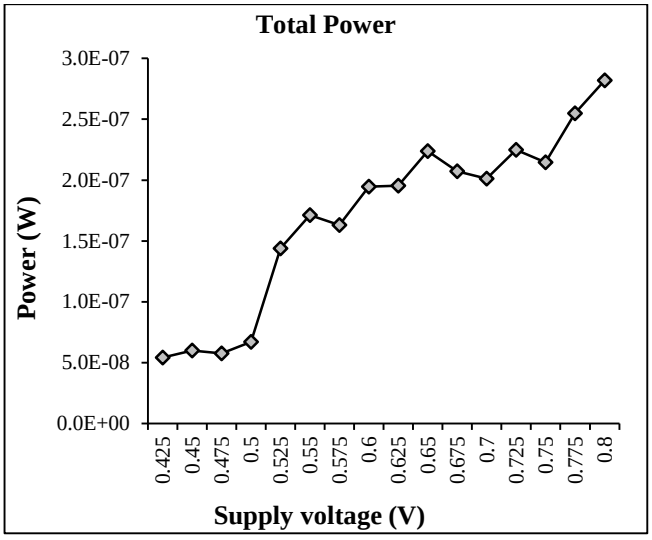

Fig.3. Total Power versus Supply voltage

As it is clearly visible from Fig.4 the delay is high at VDD = 0.425V. Consequently it cannot be employed for high speed circuits. However VDD = 0.425V ~ 0.525V can be a decent tradeoff between power and delay that can be maintained as far as low power is concern. Delay seems to be constant for VDD > 0.675V. So VDD can be directly scaled down to 0.675V that will allow the FF to run at high speed as much as possible. So VDD = 0.525V can be used for applications like remote sensing where a moderate speed with low power consuming circuits are needed. The Fig.5 shows the plot of Power Delay Product variation against operating voltages. From Fig.5, one can say that choosing VDD = 0.5V can be a good solution to applications where speed and power consumption needs to be optimized.

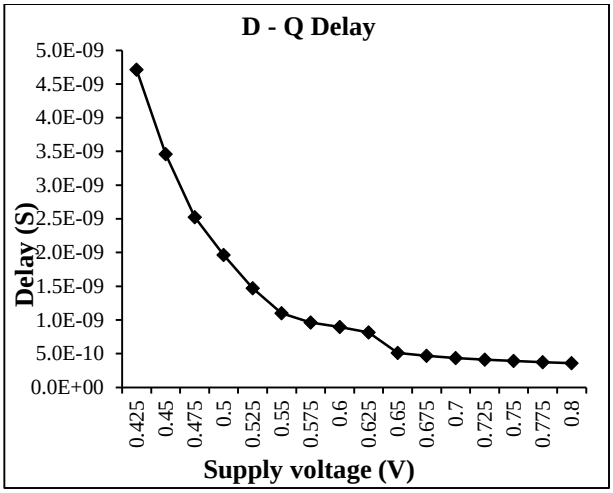

Fig.4. D-Q Delay versus Supply voltage

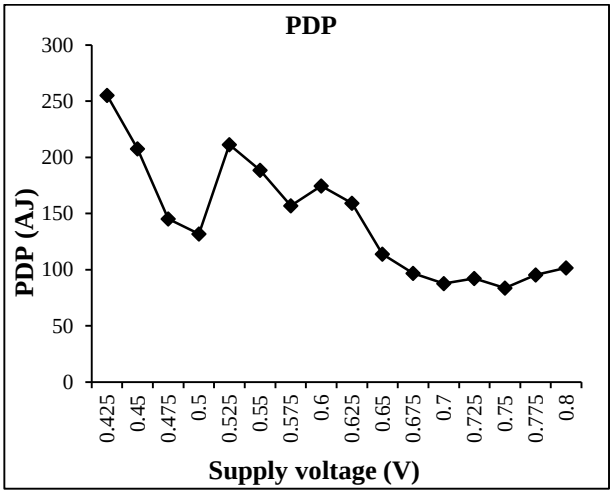

Fig.5. PDP versus Supply voltage at 55nm

5. PERFORMANCE ANALYSIS USING SAED 32/28nm NODE

5.1 ROBUSTNESS AGAINST VARIATIONS IN SUPPLY VOLTAGE

SAED 32/28nm is an Interoperable Process Design Kit designed as a part of Synopsys University program for student's learning purpose. The PowerPC FF is simulated with SAED 32/28nm technology under similar conditions as done earlier for UMC 55nm node. The robustness against variations in supply voltage is analyzed by measuring Total power consumption, delay and PDP. The Fig.6(a), Fig.6(b), Fig.6(c) shows the above said measurements respectively. The Fig.6(a) depicts that Flip-Flop consumes almost equal amount of power even after VDD >> 0.575V. So VDD can be directly scaled down to 0.575V for low power applications. It is predicted that in 32nm node the FF output degrades when VDD is reduced below 0.575V. Since the output degrades it has not been included for the analysis.

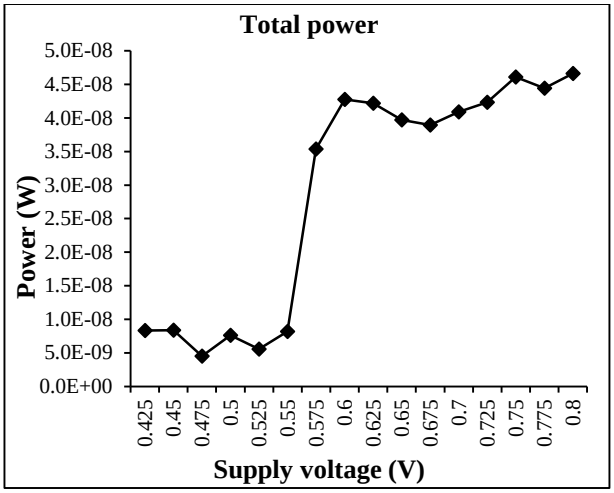

Fig.6(a). Total power vs. supply voltage at 32nm

The Fig.6(b) shows the delay of FF when varying the supply voltage. Similar to Fig.4, the FF exhibits a constant delay for VDD > 0.675V. So even for high speed circuits such as to be used in core processors the supply voltage can be reduced to 0.675V. But further reduction in VDD will increase the delay rapidly as depicted by Fig.6(b).

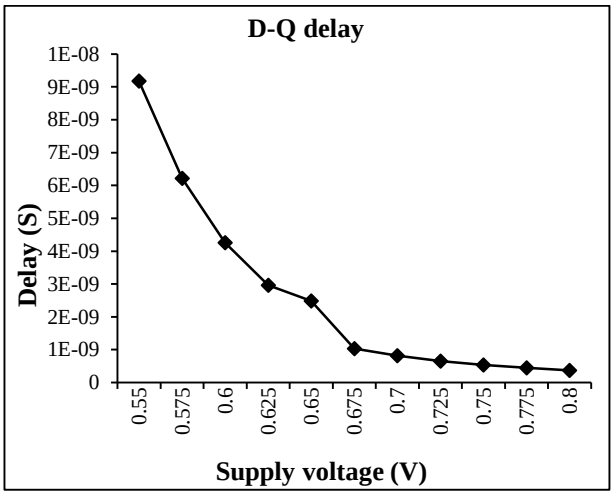

Fig.6(b). D-Q delay vs. supply voltage at 32nm

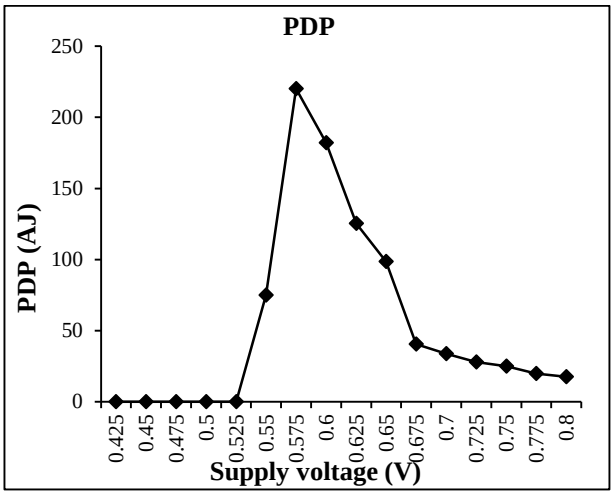

Fig.6(c). PDP vs. supply voltage at 32nm

From Fig.6(c) one can say that choosing VDD = 0.675V can be a good solution for low power as well as high speed circuits. While calculating PDP because of the highest delay at VDD = 0.55V it jumps over the PDP point at VDD = 0.675V. So VDD = 0.55V can be chosen for low power circuits with moderate speed such as WSNs or IoT. The value of PDP below VDD = 0.55V implies that the flip-flop does not produces an acceptable level of output.

6. PDP AT DIFFERENT PROCESS CORNERS FOR 55nm AND 32nm

The devices are shrunk when the technology scales down. This paves way for increased speed of operation even with low supply voltage. This advantage leads to low power high speed circuits. But sometimes this could not be achieved because of process corner variations during manufacturing. Here the FF is simulated using the UMC 55nm and SAED 32/28nm technology libraries in all possible corners to ensure its robustness. When the FF is simulated in TT corner the total power is reduced by 61% when the technology is scaled down from 55nm to 32nm. Similarly the delay is also reduced by 70%.

The Fig.7(a) to Fig.7(e) shows the curve PDP for the flip-flop when simulating it with UMC 55nm and SAED 32nm. The Fig.7(a) shows the variation of PDP in TT section. The flip-flop exhibits a linear variation when the temperature increases. So the designer can predict the change in the power and delay with respect to change in temperature and design the flip-flop according to the operating condition. But in SS corner the PDP varies in an unpredictable manner, which makes the design process complicated. From Fig.7(a) to Fig.7(e), it can be inferred that for all corners except SS corner PDP saturates and remain almost as a constant for extreme high temperature ranges. This implies that for industrial applications where the devices employed at high temperature will have no effect on the process corner variations. So PowerPC flip-flop is suitable for devices used in high temperature areas.

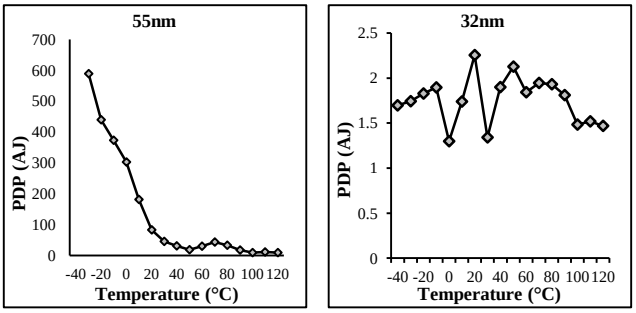

Fig.7(a). PDP at TT Corner

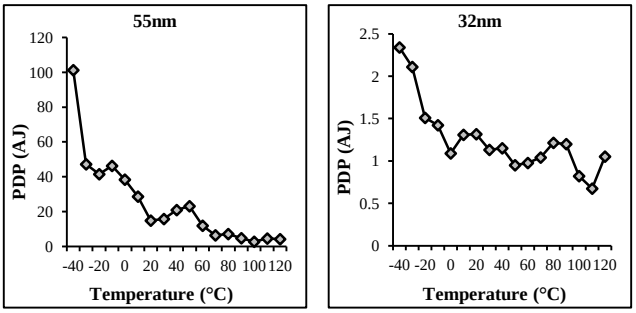

Fig.7(b). PDP at FF Corner

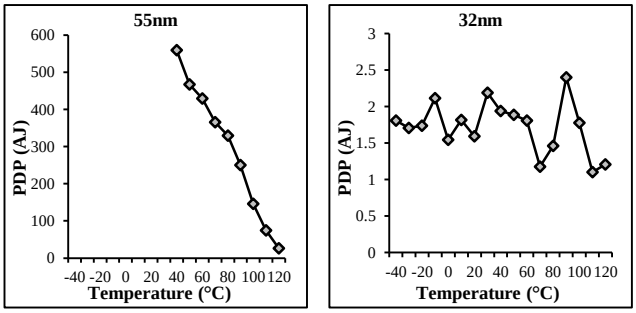

Fig.7(c). PDP at SS Corner

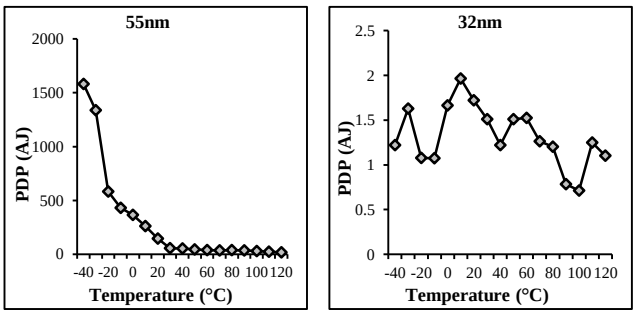

Fig.7(d). PDP at FNSP Corner

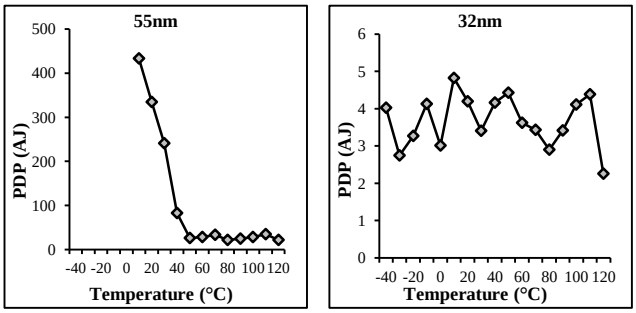

Fig.7(e). PDP at SNFP Corner

For SAED 32nm, the calculated values of PDP do not varies that much. From an overall view it is identified from Fig.7(a) to Fig.7(e) is that the flip-flop exhibits high PDP nearly around the room temperature. And it is inferred that while using SAED 32nm technology node the power consumption and delay becomes independent functions of the process corners.

The Fig.8(a) and Fig.8(b) shows the contribution of power sources to the total power with 55nm and 32nm. Among the three sources viz. data, clock and latching power the main contributing sources are the data power and the clock power. In PowerPC architecture the clock signal needs to drive the stacked devices into saturation or cut off region. This led to increment in clock power consumption. By using low C_g devices the clock power and the data power can be reduced.

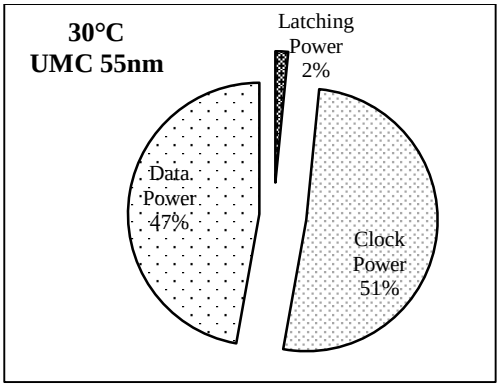

Fig.8(a). Proportion of various power sources contributing total power consumption

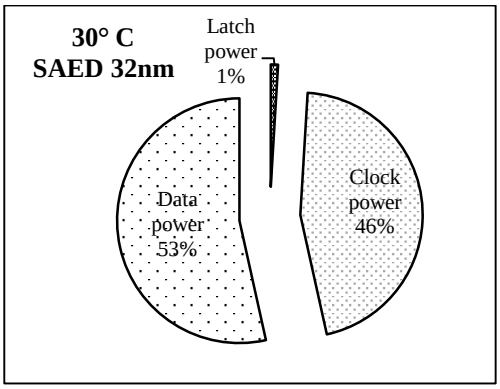

Fig.8(b). Proportion of various power sources constituting total power

Because of the architecture of PowerPC it consumes more power from Clock signal. Clock power can be reduced by incorporating buffers to drive the stacked devices and transmission gates instead of using the clock signal directly. The latching power implies the driving capability of the flip-flop. Obviously it is very small in finer technologies.

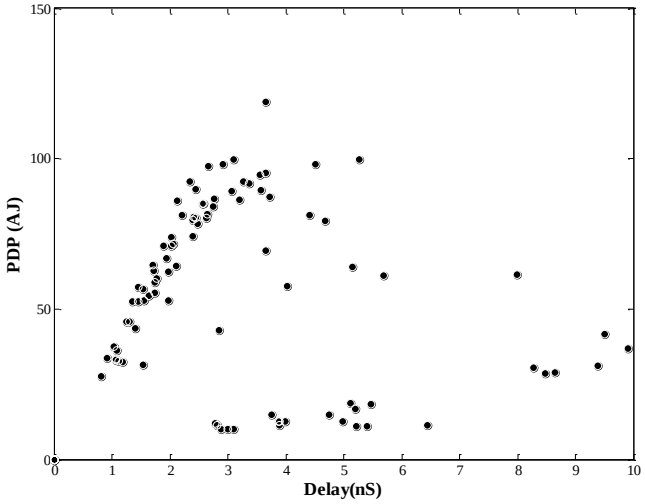

Fig.9. Monte-Carlo simulation result

To further ensure reliable operation of the flip-flop under PVT variations we have simulated the flip-flop using a 100 point Monte-Carlo simulation with ±6σ variation where we have got Mean = 51.256AJ and σ = 27.34AJ The simulation results are shown in Fig.9. The very small deviation shows that flip-flop can serve its purpose even at an extreme range of operating conditions.

7. CONCLUSION

In this paper, the PowerPC Flip-Flop is simulated under extreme conditions ranging from low to high temperatures with all possible corners. The energy consumed by the flip-flop is denoted in terms of PDP. And the result shows that PowerPC sustains almost all the variations. And so it is suitable for industrial applications. By choosing an appropriate PDP value the flip-flop can be made suitable either for low power or for high speed applications. From the PDP plots the position of PDP can be fixed at any point by choosing a proper supply voltage. The simulated results proved that PowerPC is the resilient FF for all corners.

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