ISSN: 0976-9102(ONLINE)
DOI: 10.21917/ijivp.2012.0065

DESIGN AND ANALYSIS OF LOW POWER MULTIPLY AND ACCUMULATE UNIT USING PIXEL PROPERTIES REUSABILITY TECHNIQUE FOR IMAGE PROCESSING SYSTEMS

M. Madheswaran[1] and S. Saravanan[2]

Centre for Advanced Research, Department of Electronics and Communication Engineering, Muthayammal Engineering College, India

E-mail: [1]madheswaran.dr@gmail.com and [2]saravanan.nivi@gmail.com

Abstract

The design of low power high performance Multiply and Accumulate (MAC) unit is presented in this paper. The power analysis for MAC unit is carried out for image filtering application exploiting insignificant bits in pixel values. The developed technique is found to reduce dynamic power consumption by analyzing the bit patterns in the input data which reduces the switching activities. The power consumption of the developed multiplier is compared with existing multiplier techniques and found that is performs better. It is observed from the simulation using SYNOPSIS EDA tool that the proposed pixel properties reusability technique saves power up to 88% with small area over head when used in MAC unit.

Keywords:

Low Power, VLSI Design, Booth Multiplier, MAC

1. INTRODUCTION

The growing popularity of portable and multimedia devices such as video phones and note books has motivated the research to design low power VLSI circuits in the recent past. The real time implementation of image processing system is expected to consume high computational power and has high data throughput rate which limits the use of general purpose processors [1]. Moreover Application Specific Integrated Circuits (ASICs) rely on efficient implementation of various arithmetic circuits for executing the specified algorithms. It is well known that if the density of transistor increases, the complexity of arithmetic circuits also increases and consumes more power. This has further motivated the design of low power VLSI circuits with new concepts. It is also clear that the reduction in power consumption and enhancement in the circuit design are expected to pose challenges in implementation of wireless multimedia and digital image processing systems where multiplication and multiplication-accumulation are the key computations. In the recent past, the researchers proposed various design methodologies on dynamic power reduction by minimizing the switching activities [2].

Choi et al [3] have proposed Partially Guarded Computation (PGC) which divides the arithmetic units into two parts and turns off the unused part to minimize the power consumption. It was reported that the PGC can reduce the power consumption by 10% to 44%. Later, Chen et al [4] have presented a multiplier using the Dynamic Range Determination (DRD) unit to select the input operand with a smaller effective dynamic range that yield the Booth codes to reduce 30% power dissipation compared to conventional method. Later, Tsoi and Leong [5] have presented a module generator for producing near-optimal parallel multipliers in a technology independent manner. The process of multiplication has broken into a partial product generator and a partial product summer. Chen and Chu [6] have reported that the spurious power suppression technique can be applied on both compression tree and modified Booth decoder to enlarge the power reduction. The combination of the signal flow optimization, left-to-right leapfrog structure and upper/lower split structure was incorporated in the design to optimize the array multipliers by Huang and Ercegovac [7]. It was reported that the new approach can save around 20% power dissipation and Pieper et al [8] presented a dedicated block for radix-16 and radix-256 multiplication. These blocks were used as basic components of the structure of the 2's complement radix-2^m array multiplier.

The design of low voltage micropower asynchronous signed multiplier was demonstrated by Gwee et al [9]. The emphases of the design were reduction in power and area. Sung et al [10] have presented a power-aware signed digital multiplier by taking the advantage of a 2-dimentional bypassing method for Fast Fourier Transform (FFT) and Inverse Fast Fourier Transform (IFFT). This multiplier is carried out by Baugh-Wooley algorithm using novel 2-dimentional bypassing cells. Veeramachaneni et al [13] have presented a novel architecture for high speed, low power 3-2, 4-2 and 5-2 compressors capable of operating at ultra-low voltages. The emphasis on the use of multiplexers in arithmetic circuits resulted in high speed and efficient design. Rouholamini et al [14] have implemented a 7:2 compressor based on conventional architecture and delay is reduced by one XOR compared to the conventional design. Yeh and Jen [15] have presented a design methodology for high speed Booth encoded parallel multiplier and reported that the generated partial products showed the improved performance. Wang et al [16] have recommended an improved Modified Booth Encoder (MBE) multiplier design to reduce and rearrange partial products. This has reduced the gate count and improved the performance of the multiplier. Chong et al [17] have described the design of micropower 16x16-bit multiplier for low voltage and low speed applications including hearing aids.

Chen et al [18] have proposed an efficient spurious power suppression technique and applied on transform coding design for H.264 compression technique. It was shown that the spurious power can be reduced. The Spurious Power Suppression Technique (SPST) using AND gates in the detection logic has been used to develop the multiplier and reported by Chen and Chu [19]. The performance of the design for various bit-width input data has been investigated. The Multiply Accumulate (MAC) unit has been one of the essential building blocks used in digital signal processing applications [20-21]. Due to the high capacitive load and large bit width, these MAC structures become the most energy consuming units in modern digital

signal processors [22]. Later more initiatives have been taken to reduce the power consumption of the multiply and accumulate unit [23]. Wang et al have presented [24] a fixed-width multiplier using left-to-right algorithm for partial-product reduction. The high speed feature offered by this design is used to trade for low power. In one design, the proposed multiplier not only owns 8% speed improvement but also gains 14% power and 13% area reduction.

A high-performance and low-power 32-bit multiply accumulate unit was described by Liao and Robert [25]. The fast mixed-length encoding scheme, one-cycle throughput for 16-bit by 16-bit and 32-bit by 16-bit MAC instructions was achieved at very high frequencies. Later, Lee [26] presented a low-power power-aware scalable pipelined Booth multiplier that makes use of the sharing common functional unit, ensemble of optimized Wallace-trees and a 4-bit array-based adder-tree for DSP applications. Hsu et al [27] have described a 16x16 bit single-cycle 2's complement multiplier with a reconfigurable PLA control block fabricated in 90-nm dual-Vt CMOS technology, operating at 1 GHz. The SPST using AND gates in the detection logic has been used to developed multiplier and reported by Chen and Chu [6]. The performance of the design under the conditions of different bit-width input data has been investigated. From the results it is clear that the design have equivalent low power performance and higher speed compared with the former SPST approach.

Keeping the above facts, the efficient algorithm has been developed to improve the performance of the multiplier unit. The developed design reduces the number of switching activities of the MAC and hence reduces the power consumption. The developed multiplier has been used to design a MAC unit with developed pixel property reusability technique. The performance analysis of the multiplier and MAC unit has been presented.

2. DEVELOPED LOW POWER MULTIPLIER

The power consumption of a digital multiplier is reduced by minimize the number of unnecessary switching activities. The reduction in number of partial products of a multiplier can reduce the switching activities. In this paper a new technique to reduce the number of partial product of a multiplier has been presented.

2.1 DEVELOPED ENCODING RULE

In the developed encoding technique, the reduction in partial products is considered to reduce the switching activity and power consumption. The operation can be defined according to the number of 1's and its position in the multiplier. The developed encoding rule is demonstrated and provided in Fig.1. $X = \{X_{n-1}, X_{n-2},\ldots X_0\}$ is multiplier, $Y = \{Y_{n-1}, Y_{n-2},\ldots Y_0\}$ is multiplicand and PP is partial product. The bit representations of the multiplier, multiplicand and partial product are $\{X_i, i = n–1\ldots 0\}$, $\{Y_i, i = n–1\ldots 0\}$ and $\{PP_i, i = n–1 \ldots 0\}$. The length of bit representation is mentioned as n. The operation of developed encoding rule is stated in Table.1 with details of operation.

Table.1. Developed encoding scheme

<table>
<tr><th>Number of 1's in the Multiplier</th><th>Encoding type</th><th>Position of the 1</th><th>Category</th><th>Operation</th></tr>
<tr><td rowspan="2">1</td><td rowspan="2">Eight bit encoding</td><td>x_0</td><td>A</td><td>Add 0 to multiplicand Y,
$PP_i = 0 + Y$, Product=PP_i</td></tr>
<tr><td>x_i</td><td>B</td><td>Shift Y left by i-1 and add 0
PP_i={< < Y by (i-1)}, $PP_{i+1}=PP_i+0$
Product= PP_{i+1}</td></tr>
<tr><td rowspan="2">2</td><td rowspan="2">Eight bit encoding</td><td>x_0 and x_i</td><td>C</td><td>Shift Y left by i-1 and add Y
PP_i={< < Y by (i-1)}, $PP_{i+1}=PP_i+Y$
Product= PP_{i+1}</td></tr>
<tr><td>x_i and x_{i+j}</td><td>D</td><td>Shift Y left by j, add Y and shift the result left by i-1, PP_i={< < Y by (j)}+Y,
PP_{i+1}={< < PP_i by (i-1)}
Product= PP_{i+1}</td></tr>
<tr><td>3</td><td>Eight bit encoding</td><td>x_i , x_j and x_k</td><td>E</td><td>Shift Y by k-j, add Y and shift the result left by j-i, add Y and shift the result left by i
PP_i={< < Y by (k-j)}+Y
PP_{i+1}={< < PP_i by (j-i)}+Y
PP_{i+2}={<< PP_{i+1} by (i)}, Product= PP_{i+2}</td></tr>
<tr><td>More than 3</td><td>Three bit encoding</td><td colspan="4">Introduce a 0 at LSB of the multiplier data and split the multiplier data in to 3 bits as x_{i+1}, x_i, x_{i-1}. Develop the partial products as per the following conditions.
<table>
<tr><th>x_{i+1}</th><th>x_i</th><th>x_{i-1}</th><th>Operation on multiplicand</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>Add 0 to partial product</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>Add multiplicand to partial product</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>Add multiplicand to partial product</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>Shift multiplicand left by 1 bit and add to partial product</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>2's complement of multiplicand, shift left by 1 bit and add to partial product</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>2's complement of multiplicand and add to partial product</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>2's complement of multiplicand and add to partial product</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>Add 0 to partial product</td></tr>
</table></td></tr>
</table>

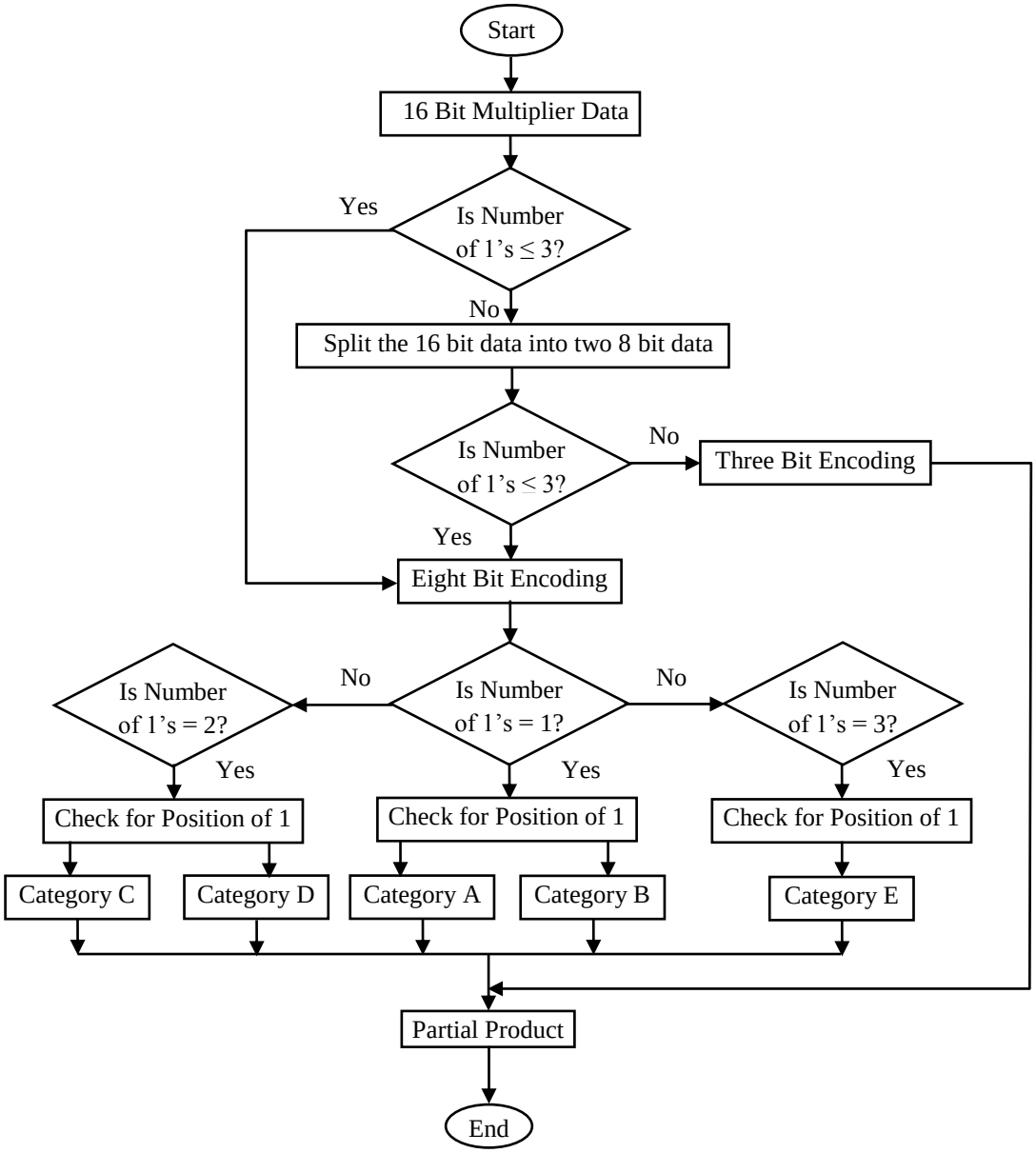

Fig.1. Flow chart of the developed multiplier

If the number of 1's in the 16 bit multiplier data is more than three then the 16 bit multiplier data is splitted in to 8 bit data. If the number of 1's in the 8 bit multiplier is less than or equal to 3, the control goes to eight bit encoding technique. Otherwise the control goes to three bit encoding technique. If the number of 1's in the multiplier is one and depends upon its position, the control goes to execute the operation in category A or B. If the number of 1's in the multiplier is two and depends upon its position, the control goes to execute the operation in category C or D. Otherwise the number of 1's in the multiplier is three and depends upon its position, the control goes to execute the operation in category E. The developed eight bit encoding multiplication technique is explained with the example shown in Fig.2.

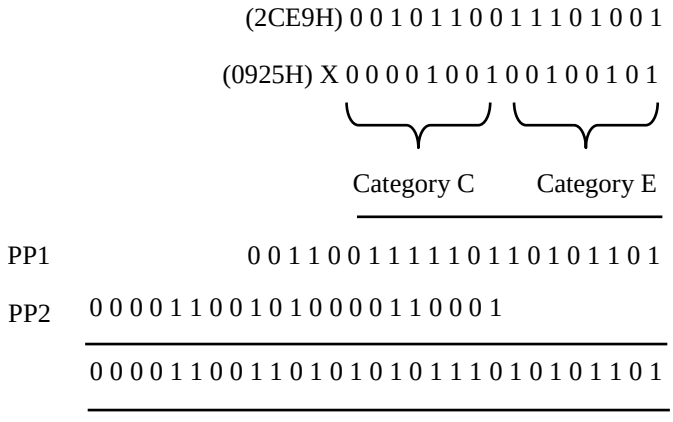

Fig.2. Demonstration of developed multiplier

In Fig.2, the number of ones in the multiplier data is five which is more than three, so the multiplier data is splitted into two parts.

Now LSP multiplier data consists of three ones and MSP multiplier data consists of two ones. According to the developed encoding scheme LSP coming under category E and MSP coming under category C. The above multiplication process completed with only two partial products by the developed encoding scheme. For the above multiplication, array multiplication scheme needs 16 partial products and 15 addition operations; Booth multiplication needs 8 partial products and 7 addition operation. But the developed multiplication scheme needs only two partial product and 4 addition operations.

2.2 BLOCK DIAGRAM OF DEVELOPED LOW POWER MULTIPLIER

The block diagram of the developed hybrid encoded low power multiplier is shown in Fig.3.

The process of the low power multiplier is divided into encoder selection, partial product generation and partial product compression. The multiplier and the multiplicand are stored in register M1 and M2, the number of 1's in the multiplier is checked by the bit checker. Based on the number of 1's the encoder selector selects either eight bit encoder or three bit encoder. A clock gating circuit is used to avoid the simultaneous operation of the two encoders. In the partial product compression the partial products are compressed using 4:2 compressor and a 2-dimentional bypassing method is used. The 4:2 compressor shown in Fig.4 is considered for simulation.

The 2-dimensional bypassing cells skip the multiplier for unwanted signal transitions and computations when the horizontal partial product or the vertical operand was zero. This is done by freezing the adder while the above condition occurs. This is expected to reduce the switching activity and hence power consumption. The final carry propagate hybrid adder is an important one for determining the performance of the multiplication block. A column bypassing provision is provided at the final adder tree to avoid the unwanted addition operation. The dynamic-range determination unit was used to detect the dynamic operand range of the input data and the multiplier with a column-based adder tree of compressors was designed. The detection logic circuit is used to detect the effective data range. If the part of the input data does not make any impact in the final computing results then the data controlling circuit freezes that portion to avoid unnecessary switching transitions. A glue circuit controls the carry and sign extension unit which manage the sign bit.

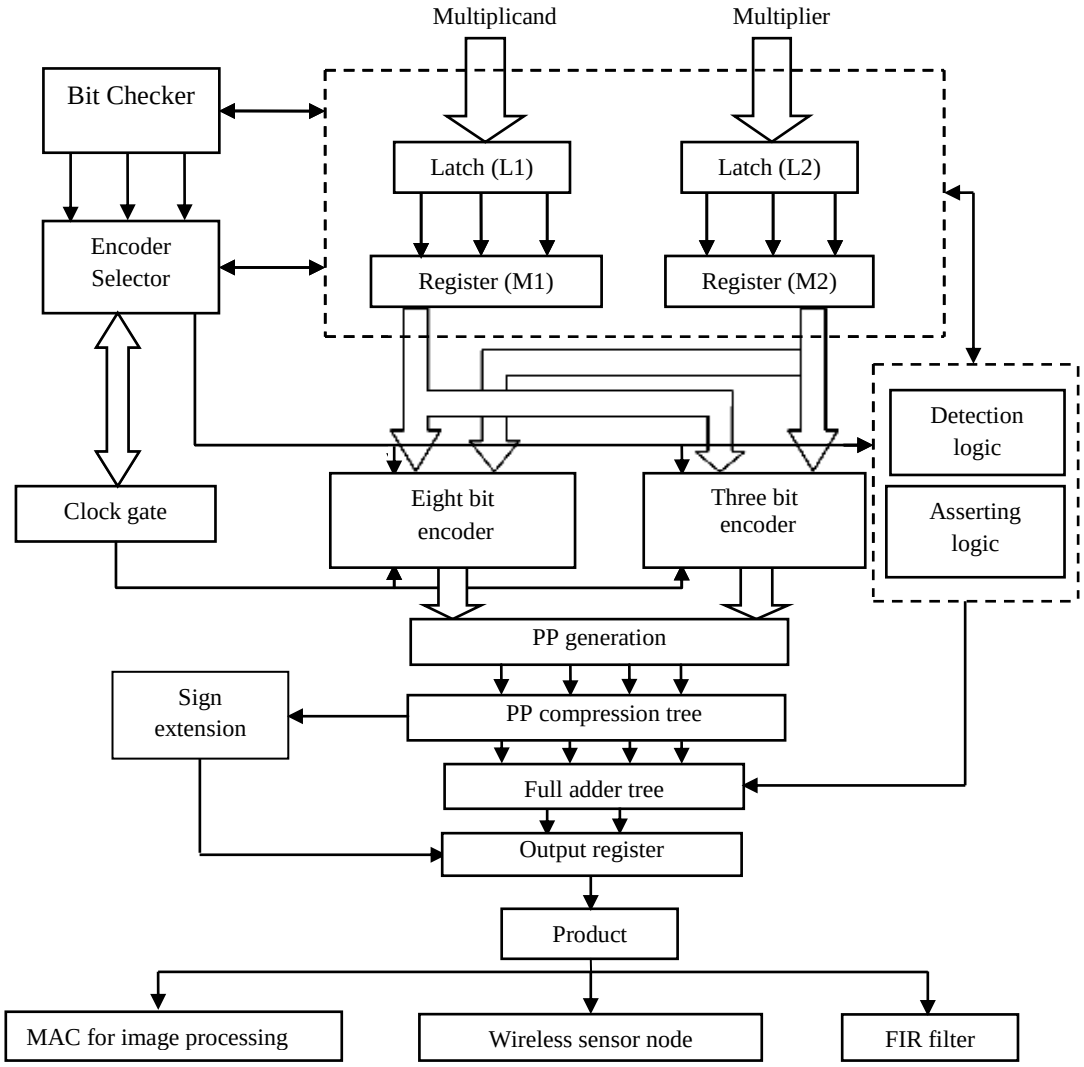

Fig.3. Block diagram of developed multiplier

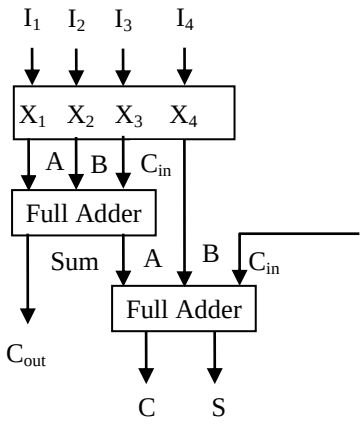

Fig.4. The structure of 4:2 compressor

3. PROPOSED POWER CONSUMPTION REDUCTION TECHNIQUE FOR MAC

The architecture of MAC with power consumption reduction technique is shown in Fig.5. The major unit of the low power MAC is control unit which generates control signals to the low power multiplier and adder according to the special conditions. MAC unit is mainly essential for kernel based process which requires a large number of repetitive computational operations on a fixed window. The repetitive operations can be performed using parallel processing concept which is expected to reduce the complexity and improve the performance. Images in the video sequences are generally processed in raster scan method hence neighboring pixels usually have the same values or very small deviations.

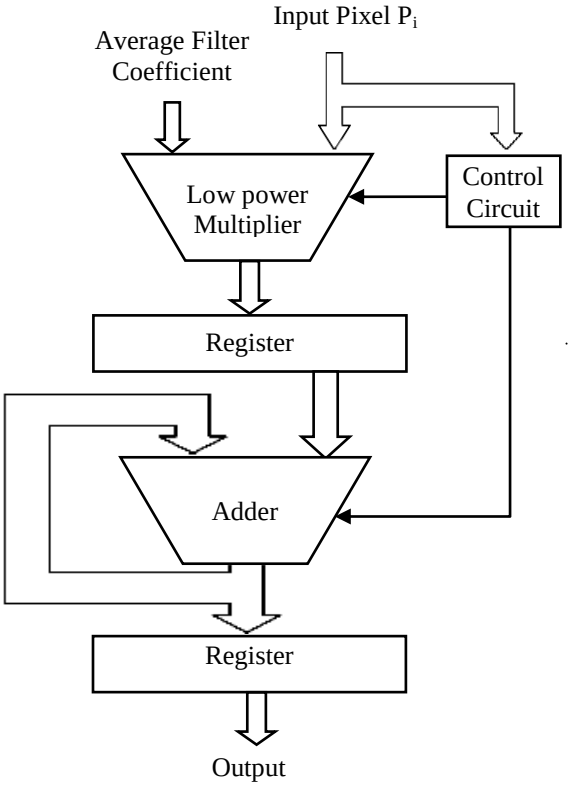

Fig.5. Architecture of low power MAC unit

It can be seen that some of the pixels are having the same value and some with the difference only in least significant part. This characteristic can be exploited to reduce switching activity in the design of arithmetic units. In this research work, the power consumption of the MAC unit is reduced using the pixel reusability technique. This technique suppresses the unwanted operation of the adder and multiplier unit to reduce the power consumption. If the most significant part or least significant part is zero, the design can be done by bypassing some operations in MAC unit to reduce the switching activities. If the condition is detected, appropriate control sequence is developed to disable the parts or all data paths in the architecture. The consecutive MAC operations for two pixels will reduce switching activities by performing the following design conditions shown in Fig.6.

If the pixel values of two consecutive MAC operations are same, the developed design disables the multiplier and reuses previous result at the output. If the current pixel value is 0, it avoids the operation of both hybrid encoded low power multiplier and adder and reuse the previous result of the accumulator. During the process, if part of the input is found to be zero, freeze those multiplier paths to reduce switching power.

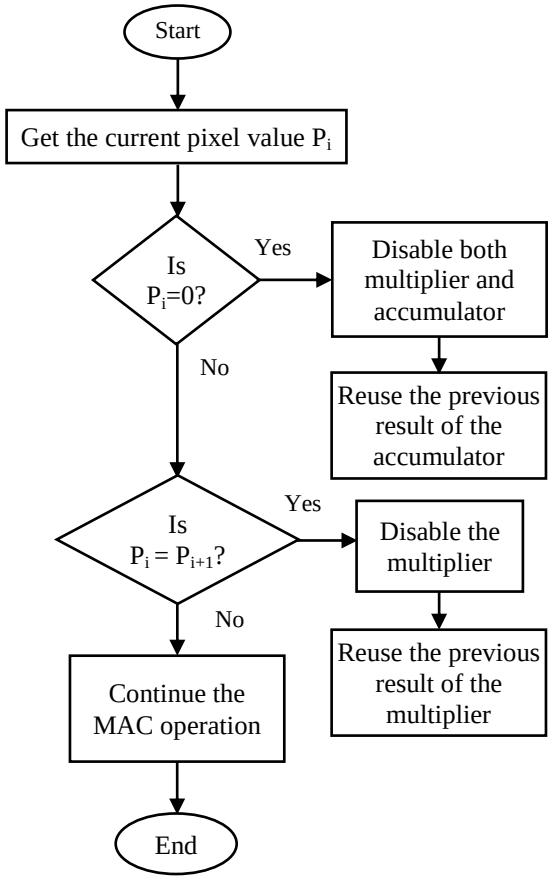

Fig.6. Flow chart of the power consumption reduction technique

4. RESULT AND DISCUSSIONS

4.1 PERFORMANCE ANALYSIS OF PROPOSED MULTIPLIER

The design of low power multiplier and MAC are realized by ASIC design flow with an in-house 120nm TSMC technology

file. Fig.7 shows the snapshot of proposed multiplier power report.

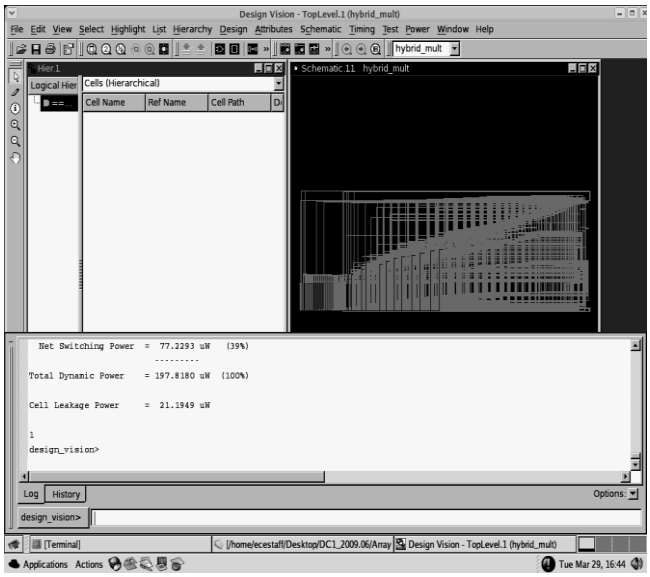

Fig.7. Snapshot of proposed multiplier power report

The designs are verified via C/Matlab behavioral simulation, VERILOG gate level simulation, SYNOPSYS VCS simulation and SYNOPSYS DC logic synthesis. The tool window shows the power consumption of the developed multiplier. The performance comparison of the proposed multiplier with some existing design is listed in Table.2.

Table.2. Power analysis of various multipliers

Design	Feature	Technology	Power (mw)	Area
Huang [7]	(1) 32bx32b	0.18µm	19.65 for Djpeg	74598 (tr.)
Liao [25]	Coprocessor SIMD 32b MAC	0.18µm	900@1.6V,800_MHz	NA
Wang [24]	32bx32b Fixed-width	0.35µm	79.86	19743 (gate)
Chen [4]	(1) 16bx16b	0.25µm	17.30 for normal distribution inputs	0.337 (mm^2)
Lee [26]	Scalable length of 4b, 8b, 16b	0.13µm	1.04@ 100MHz for random data	6388 (gate)
Hsu [27]	(1)16bx16b (2) Sleep mode (3) Dual V_t	90nm	9@1.3V 1GHz (2) $7.9x10^{-2}$ @50MHz, 0.57V	0.03 (mm^2)
Chen[19]	(1)16bx16b (2) SPST	0.18µm	(1) 1.21@ 100MHz , 1.8V for H.264 Texture coding (2) 2.82 @100MHz, 1.8V for normal distribution inputs	11028 (tr.)
Proposed	16bx16b	120nm	0.197 @ 100MHz	5228 (nm^2)

From the comparison table it is clear that the proposed multiplier consumes less power than the other design. The performance analysis of multipliers belongs to category A to category E is listed in Table.3.

Table.3 provides the power consumption of various multipliers for both control logic and total logic. The power consumption of the multiplier for the specific input data X and Y coming under various categories are shown in the Table.3. From the results it is clear that the developed multiplier consumes less power compared to array and Booth multiplier for all categories.

Table.3. Power analysis of various multipliers

Input (Category)	Array Multiplier Power (µw)		Booth Multiplier Power (µw)		Developed Multiplier Power (µw)	
	Control logic	Total logic	Control logic	Total logic	Control logic	Total logic
X=01000001 Y=00000001 (Category A)	3.94	91.38	0.24	1.24	0.10	0.33
X=01000001 Y=00000010 (Category B)	3.94	91.38	4.25	7.83	0.33	1.89
X=01000001 Y=00100001 (Category C)	3.94	91.38	3.81	10.61	3.42	7.38
X=01000001 Y=00100010 (Category D)	3.94	91.38	4.25	17.23	3.13	8.30
X=01000001 Y=01100010 (Category E)	3.94	91.38	3.81	17.54	0.93	7.65

4.2 PERFORMANCE ANALYSIS OF PROPOSED MAC FOR AVERAGING FILTER

The power analysis of the developed MAC unit is demonstrated with an example of image filtering (average filter) application having the filter size of 3x3 and input pixel size of 128x128. The 3x3 average filter window is shown in Fig.8. A 128X128 image has been taken as input for the average filtering action and the pixel values are shown in Fig.9.

1/9	1/9	1/9
1/9	1/9	1/9
1/9	1/9	1/9

Fig.8. Window of a 3x3 average filter

The pixel values of the filtered image have been obtained by Eq.(1),

$$H(x,y) = \sum_{j=1}^{height} \sum_{i=1}^{width} I(i,j)M(x-i,y-j) \qquad (1)$$

H(x,y) denotes output image, I(i,j) be the input image and M is the average filter.

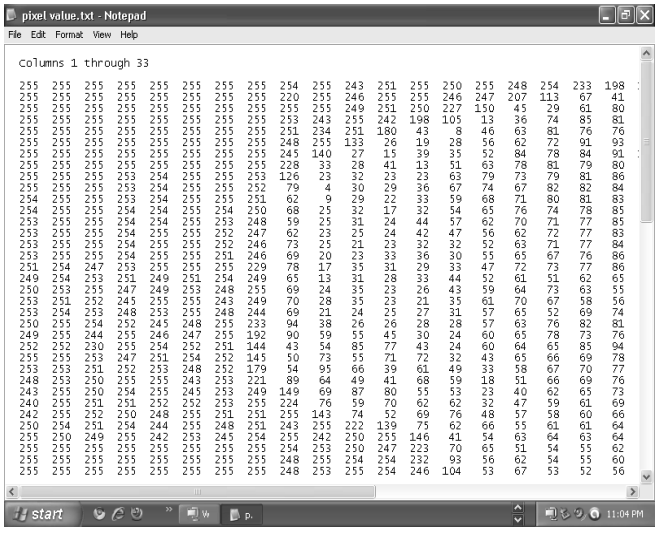

Fig.9. Pixel value matrix of input image

The pixel values of position X_iY_i, X_iY_{i+1}, X_iY_{i+2}, $X_{i+1}Y_i$, $X_{i+1}Y_{i+1}$, $X_{i+1}Y_{i+2}$, $X_{i+2}Y_i$, $X_{i+2}Y_{i+1}$, X_{i+2} Y_{i+2} are same. So the reusability technique avoids the repeated operations. Table.4 shows the power consumption and area utilization of the MAC unit with and without repeated pixel values consideration using different multipliers.

Table.4. Power and area analysis of MAC with and without repeated pixel values consideration

MAC type	Multiplier type					
	Array multiplier		Booth multiplier		Developed multiplier	
	Power in mw	Area in µm2	Power in mw	Area in µm2	Power in mw	Area in µm2
Without reusability consideration	52.51	10259	4.02	45377	3.748	50721
With reusability consideration	36.24	13887	2.88	61925	0.416	73394

By comparing the results shown in Table.4 the power consumption of MAC with repeated pixel values consideration reduced by 88% compared to MAC without repeated pixel values consideration with small area overhead.

5. CONCLUSION

The performance of the developed low power multiplier has been estimated and compared with some existing multipliers. The developed unit has been tested for image processing systems exploiting insignificant bits in pixel values and the similarity of neighbouring pixels in video streams. The power and area analysis of MAC using hybrid encoded multiplier, array multiplier and Booth multiplier has been done. From the power and area analysis of MAC with repeated pixel values consideration and without repeated pixel values consideration, it is clear that the MAC with repeated pixel values consideration consumes less power with small area overhead.

REFERENCES

[1] Unsal O S and Koren I, "System-level power-aware design techniques in real-time systems", *Proceedings of the IEEE*, Vol. 91, No. 7, pp.1055-1069, 2003.

[2] Gandhi K R, and Mahaptra N R, "Dynamically exploiting frequent operand values for energy efficiency in integer functional units", *Proceedings of 18th International Conference on VLSI Design*, pp. 570-575, 2005.

[3] Choi J, Jeon J and Choi K, "Power minimization of functional units by partially guarded computation", *Proceedings of the IEEE International Symposium on Low Power Electronics and Design*, pp. 131–136, 2000.

[4] Chen O T C, Wang S, and Wu Y W, "Minimization of switching activities of partial products for designing low-power multipliers", *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, Vol. 11, No. 3, pp. 418–433, 2003.

[5] Tsoi K H and Leong P H W, "Mullet-A parallel multiplier generator", *Proceedings of International Conference on Field programmable Logic and Applications*, pp. 691-694, 2005.

[6] Chen K H and Chu Y S, "A low power multiplier with spurious power suppression technique", *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, Vol. 15, No.7, pp. 846–850, 2007.

[7] Huang Z and Ercegovac M D, "High performance low power left-to-right array multiplier design", *IEEE Transactions on Computers*, Vol. 54, No. 3, pp. 272-283, 2005.

[8] Pieper L, Costa E, Almeida S, Bampi S and Monteiro J, "Efficient dedicated multiplication blocks for 2's complement radix-16 and radix-256 array multipliers", *Proceedings of Second International Conference on Signals, Circuits and Systems*, pp. 1-6, 2008.

[9] Gwee B H, J S Chang, Shi Y, Chua C C and Chong K S, "A low-voltage micropower asynchronous multiplier with shift-add multiplication approach", *IEEE Transactions on Circuits and Systems-I*, Vol. 56, No. 7, pp. 1349–1359, 2009.

[10] Sung G N, Lu Y C and Wang C C, "A power-aware signed 2-dimensional bypassing multiplier for video/image processing", *Proceedings of International Conference on Consumer Electronics*, pp.11-2.4, 2010.

[11] Ko U, Balsara P and Lee W, "Low-power design techniques for high-performance CMOS adders", *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, Vol. 3, No. 2, pp. 327-333, 1995.

[12] Song P J and De Micheli G, "Circuit and architecture trade-offs for high-speed multiplication", *IEEE Journal on Solid-State Circuits*, Vol. 26, No. 9, pp. 1184-1198, 1991.

[13] Veeramachaneni S, Krishna K M, Avinash L, Sreekanth R P and Srinivas M B, "Novel architectures for High-Speed and Low-Power 3-2, 4-2 and 5-2 Compressors", *Proceedings of the 20th International Conference on VLSI Design*, pp. 324-329, 2007.

[14] Rouholamini O, Kavehie O, Mirbaha A, Jasbi S and Navi K, "A new design for 7:2 compressors", *IEEE/ACS International Conference on Computer Systems and Applications*, pp. 474-478, 2007.

[15] Yeh W C and Jen C W, "High-speed Booth encoded parallel multiplier design", *IEEE Transactions on Computers*, Vol. 49, No. 7, pp. 692-701, 2000.

[16] Wang L R, Jou S J and Lee C L, "A well-structured modified Booth multiplier design", *Proceedings of IEEE International Symposium on VLSI Design, Automation and Test*, pp. 85-88, 2008.

[17] Chong K S, Gwee B H and Chang J S, "A micropower low-voltage multiplier with reduced spurious switching", *IEEE Transactions on Very Large Scale Integration Systems*, Vol. 13, No. 2, pp. 255-265, 2005.

[18] Chen K H, Chao K C, Guo J I and Chu Y S, "An efficient spurious power suppression technique (SPST) and its applications on MPEG-4 AVC/H.264 transform coding design", *Proceedings of IEEE International Symposium on Low Power Electron Devices*, pp. 155-160, 2005.

[19] Chen K H and Chu Y S "A low power multiplier with the spurious power suppression technique", *IEEE Transactions on Very Large Scale Integration Systems*, Vol. 15, No. 7, pp. 846-850, 2007.

[20] Fayed A, Elgharbawy W and Bayoumi M, "A data merging technique for high-speed low-power multiply accumulate

units", *Proceedings of IEEE International Conference on Acoustics, Speech and, Signal Processing*, pp. 145-148, 2004.

[21] Gao J and Chen J, "A novel asynchronous multiple function multiply-accumulator", *Proceedings of 6th International Conference on ASIC*, Vol. 1, pp. 223-226, 2005.

[22] Fujino M and Moshnyaga G, "Dynamic operand transformation for low-power multiplier-accumulator design", *Proceedings of International Symposium on Circuits and Systems*, pp. 345-348, 2003.

[23] Krishnamurthy R K, Schmit H and Carley L R, "A low-power 16-bit multiplier-accumulator using series-regulated mixed swing techniques", *Proceedings of IEEE Custom Integrated Circuits Conference*, pp. 499-502, 1998.

[24] Wang J S, Kuo C N and Yang T H, " Low-power fixed-width array multipliers", *Proceedings of IEEE Symposium on Low Power Electron Devices*, pp. 307-312, 2004.

[25] Liao Y and Roberts D B, "A high-performance and low-power 32-bit multiply-accumulate unit with single-instruction- multiple-data (SIMD) feature", *IEEE Journal on Solid-State Circuits*, Vol. 37, No. 7, pp. 926–931, 2002.

[26] Lee H, "A power-aware scalable pipelined Booth multiplier", *Proceedings of International Conference on System-On-Chip*, pp. 123-126, 2004.

[27] Hsu S K, Mathew S K, Anders M A, Zeydel B R, Oklobdzija V G, Krishnamurthy R K, and Borkar S Y, "A 110 GOPS/W 16-bit multiplier and reconfigurable PLA loop in 90nm CMOS", *IEEE Journal on Solid-State Circuits*, Vol. 41, No. 1, pp. 256–264, 2006.