A LEVEL SHIFTER ANTENNA FOR HIGH SPEED COMMUNICATION USING WILSON CURRENT MIRROR

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Abstract

A feed system that has been presented consists of high-gain antenna arrays that each have six slots and are arranged on a single substrate layer. This system makes use of a phase shifter that is not frequencydependent and a power splitter that is constructed on the design of a binary T-junction power splitter. The frequency of the signal is not taken into consideration by the phase shifter. In order for the antenna to attain its front-to-back ratio and high realized gain in ultrawideband areas, the feeding mechanism of the antenna is designed to be out-of-phase. This is done in conjunction with the correct antenna array architecture, which is implemented on distinct rows (2.5-6.8 GHz). Because of this, the antenna is able to accomplish both a high gain and a high front-to-back ratio (7.5–9.5 GHz). Applications that require communication over a wide band are appropriate candidates for the antenna that has been presented because of its vast bandwidth, high gain, and outstanding directivity. These characteristics make it an ideal contender for these applications. These are all limitations of earlier designs that have been reported in the literature, and they are all eliminated by the feeding system. The feeding system contributes substantially to an improvement in the array radiation directivity.

Keywords:

Feed System, High Gain, Power Splitter, Wilson Current Mirror

1. INTRODUCTION

Scaling the voltage is a tried and tested strategy for lowering the dynamic and leakage powers in the digital and mixed-signal systems of today. Scaling the voltage can be done in a number of different ways. Constructing ultra-low-power systems by reducing the supply voltage to values that are either close to or below the threshold voltage is a strategy that has shown to be very helpful [1].

Nevertheless, the performance of digital circuits suffers when they are operated either close to or below their thresholds, which has a negative effect on both efficiency and speed. It is required to make use of more than one supply voltage in order to accommodate the various components of the system, which work at different speeds. MSVD is an innovative method that allows designers the option to strike a better power-delay balance. MSVD is an abbreviation that stands for multi-supply voltage design. Through the use of the MSVD methodology, the design is sectioned off into a wide variety of voltage domains, and in order to ensure that the design timing restrictions are met, each of these voltage domains is provided with the appropriate supply voltage [2].

MSVD systems almost always make use of level-shifting circuits so that they can close the gap that exists between the various voltage levels. As a direct result of this, level shifters (LSs), which are able to convert between low voltage (VDDL) and high voltage (HV), have developed into an indispensable part of the modern systems (VDDH) [3] [4].

LSs ought to be noticeably quicker as well as more compact. In addition to this, they should be able to convert input voltages that are incredibly low while using the bare minimal amount of energy possible [4] [5]. Numerous LSs have been proposed as a potential solution, each of which possesses low power consumption, little latency, and a broad conversion range. The differential cascode voltage switch, also known as a DCVS, and the current mirror are the two varieties of LS designs that are deployed in practice the majority of the time (CM) [6].

The pull-up network of the CM-based LS circuit makes use of a current mirror circuit topology as its architecture. In response to a change in the state of an input signal, this topology causes a modification to take place in the transition current that is being carried by the transistors NM1 and PM1 [7]. Contention is reduced as a result of this. It is possible to say that this current has an effect on the output node (OUT) because it is reflected at the PM2 node [8]. Due to the design of this circuit, the LS circuit is able to work with only a small amount of supply voltage from the VDDL. This is because of the structure of the circuit. In standby mode, even though there is no change in the input signal, current continues to flow through the various nodes of the circuit, which results in a significant rise in the amount of static power that is consumed. This causes the amount of static power consumed to significantly increase [9].

This has been done in order to increase the performance of LS circuits. Because of this, the overall performance of the LS circuits has been improved to the point where they can reach their full potential [10]. Moving forward, we are going to proceed with classifying and evaluating these significant advances in further depth. When it comes to designing circuits, some of the basic types of approaches and structures that are available to choose from are as follows: cascaded LS circuits with multiple voltage domains and numerous stages, as well as cascode LS circuits with multiple voltage domains [11].

1.1 MODIFIED INPUT CIRCUIT

The architecture of the LS circuit determines whether the input signals are single-ended or differential. Both types of signals are possible. One example of this is a circuit that uses a multiple N-type input circuit. Finding an I.N. signal of high quality that is also complementary to the information that you are currently sending in can be challenging. The pass transistor can lessen the amount of switching energy required and lower the length of time required for the transition delay. Using the traditional pull-up network is something that can be done if one so chooses.

1.2 DCVS-BASED LS WITH DIODE

It is feasible to reduce the amount of current contention that is present in the circuits. However, doing so would result in a longer conversion time and a larger short-circuit current than would be the case otherwise. Neither of these outcomes is desirable. When it comes to the positioning of the transistors in a DCVS-based LS circuit, there is a wide variety of different conceivable designs that can be used. Every possible architecture for a circuit represents a trade-off between the three aspects of conversion delay, current contention, and short circuit current. The trade-offs can be made in a number of different ways. It is feasible to combine this approach with the current limiter circuit method, which makes use of additional transistors to minimize the normal short-circuit current. This can be done by following the instructions provided in both methods. This offers an additional advantage to the user.

1.3 LS WITH CURRENT LIMITER

In order to put a cap on the amount of current that can flow through the pull-up transistors, the structure of the current limiter makes use of the dynamic current mirror circuit concept. This action is taken with the purpose of weakening the pull-up network that is utilized in the DCVS-based LS circuit. As a direct consequence of this, the contention issue that can arise in an LS circuit that uses DCVS is overcome. In addition, once the output signal transition has been completed, it is disabled so that there is no loss of static power. This is done in order to prevent the loss of power. Drive capacity and the range of voltage that can be used are both lowered when the mirror structure is off, which also reduces the range of voltage that can be used.

1.4 MODIFIED CM-BASED LS

A number of adjustments were made to the CM-based LS circuit with the intention of cutting down on the amount of static current. The characteristics of the feedback loop in the circuit led to the implementation of these adjustments (s). As the CM-based LS circuit output impedance increases, the conversion rates it experiences become more gradual, and the output voltage swing becomes less dramatic. Both of these effects are a direct result of the increase in impedance. As a consequence of this, it is far more challenging to build a buffer circuit that has excellent overall performance. It is essential to keep in mind that the CM-LS have floating nodes, which renders them vulnerable to dynamic noise. This fact is one of the reasons why this is the case. As a direct consequence of this, these circuits are incompatible with the electrical components of systems intended for use in the aerospace and military industries.

2. ANTENNA DESIGN BASED ON LEVEL SHIFTER

During the process of fabricating the antenna, a taconic substrate that had a value of 4.3 for the r component and 0.0035 for the tan component was used. The antenna has the following dimensions: 167.48 millimeters in length, 158.25 mm in width, and 0.6 millimeters in height. The antenna is made up of a ground plane at the bottom, a microstrip feeding network at the top, and a radiating patch that gradually tapers off exponentially at the top. The ground plane is located at the bottom of the antenna.

The guided wavelength located in the frequency range that is considered to be the center of the ultra-wideband (UWB) spectrum. This calculation was performed using the frequency range that is considered to be the center of the UWB spectrum. The phase shifter is now able to operate at any frequency because a link has been built from one of the power lines to the phase shifter.

Because of this phase shifter, every power branch goes through a phase shift that is equal to 180 degrees plus 20 degrees. This makes the process of producing a steady and directional radiation pattern substantially more effective.

Parameter	mm	Parameter	mm
Fw	1.2	Sw	0.3
λg	21.1	Vw	0.3
Rs	$0.125 \times Ws$	Sl	$\lambda_g/2$
Sr	$\lambda_g/8$	S_5	$2 \times Fw$
Fr	$\lambda_g/8$	L_5	10.25
Vr	$\lambda_g/8$	Ls	147.7
Vfr	$\lambda_g/8$	Ws	158.25
Lv	$4 imes \lambda_g$	a+b	$\lambda g/4$

Table.1. Simulation Parameters

The two output ports of the power divider, which are located on segments 4 and 5, are the ones responsible for splitting the power in half while maintaining a phase difference of 180 degrees and 20 minutes. These two output ports are located on segments 4 and 5. The presence of fringing both at the end of the stub and all the way around the slot line creates a distinction in the apparent length of the arm that is a part of segment 4, and this distinction contributes to the overall length of the arm (segment 2). The difference that existed between the two ends of the segment has been changed as a result of the change in effective arm length that occurred at the microstrip transition as well as the power loss that occurred at that location.

These changes have occurred as a direct consequence of the microstrip transition. This is due to the fact that the planned antenna has a beam tilt angle that is less than nine degrees. Beam splitting, decreased gain, and decreased directivity are all possible outcomes that could be brought on by a significant shift in phase or magnitude difference. It is feasible for these effects to occur.

3. RESULTS AND DISCUSSION

The process of optimizing and simulating the performance of the proposed antenna makes use of high-frequency structure simulator (HFSS) software, which is available for purchase and may be found online. The proposed antenna has an impedance bandwidth that ranges from 2.5 to 6.8 GHz and achieves a loss in impedance bandwidth of less than 10 dB. (7.5–9.5 GHz). Figure 4b depicts the realized gain, which is lower than 14.12 dB across the whole bandwidth. Furthermore, the values that were measured and those that were modeled agree with one another in a manner that is very near to being in perfect accord.

The minor discrepancies between the simulated and measured results can, with the exception of 4, 8, and 8.5 GHz, be attributed to the losses that occur in the connector as a result of dimension imperfection and parasitic effect, imperfect soldering of the feed line with the connector, and fabrication errors during the process of etching and characterization of the parameters of the substrate. The fact that there are only a few key changes between the two collections of results lends credence to the idea that these losses are warranted.

Table.1. Antenna 1

Parameters	Value
f_c	0.952 GHz
$f_L - f_H$	0.79 - 1.22GHz
Impedance BW	32.5 MHz
Axial ratio	3.5 dB
Peak Gain	3.5 dB

Table.2. Antenna 2

Parameters	Measured	Simulated	
f_c	0.945	0.92	
$f_L - f_H$	0.89 - 1.20	0.89 - 1.22	
Impedance BW	315	325	
Axial ratio	0.845 - 1.13	0.84 - 1.13	
Peak gain (dB)	3.250	3.650	

Table.3.	Antenna	3
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Parameters	Simulated	Measured
f_c	0.885	-
Impedance BW	370	>370
Axial ratio	0.85 - 1.3	0.85 - 1.17
f _L - f _H	0.82 -1.27	<0.80 - 1.27
Peak Gain	290	245

Table.4. Antenna 4

Parameters	Simulated	Measured
f_c	0.935	0.949
fl-fн	0.70 - 0.76	0.838 - 1.06
Impedance BW	250	222
Peak gain (dB)	3.34	3.13

We initially evaluated the proposed antenna design in the lab to be certain that it would function properly before putting it to the test in the field. Following that, we moved on to the following phase, which was to build a microwave imaging measuring chamber in a clean environment. This was done after we had completed the previous step. The test is designed to research and assess the variance in GPR images in connection with the concealed targets that have been positioned within these apertures.

The purpose of the test is to investigate and evaluate the variance. These tests are designed to create GPR survey methods for measuring the length and width of cavities within a concrete block and pinpointing the location of subsurface pipelines, cables, or other metallic surfaces. The purpose of these tests is to develop GPR survey methods. These tests are being done with the intention of improving GPR survey methodologies.

In order to conduct the experiment, a variety of metallic objects are placed inside of three hollow aerated concrete brick houses, which are then stacked on top of one another after the stacking process has been completed. The major purpose of this mission is to unearth the hidden targets that are situated within certain areas of the map. Manual scans were carried out using a step size of 0.25 millimeters, and the recommended antenna was mounted at a height of 2.5 centimeters above the concrete surface. Following each scan, an image is constructed by gradually integrating the reflected echo signals that are received at each antenna point in the system. This is done in order to produce the final image.

During the subsequent scan, the echo from each antenna position is treated as if it were a pixel, and it is shifted about in order for it to align with the various components of the image map. This is done in order to ensure that the scan is accurate. The figure depicts the raw scanned data that was recovered from the radar module before any signal processing was carried out. A total of 176 scans were performed in order to create a comprehensive two-dimensional representation of the region that was being scanned. A substrate plate is placed as a target inside of the hollow concrete brick at a depth of 7.5 centimeters from the surface of the brick. This depth was determined by measuring from the center of the brick outward.

4. CONCLUSION

The antenna is used for the purpose of locating substrate plates that serve as targets that are put within the concrete block. These substrate plates are located using the concrete block as the locator. Brick and concrete were the first materials to be scanned after the surface had been cleaned. The power spectral density of the scanned image made the three voids in the brick appear to be smaller than they actually were. When placing all three plates into the hollow concrete block, a scanned image with three targets was revealed; however, a scanned image with just two targets was created after scanning the block with only two of the targets after one of the targets had been removed and scanned. The twodimensional imaging of the system detection of the target position and a hollow space inside the concrete brick demonstrates that the proposed antenna is suitable for use in microwave imaging applications. This demonstrates the suitability of the proposed antenna for use in microwave imaging applications. This illustrates that the suggested antenna is acceptable for utilization in applications involving microwave imaging.

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