

PERFORMANCE OF LEAKAGE POWER MINIMIZATION TECHNIQUE FOR CMOS VLSI TECHNOLOGY

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Abstract

Leakage power of CMOS VLSI Technology is a great concern. To reduce leakage power in CMOS circuits, a Leakage Power Minimization Technique (LPMT) is implemented in this paper. Leakage currents are monitored and compared. The Comparator kicks the charge pump to give body voltage (V_{body}). Simulations of these circuits are done using TSMC 0.35 μ m technology with various operating temperatures. Current steering Digital-to-Analog Converter (CSDAC) is used as test core to validate the idea. The Test core (eg.8-bit CSDAC) had power consumption of 347.63 mW. LPMT circuit alone consumes power of 6.3405 mW. This technique results in reduction of leakage power of 8-bit CSDAC by 5.51mW and increases the reliability of test core. Mentor Graphics ELDO and EZ-wave are used for simulations.

Keywords:

Leakage Currents, Current Comparator, Charge Pump, Test Core, Current Steering DAC, CMOS

1. INTRODUCTION

CMOS has become the dominant devices for VLSI digital and analog technology. To sustain device reliability and decrease power consumption, the supply voltage of these circuits have to be scaled down further to maintain the high drive current and achieve performance improvements, which in effect causes substantial increase in sub-threshold leakage current severely affecting the power dissipation. Since VLSI technology had both analog and digital circuits we have implemented mixed signal circuit (DAC) for test core. This paper is organized with section 2, briefing the previous work on power Minimization with various methods. Section 3, explains about leakage power Minimization technique. The results are presented in section 4, followed by conclusions on section 5. The circuit level implementations of Minimization technique with various bits of CSDAC are carried out.

2. LITERATURE SURVEY

H. Jeon, Y.-B. Kim, and M. Choi et al (2009) proposed a novel approach to minimize leakage current in CMOS circuit during the off-state (or standby mode, sleep mode) by setting the optimal substrate bias voltage to control the transistor threshold voltage. The total minimum leakage current is found by comparing the sub threshold current (I_{sub}) and band-to-band current (I_{btbt}). The proposed circuit was simulated in HSPICE using 32nm bulk CMOS technology and evaluated using ISCAS85 benchmark circuits at different operating temperature (ranging from 25oC to 100oC). Analysis of the results shows a maximum of 551 and 1491 times leakage power reduction at 25oC and 100oC on a circuit with 546 gates. The proposed approach demonstrates that the optimal body bias produces high energy reduction in nanoscale CMOS integrated circuits. Additionally

temperature and supply voltage variation effects are compensated by applying the feedback loop of the proposed technique [1].

Kaushik Roy, et al (2003) reviews various transistor intrinsic leakage mechanisms, including weak inversion, drain-induced barrier lowering, gate-induced drain leakage, and gate oxide tunneling. High leakage current in deep-sub micrometer regimes is becoming a significant contributor to power dissipation of CMOS circuits as threshold voltage, channel length, and gate oxide thickness are reduced. Consequently, the identification and modeling of different leakage components is very important for estimation and reduction of leakage power, especially for low-power applications. Channel engineering techniques including retrograde well and halo doping are explained as means to manage short-channel effects for continuous scaling of CMOS devices. Finally, the paper explores different circuit techniques to reduce the leakage power consumption [2].

Cassandra Neau, Kaushik Roy et al (2003) presented a techniques to determine the optimal body bias (forward or reverse) to minimize leakage current and compensate process variations in scaled CMOS technologies. A circuit trades off sub-threshold leakage with band-to-band tunneling leakage at the source/drain junctions to determine the optimal substrate bias for different technology generations and under process variations. Using optimal body bias results in 43% and 42% savings in leakage for predictive 70nm and 50nm NMOS devices, respectively. This technique also reduces the effects of die-to-die and intra-die process variations in transistor length and supply voltage by 43% and 60%, respectively, in 50nm NMOS devices, resulting in improved yield [3].

Kyung Ki Kim, Yong-Bin Kim, Minsu Choi, Nohpill Park et al (2007) estimated the total leakage power is critical to designing low-power digital circuits. In nanometer CMOS circuits, the main leakage components are the sub threshold, gate-tunneling and reverse-biased junction band-to-band-tunneling (BTBT) leakage currents. As transistor geometries decrease, it is necessary to reduce the supply voltage to avoid electrical breakdown and obtain the required performance.

However, to retain or improve performance, it is necessary to reduce the threshold voltage (V_{th}) as well, which results in an exponential increase of sub threshold leakage. To control short-channel effect and increase the transistor driving strength in deep-submicron (DSM) circuits, gate-oxide thickness also becomes thinner as technology scales down [4].

3. LEAKAGE POWER MINIMIZATION TECHNIQUE

Leakage Power Minimization technique has four stages; 1) Leakage Current Monitoring, 2) Current Comparator, 3) Charge Pump, and 4) Test Core (CSDAC).

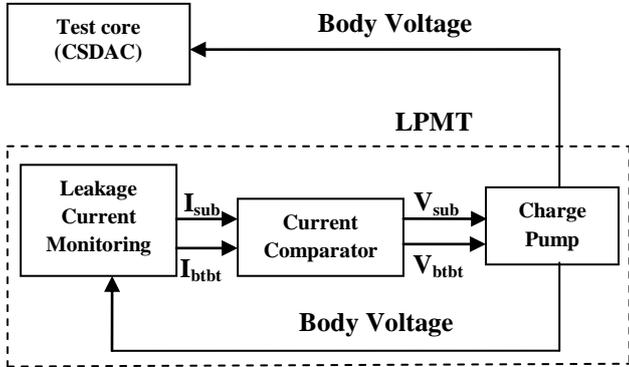


Fig.1. LPMT system

Fig.1 shows Leakage currents I_{sub} and I_{btbt} are monitored in stage 1. In next stage Current comparator gives out the compared values of leakage currents. Stage 3 produces the body voltage to test core (CSDAC).

3.1 LEAKAGE CURRENT MONITORING

Leakage Current Components in CMOS VLSI technology consists of the Threshold current, Band-to-Band Tunneling current and Gate to Bulk oxide tunneling current. Fig.2 shows all the leakage current components present in CMOS transistor. Mainly Sub-threshold and Band-to-band current causes more power leakage in CMOS circuits.

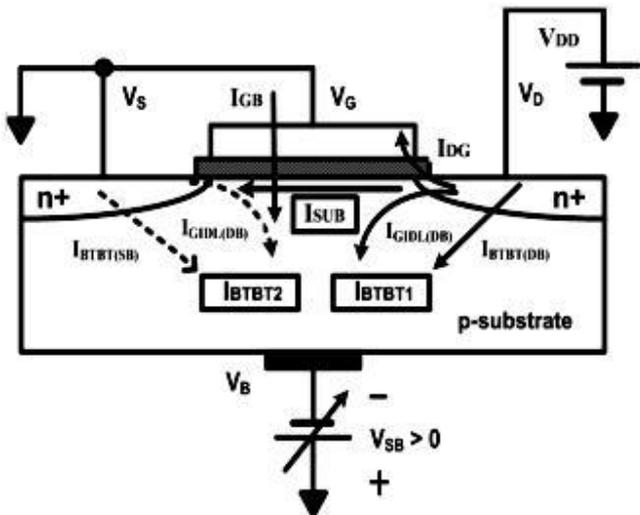


Fig.2. Leakage Current Components in MOS

The leakage monitoring circuit separates the sub-threshold leakage (I_{SUB}) and BTBT leakage current (I_{BTBT}) from the total leakage components. When there are two or more stacked transistors, the sub threshold leakage is reduced. This Minimization depends on the choice of the input pattern during standby

periods because it determines the number of off transistors in the stack.

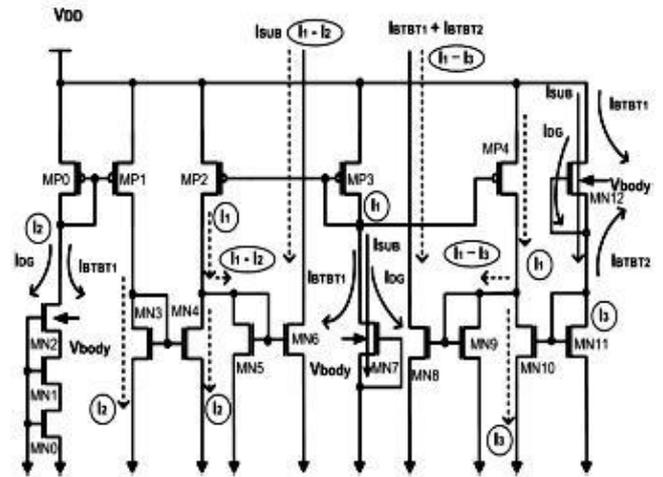


Fig.3. Leakage Current Monitoring Circuit

The leakage monitoring circuit separates the sub-threshold leakage (I_{SUB}) and BTBT leakage current ($I_{BTBT1, 2}$) from the total leakage components. Fig.3. shows a new leakage monitoring circuit for CMOS device, where the transistors, MN2, MN7, and MN12 are the replica circuits to generate leakage current components, and MP0/MP1, MP2/MP3, and MN10/MN11 form current mirrors.

By using triple off-transistors in a stack, we can ignore the sub-threshold current flowing from drain to source of MN2 transistor. Thus the amount of drain current of MN2 transistor notated as I_2 is approximately the same as the sum of I_{DG} and I_{BTBT1} . The drain current of MN7 notated as I_1 consists of I_{DG} , I_{BTBT1} , and I_{SUB} . In the source of the MN12 transistor, the current I_3 consisting of I_{DG} , I_{BTBT2} , and I_{SUB} is generated. The leakage monitoring circuit for PMOS device is made up of the same structure as the monitoring circuit for NMOS device. Two current differential amplifiers are employed based on the generated leakage components. I_{SUB} (current I_1 –current I_2) is obtained through MN4, MN5 and MN6 transistors while $I_{BTBT} = I_{BTBT1} + I_{BTBT2}$ (current I_1 –current I_3) is obtained through MN8, MN9, and MN10 transistors.

The separated leakage components are applied to the current comparator to generate pulse width proportional to the magnitude of each leakage. Then, depending on the two signals from the current comparator and its own bias voltage, the charge pump discharges or charges its output capacitor. The current comparator-based circuit provides the optimal body-bias voltage to match I_{SUB} with I_{BTBT} [1].

3.1.1 Stack Effect:

The stack formation of CMOS transistor produces a stack effect, it works by turning off more than one transistor in a stack forces the intermediate node voltage to go to a higher value than 0. This causes a negative V_{GS} , a negative V_{BS} (more body effect), and a V_{DS} reduction (less DIBL) in the top transistor closest to the outputs, thereby reducing the sub threshold leakage current flowing through the stack considerably, which is known as the stack effect. The leakage current decreases monotonically with the number of stacked off transistors. Because of the tran-

sistor stack effect, a gate's leakage current depends on its input combination. An individual CMOS gate shows a variation in the leakage power for different input patterns. Only a few input patterns, defined as dominant leakage states, cause significant leakage. When there are two or more stacked transistors, the sub threshold leakage is reduced. This reduction depends on the choice of the input pattern during standby periods because it determines the number of off transistors in the stack.

3.2 CURRENT COMPARATOR

The separated leakage components are applied to the current comparator to generate pulse width proportional to the magnitude of each leakage. It mainly consist Current mirror circuits. Then, depending on the two signals from the current comparator and its own bias voltage, the charge pump discharges or charges its output capacitor. The current comparator-based circuit provides the optimal body-bias voltage to match I_{SUB} with I_{BTBT} .

3.2.1 Current Mirror:

The cascode connection achieves a very high output resistance. Since this is a desirable characteristic for a current mirror, exploring the use of cascades for high-performance current mirrors is natural.

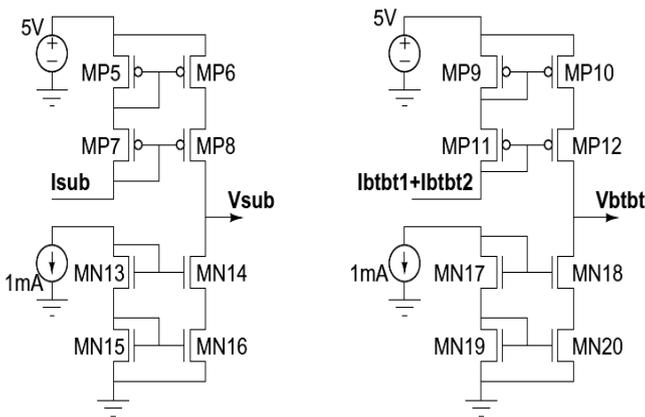


Fig.4 Cascode Current mirror

The separated leakage components are applied to the current comparator to generate pulse width proportional to the magnitude of each leakage. Fig.4. mainly consist Current mirror circuits. Then, depending on the leakage currents I_{sub} and $I_{bibt1} + I_{bibt2}$ from the Leakage Current Monitoring Circuit and positive reference current supply, the current comparator circuit produces V_{sub} and V_{bibt} leakage voltages.

The positive reference current has the value of 1mA. MP5, MP6, MP7, MP8, MN13, MN14, MN15 and MN16 form the cascode current mirror circuit which has I_{sub} as input likewise $I_{bibt1} + I_{bibt2}$ is given as input to MP9, MP10, MP11, MP12, MN17, MN18, MN19 and MN20 which form another cascode current mirror circuit. The current comparator-based circuit provides the optimal leakage voltages to match with I_{sub} and $I_{bibt1} + I_{bibt2}$.

3.3 CHARGE PUMP

Unlike the other traditional DC-DC converters, which employ inductors, CPs are only made of capacitors and switches (or diodes), CPs were used in smart power ICs and nonvolatile

memories and given the continuous scaling down of ICs power supplies.

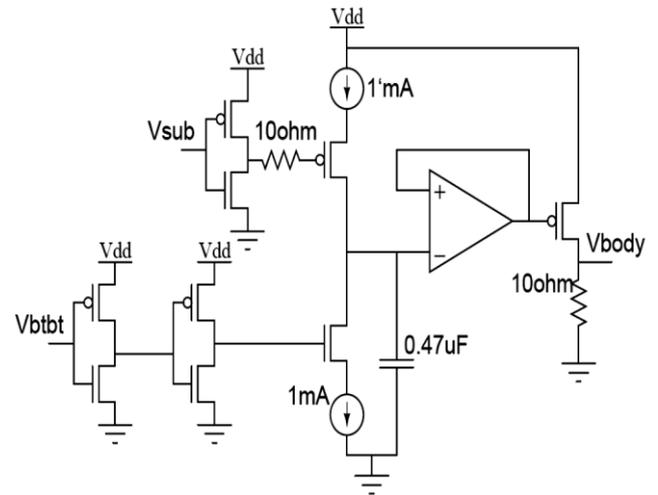


Fig.5. Charge Pump

Fig.5 shows the Charge Pump used in LPMT for CMOS VLSI circuit that converts the Sub-threshold voltage V_{sub} and Band-to-band tunneling voltage V_{bibt} to a DC output voltage V_{body} that is higher than V_{DD} (i.e., it is a DC-DC converter whose input voltage is lower than the output one).

3.4 TEST CORE

In this paper we have taken the test core as mixed signal circuit, current steering digital-to-analog converter. A Digital-to-Analog Converter transforms the digital representation of a signal into its equivalent analog value.

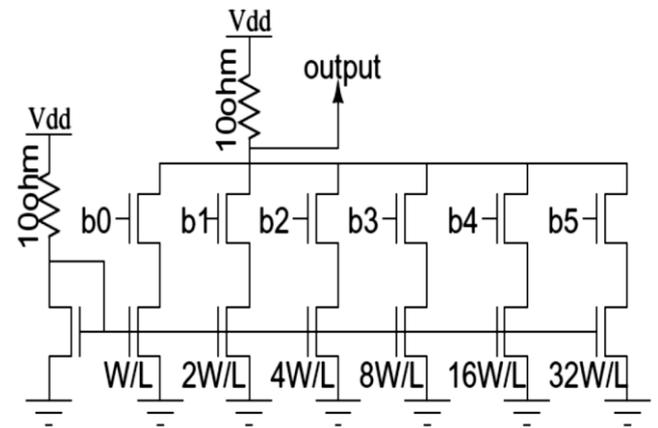


Fig.6. Test core (6-bit CSDAC)

An N-bit DAC accepts one among the 2^N digital codes as input. Due to the limited number of discrete amplitudes at the input, quantization error is inherent in a DAC. Fig.6 shows 6-bit CSDAC which had taken for consideration as test core in this paper. The width to length (W/L) value of the NMOS transistors are in the ratio 1:2:4:8:16:32. Digital input bits are given in "b0", "b1", "b2", "b3", "b4", "b5" of DAC circuits and "output" gives analog output in continuous slope fashion. 6-bit CSDAC produces 64 different voltages i.e. 6 to 2^6 . Likewise from 3-bit to 8-bit CSDAC are implemented as test core in this paper.

4. RESULTS

The power minimization system was simulated in Mentor Graphics ELDO & EZWAVE using TSMC 0.35µm CMOS technology and evaluated using test core (CSDAC) with wide temperature ranges. Fig.6 shows the average power consumption of CSDAC along with transfer characteristics. From the simulation results one can observe that power consumption increases linearly with resolution. To have fair comparison, 3, 4,5,6,7 and 8bit CSDAC results are superimposed in Fig.7.

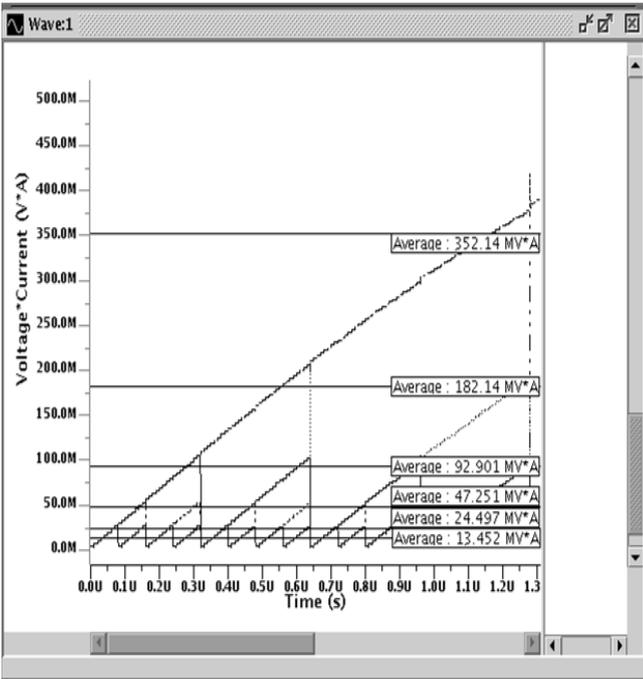


Fig.7. Transfer characteristics of Test core (3-8 bit CSDAC)

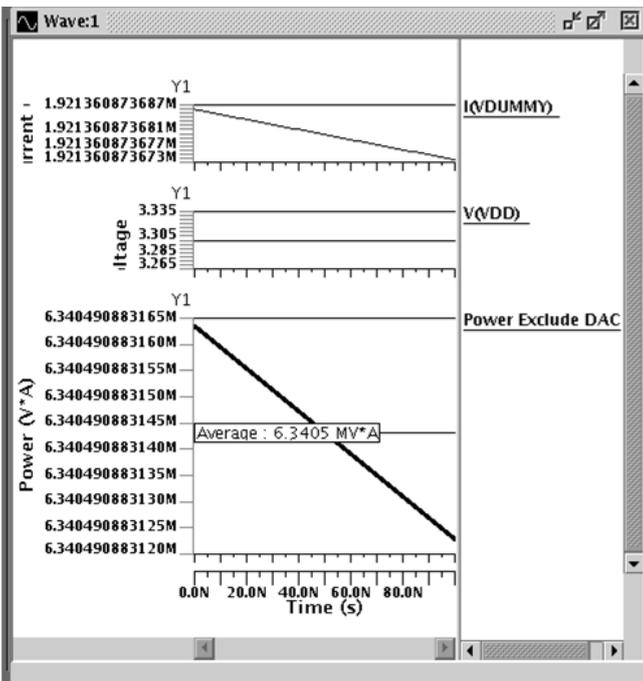


Fig.8. Average Power of Leakage power Minimization circuit

Fig.8 shows the average power of the leakage current monitoring, current comparator and charge pump in Leakage power minimization technique circuit alone. The average power consumption is 6.3405mW.

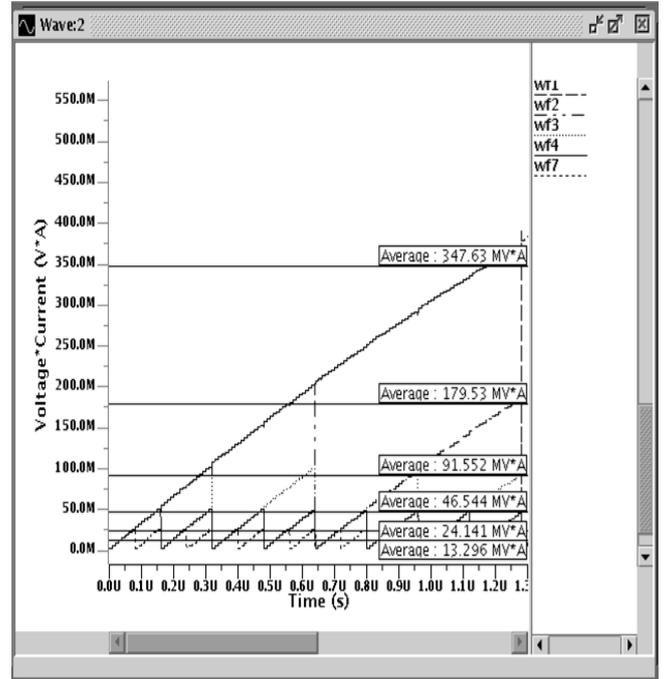


Fig.9. Average power consumption of LPMT system (inclusive of CSDAC [3 to 8 bit])

In comparing Fig.9 with Fig.7 one can observe the average power consumption is reduced for various resolution of CSDAC. In case of 8 bit CSDAC the power reduction is 5.51mW.

The LPMT system is validated for the test core at different temperature 27°C,-5°C and 100°C respectively and the results are tabulated.

Table.1. Comparison of Average Power at 27°C

CSDAC Circuits	Average Power Consumption of CSDAC alone without body bias (mW)	Average Power Consumption of CSDAC inclusive of LPMT circuit with body bias (mW)
3-bit	13.452	13.296
4-bit	24.497	24.141
5-bit	47.251	46.544
6-bit	92.901	91.552
7-bit	182.14	179.53
8-bit	352.14	347.63

Table.1 shows the average power consumption of various bits of CSDAC with body bias and without body bias.

Table.2. Comparison of Average Power at -5°C

CSDAC Circuits	Average Power Consumption of CSDAC alone without body bias (mW)	Average Power Consumption of CSDAC inclusive of LPMT circuit with body bias (mW)
3-bit	14.234	13.500
4-bit	25.885	24.583
5-bit	49.870	47.412
6-bit	97.947	93.213
7-bit	191.80	182.74
8-bit	396.51	353.22

Table.2 shows the average power consumption of various bits of CSDAC with body bias and without body bias at the operating temperature of -5°C.

Table.3. Comparison of Average Power at 100°C

CSDAC Circuits	Average Power Consumption of CSDAC alone without body bias (mW)	Average Power Consumption of CSDAC inclusive of LPMT circuit with body bias (mW)
3-bit	11.771	11.632
4-bit	21.508	21.196
5-bit	41.580	40.948
6-bit	81.927	80.697
7-bit	161.09	158.72
8-bit	313.78	309.62

Table.3 shows the values of various bits of CSDAC with body bias and without body bias at the operating temperature of 100°C. From the Table.1, 2 & 3 one can understand the average power Minimization is higher for 8-bit CSDAC for the proposed LPMT circuit in all temperatures. The values of average power in these table indicates that when the operating temperature goes low, average power get increases and when temperature goes high, average power get decreases. The reason for that is at temperature the mobility gets decreased because of second order effects like mobility, velocity saturation etc.

Fig.10 shows the average power of CSDAC with respect to various resolutions ranging from 3 to 8 bits for both the conventional and proposed LPMT system. From fig. 10 one can notice that the power consumed by LPMT system is lesser than that of conventional one. This technique can be applied to sigma delta modulator of high resolution 16, 20 bits DAC to have a significant power savings.

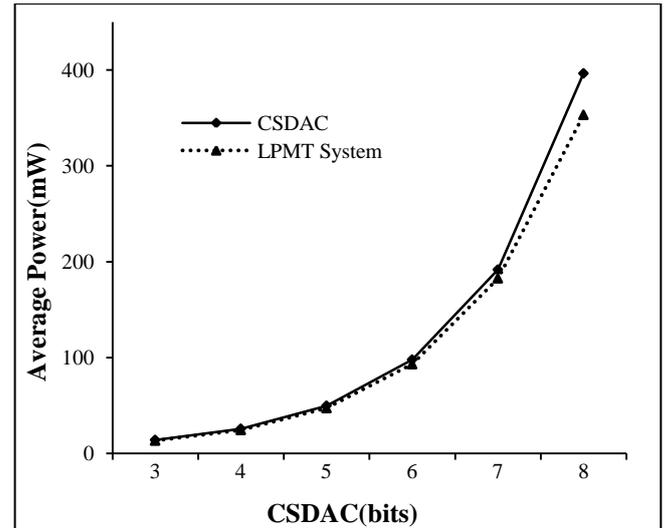


Fig.10. Average power of various bits in CSDAC

5. CONCLUSION

Leakage current components are measured using leakage monitoring circuit. By using charge pump body voltage is produced which in turn gives as feedback loop to test core and leakage current monitoring circuit in order to minimize power consumption. The result from LPMT system gives prominent power saving at wide range of temperatures. This trend may also be applicable for wide variation of process parameters. Hence this technique proves to be robust in minimizing the leakage power in finer technologies.

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