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IMPLEMENTATION OF TRANSMITTER AND RECEIVER ARCHITECTURE FOR PHYSICAL HYBRID INDICATOR CHANNEL OF LTE-ADVANCED USING PARTIAL RECONFIGURATION IN ML605 VIRTEX-6 DEVICE

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Abstract

LTE-A (Long Term Evolution-Advanced) is the fourth generation technology to increase the speed of wireless data network. The LTE-A Physical layer provides both data and control information between an enhanced base station and mobile user equipment which is quite complex and consists of a mixture of technologies. Since there is requirement for more resources to accommodate all the channels in a single FPGA, Partial Reconfiguration (PR) technique is introduced to configure the total hardware into sub modules that configure and operate in different instants of time. PR enables a part of FPGA to be reconfigured, while the rest continues to function without any interruptions and reduces the hardware resource power and fabric area. This work proposes the realization of transmitter and receiver architecture of Physical Hybrid Indicator Channel (PHICH) channel for LTE-A using partial reconfiguration on xc6vlx240tff1156-1 FPGA. The receiver architecture for PHICH is to report the correct reception of uplink user data to the User Equipment (UE) in the form of Acknowledgment (ACK), or Negative ACK (NACK) in a 1 millisecond duration sub-frame of Long Term Evolution (LTE) System. The modules for the different diversities are reconfigured based on the control signals from the transmitter.

Keywords:

Diversity, LTE, PHICH, Partial Reconfiguration

1. INTRODUCTION

LTE-A is a standard for wireless communication of high-speed data for mobile phones and data terminals, which is capable of providing high peak data rates, multi antenna support, reduced cost and wide range of bandwidth. The LTE physical layer provides a highly efficient means of conveying both data and control information between an enhanced base station and mobile user equipment (UE). LTE differs from its predecessors by using OFDM along with MIMO antennas. It has six physical downlink layer channels namely, physical Hybrid ARQ Indicator Channel (PHICH), Physical Control format Indicator Channel(PCFICH), Physical Downlink Control Channel (PDCCH), Physical Broadcast channel (PBCH), Physical Multicast Channel (PMCH) and Physical Downlink Shared Channel (PDSCH) for downlink operation. LTE-A supports both frequency-division duplex (FDD) and time-division duplex (TDD), as well as a wide range of system bandwidth in order to operate in a large number of different spectrum allocations [1]. The control signals are transmitted at the start of each sub-frame in the LTE grid.

Field Programmable Gate Array (FPGA) rapidly used for the several applications in different industries. Their great advantage is their flexibility that arises from their programmable nature as compared to systems using application specific integrated circuits (ASICs). Implementation of LTE downlink control channel architecture for Single Input Single Output (SISO) 1 × 1, Multiple Input Single Output (MISO) 4 × 1, Multiple Input Multiple Output (MIMO) 4 × 2 is implemented on virtex 5 FPGA [2]. The physical downlink channel processing involves scrambling, modulation, layer mapping, precoding, data mapping to the resource elements at transmitter and demapping from resource elements, decoding, delayer mapping, demodulation and descrambling at receiver. There is a new concept evolving in FPGA industry, called Partial Reconfiguration(PR) which can be exploited in many application fields, for instance to fulfill space requirements in small portable systems, to create a system-on-a-chip with a very high level of flexibility and to realize adaptive hardware systems. In order to configure an FPGA with the desired functionality, one or more bit streams are needed. The number of frames (configuration area) and the bits per frame are specific for each device family. The number of frames is proportional to CLB (Configurable Logic Block) width. PR is used for adaptive systems, to adapt their functionality to variations in their environment, leading to more sophisticated applications and improved system performance [3, 4]. Functionality of the system is modified by different configuration files (bitstream). A full bitstream of the design configures the static logic at the beginning of the execution of a reconfiguration system, to define the initial state of SRAM cells. Partial bitstream configures only a portion of the device and is one of the end products of any partial reconfiguration flow. The size of the bit stream is directly proportional to the number of resources being configured; it will shorten the reconfiguration time [5]. So PR offers a great improvement in terms of hardware resource usage, and degree of design flexibility. Alternatively, PR design using embedded configuration controller, wireless receiver and transmitter has been developed and tested to configure an Altera FLEX device, and Software defined radio design using partial reconfiguration discussed in [6,7].

The rest of this paper organized as follows. Section 2 describes the partial reconfiguration technique and section 3 describes the system architecture of the transmitter part of the PHICH. Section 4 describes the structures of the receiver part for PHICH. Section 5 and section 6 introduce the system model for the partial reconfiguration of PHICH transmitter and receiver respectively. Section 7 and 8 present results, analysis and conclusions.

2. PARTIAL RECONFIGURATION

Digital design process provides solutions for high performance, flexibility for multifunctional use, and energy

efficiency. Reconfigurable computing technology was developed to modify hardware features in the digital design process. Modern consumer appliances as wireless communication and multimedia systems present very strong requirements for reconfiguration. PR is one of the key features that is supported by programmable devices such as FPGAs, to change system functionality by loading different configuration bitstreams [8]. The PR method was initially a difference-based reconfiguration flow which only allowed small changes, e.g. block RAM contents and LUT equations. After that, it developed into a more advanced, "module based reconfiguration flow" design methodology. This allowed two or more modules which are similar in function to be reconfigured. A new reconfiguration flow based on Hierarchical design is introduced which offers improvements in timing results and reusability. Bus macro used in previous PR design flows to enable the communication between regions of static and reconfiguration module is removed in this method. This has the effect that signal delay may be reduced and hence timing result improved. A partition is a logical section of the design, defined by the user at a hierarchical boundary, to be considered for design reuse. In this method, resource utilization is a significant parameter, which determines the switching of PR modules. Partial reconfigurable platform, explore the architectural design space to shrink and obtain the optimized area and low power.

3. PHICH TRANSMITTER ARCHITECTURE

The PHICH carries the channel coded HARQ Indicator (HI) codeword. PHICH is used to report the Hybrid ARQ (HARQ) status which indicates to the UE whether the uplink user data is correctly received by the UE. The HARQ Indicator of '1' represents ACK and '0' represents NACK [9]. Multiple PHICHs are mapped to the same set of resource elements (REs). This set of REs constitutes a PHICH group. The PHICHs within a PHICH group are separated through different orthogonal sequences. The PHICH employs BPSK modulation. A PHICH group is not dedicated to a single mobile user; instead it is shared amongst eight users, by assigning each user a different orthogonal sequence index. Together the PHICH group number and orthogonal sequence index are known as a PHICH resource.

Table.1. Orthogonal Sequences for PHICH

User/Sequence index	Orthogonal sequence
0	[+1 +1 +1 +1]
1	[+1 -1 +1 -1]
2	[+1 +1 -1 -1]
3	[+1 -1 -1 +1]
4	[+j +j +j +j]
5	[+j -j +j -j]
6	[+j +j -j -j]
7	[+j -j -j +j]

Acknowledgement/ Negative Acknowledgement is the value to be transmitted in PHICH. ACK/NACK bit undergoes repetition coding, BPSK modulation, scrambling and multiplication with orthogonal sequences. The channel carries information of 8 users in 12 subcarriers. Hence each user has got an orthogonal sequence as shown in Table.1, to be multiplied with the information. The 12 subcarriers generated for each user are added individually or superpositioned with that of the other 7 users and transmitted after LTE processing. This sort of arrangement would increase the reliability. Signals are then transmitted after layer mapping, precoding and resource element mapping. General block diagram for PHICH transmitter is shown in the Fig.1. The transmitted signal undergoes the effect of channel gain and noise before reaching the receiver.

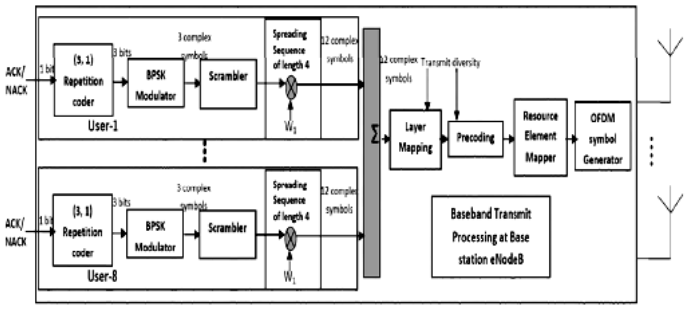

Fig.1. Transmitter Architecture for PHICH

4. PHICH RECEIVER ARCHITECTURE

In the receiver, the received signals after demapping and pre-processing with channel gain are again multiplied with orthogonal sequence of the specific user (w_1) to get back the 12 subcarriers of that user. Finally the HI is detected from the decoded output. General block diagram for PHICH receiver is shown in the Fig.2.

To implement the PHICH Architecture using Partial Reconfiguration, system has the 4 modes of operation. Each Mode of operation is the reconfiguration module for PR. Four modes of system model are, Single antenna port at both base station and UE, single antenna at base station and 2 antenna ports at UE, two antenna ports with Space Frequency Block Code (SFBC) at base station and one/two antenna ports at UE.

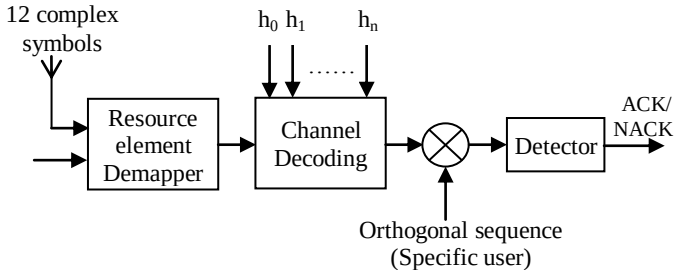

Fig.2. Receiver Architecture for PHICH

4.1 SISO ARCHITECTURE FOR PHICH

SISO Architecture of PHICH for LTE refers to a wireless communications system in which one antenna is used at the source (transmitter) and one antenna is used at the destination (receiver). SISO requires no processing in terms of the various forms of diversity that may be used. However the SISO channel is limited in its performance. Interference and fading will impact the system more than a MIMO system using some form of diversity. Fig.3 shows the basic architecture for SISO configuration which consists of three Receiver Processing Blocks (RPB) since there are 12 subcarriers in a column in each slot for PHICH. The internal architecture of RPB is shown in Fig.4.

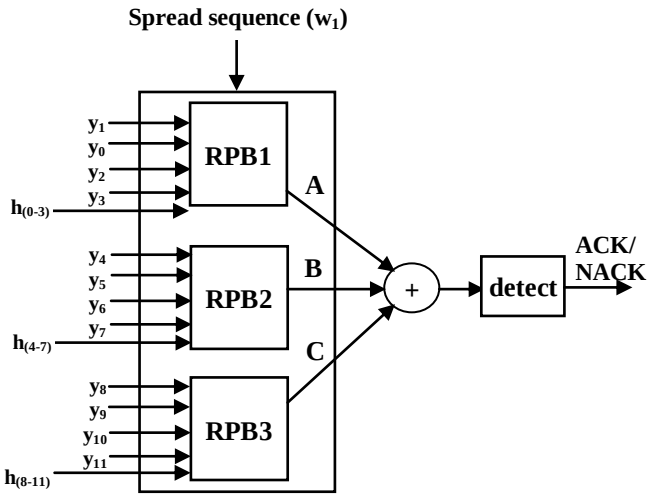

Fig.3. SISO Receiver for the PHICH

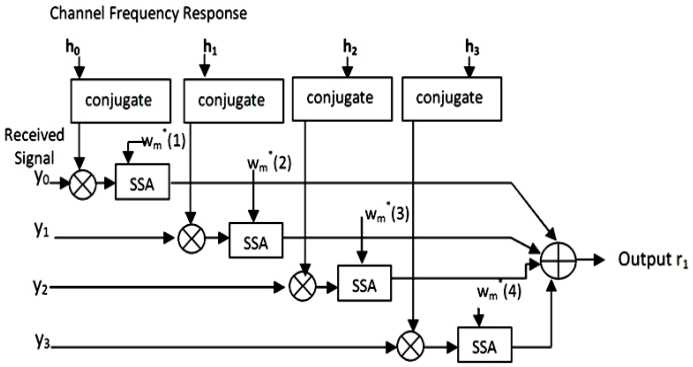

Fig.4. Internal Architecture of SISO Receiver Processing Block (RPB-1)

RPB1 multiplies set of four received signals (y_0 to y_3) with channel frequency response (h_0 to h_3) and the output is multiplied with the receiver spread sequence of specific user (w_1) in the SSA sub-block to obtain the decoded output $r_1$which is denoted as A. Similarly the RPB2 and RPB3 block process 4 received signals each and corresponding channel frequency response (h_4 to h_7) and (h_8 to h_{11}) respectively. The output is multiplied with the receiver spread sequence to obtain decoded outputs B and C respectively. Based on the spreading sequence bit[1, -1, *j*, -*j*], control bits of the SSA block are assigned as [00,01,10,11] respectively. The description of the SSA based on the control bits are listed in Table.2. The sum of the outputs of the four SSA is denoted as A. It is the output of RPB1 also. The output of RPB1, RPB2 and RPB3 A, B and C respectively are summed up and is given as input to HI Detection (HID) block.

In the detection circuit shown in the Fig.4, it is multiplied with $1/\sqrt{2} - j1/\sqrt{2}$ and the magnitude of the real part is checked for acknowledgement or negative acknowledgment [15].

Table.2. Description of SSA in RPBs

Spread Sequence bit	Control Bits	Description
+1	00	No change
-1	01	The signs of real and imaginary parts are changed
+j	10	Real and Imaginary parts are exchanged and the sign of real part is changed
-j	11	Real and Imaginary parts are exchanged and the sign of imaginary part is changed

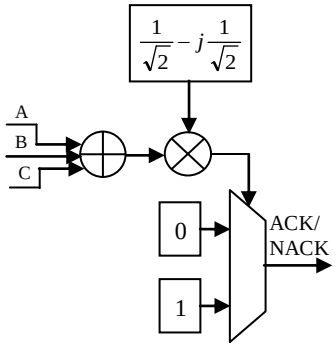

Fig.4. Detection module for the PHICH

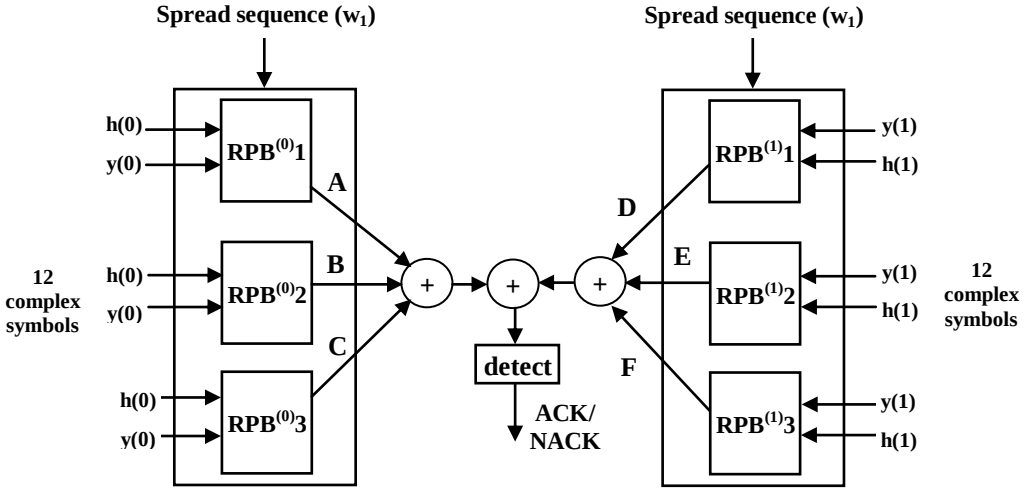

Fig.5. SIMO Receiver for the PHICH

4.2 SIMO ARCHITECTURE FOR PHICH

The SIMO 1 × 2 architecture is shown in the Fig.5. The architecture has two SISO processing blocks RPB(0) and RPB(1) for manipulation of signals received at Antenna '0' and Antenna '1' respectively. The internal structure of receiver processing blocks is as shown in Fig.4. The output of these processing blocks RPB (0) and RPB (1) are produced as A, B, C and D, E, F respectively. Their sum is given to detection circuit to check for ACK or NACK.

4.3 MISO ARCHITECTURE FOR PHICH

For MISO 2 × 1 architecture, a mix of two signals from two antennas with different set of channel estimations is received at the receiver as shown in Fig.6. It has three receiver processing blocks and detection block. The internal structure of MISO RPB has two different set of Channel estimation $h(0)$, $h(1)$ and the noise. The received signals from two antennas are multiplied with the channel estimation and the spread sequence of specific user (w_1). Sum of A, B and C is given to detection block to check for acknowledgement.

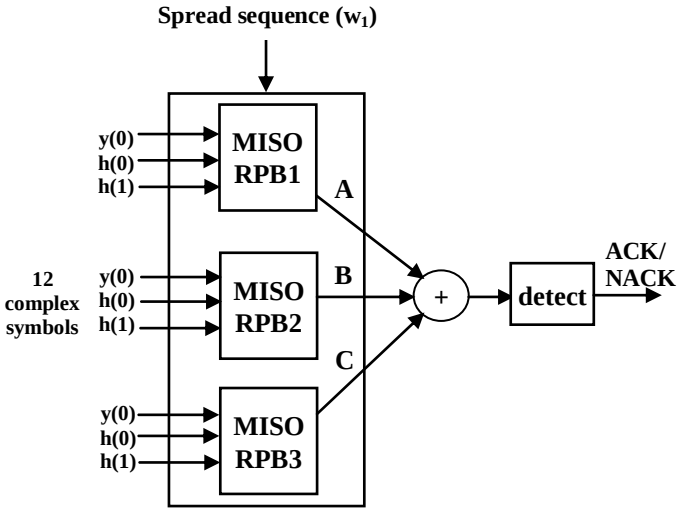

Fig.6. MISO Receiver for the PHICH

4.4 MIMO ARCHITECTURE FOR PHICH

MIMO 2 × 2 architecture shown in Fig.7 is similar to MISO architecture but the receiver has two receiving antennas and hence for each receiving antenna a mix of two signals from two transmitting antennas with different channel estimations and noise is received. The architecture has three receiver processing blocks and their output is fed to detection block.

The internal structure of MIMO RPB has four different channel estimation $h(00)$, $h(01)$ $h(10)$, $h(11)$ and noise value. The result is multiplied with spread sequence (w_1) and added together to get the decoded output A. Similarly the RPB2 and RPB3 block process 4 set of received signal and corresponding channel frequency response. The sum of A, B and C is given to Detection Circuit and the magnitude of the real part is checked for acknowledgement [15].

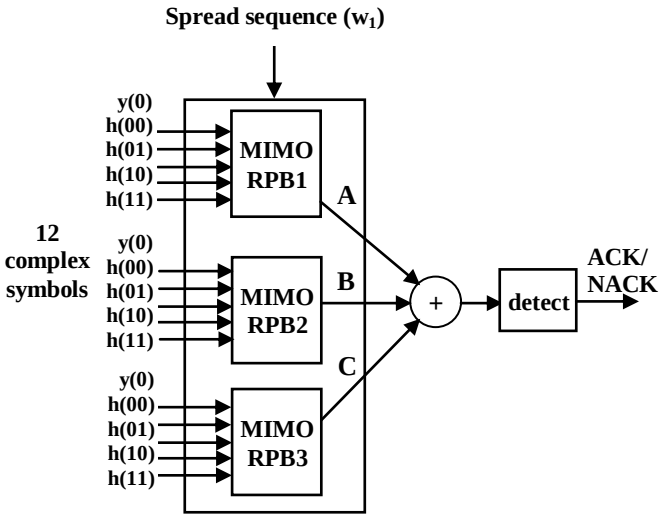

Fig.7. MIMO Receiver for the PHICH

5. SYSTEM MODEL FOR RECONFIGURATION OF PHICH TRANSMITTER ARCHITECTURE

The hierarchical design flow for the Partial Reconfiguration of PHICH receiver is shown in the Fig.8. The top module is divided into two Reconfigurable Partitions (RPs). RP is defined as an area of the FPGA device to which the Partial Reconfiguration is applied. Each RP is mutually independent of others. In other words, the logic and functionality of the RP may be swapped using the technique of Partial reconfiguration, while rest of the FPGA device can continue its operation. Reconfiguration Module (RM) is defined as the swappable functionality within the RP. Each Reconfigurable partition may have multiple associated RMs. For the particular configuration, one of the RM occupies the RP. RM shares the allocated hardware resources within the RP. In the transmitter, layer mapping and precoding corresponding to SISO, SIMO, MISO and MIMO are the swappable functionalities. Control information from the higher level layers and the global clock logic are used in the static logic which remain constant throughout design process.

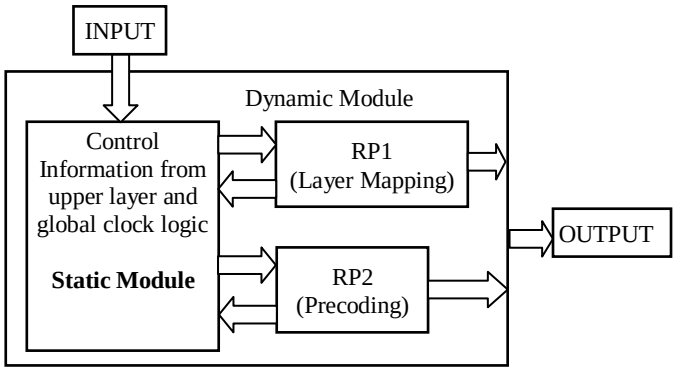

Fig.8. PR Architecture of PHICH transmitter on FPGA

The system model for the Partial Reconfiguration (PR) of PHICH transmitter is shown in Fig.9. The system design is divided into static logic and reconfigurable logic. The functionality of the static logic does not change during operation. The static logic contains the repetition coder,

modulator, orthogonal cover assignment, scrambler and resource element mapping modules. In PR transmitter design, 4 modes of reconfigurable module are single antenna port at both eNodeB and UE, single antenna at eNodeB and 2 antenna ports at UE, two antenna ports with Space Frequency Block Code (SFBC) at base station and one/two antenna ports at UE. Using PR technique, flexibility of the hardware modifies the system functionality and it is reconfigured for one of the four diversities.

Based on diversity selection, layer mapped output from 1 or 2 layers are precoded for specific diversity. Finally, precoded output from dynamic region is mapped to the REs of LTE grid. The configuration Bit files are converted into SystemACE File format and it is stored in the Compact Flash (CF) memory. Maximum of 8 Configuration images are stored in CF memory with 8 configuration address. During system run time, diversity selection signal is used as input for configuration address selection. The modules for single antenna at eNodeB and UE(SATSAR), single antenna at eNodeB and two at UE (SATMAR), two antennas at eNodeB and single at UE (MATSAR), two antennas at eNodeB and UE(MATMAR) are stored in CF. It is observed that reconfiguration time is shorter for partial bitstream.

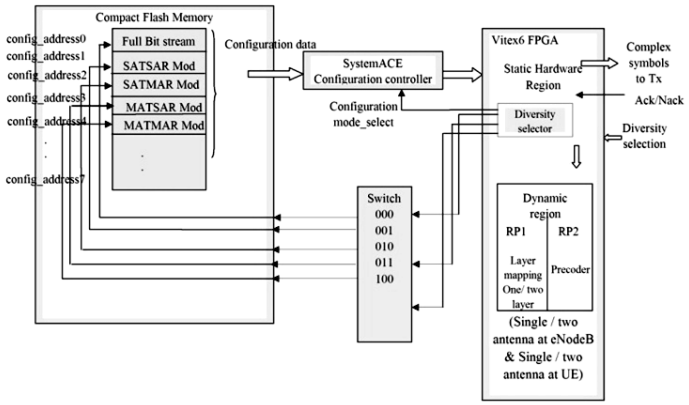

Fig.9. Hardware setup for implementation of PR transmitter

6. SYSTEM MODEL FOR RECONFIGURATION OF PHICH RECEIVER ARCHITECTURE

6.1 HIERARCHY OF SYSTEM DESIGN

The hierarchical design flow for the Partial Reconfiguration of PHICH receiver is shown in the Fig.10. The system model is designed for the receiver architecture of the PHICH for LTE-A, based on the analysis of Partial Reconfiguration. The PHICH receiver will get the acknowledgement information from uplink user data to the User Equipment (UE). Based on diversity chosen, FPGA is configured and the necessary components of the different diversities SISO, SIMO, MISO, and MIMO are programmed.

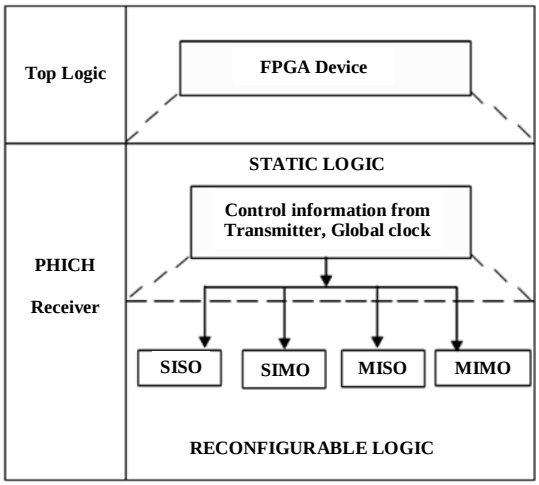

Fig.10. Hierarchical Design methodology for PHICH Receiver Architecture

6.2 PARTIAL RECONFIGURATION ARCHITECTURE FOR PHICH RECEIVER

The receiver side of the PHICH Architecture consists of demapping of the resource elements, decoding and detection. The receiver architecture is designed with two receiving antennas. When transmitter diversity is SISO or MISO, antenna 1 is enabled to receive. Similarly when SIMO or MIMO case occurs both the antennas are enabled to receive. According to the control signal, Receiver module is configured for the particular diversity. Configuration of particular diversity is implemented in the corresponding reconfigurable partition, and the resource is shared within the RP, so the area of the FPGA is reduced. Flow graph for the design process of PR is shown in the Fig.11.

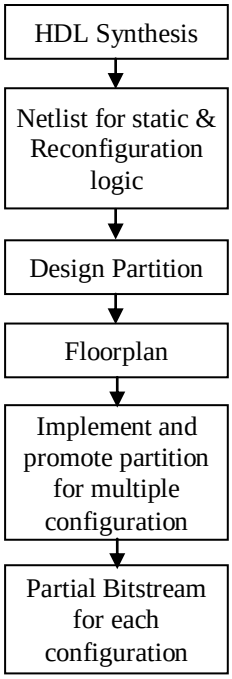

Fig.11. Flow diagram for the partial reconfiguration of PHICH receiver

At the system level, Partition may have multiple modes, which are mutually exclusive configuration of a module that might be activated at different times, with compatible inputs and outputs. At process time, net lists for static and reconfiguration modules were generated by synthesis. PlanAhead PR tool is used for the system partition [10]. Reconfiguration modules are added to the RPs. Modules may switch from one mode to another and the receiver is configured based on the diversity signal. Multiple configurations generated for SISO SIMO, MISO and MIMO modules and it will utilize the same reconfiguration area which is depend on the frame size of the device. Depends on the device family of FPGA frame size will vary.

Floor plan of RP based on number of frames shown in the Fig.12. In this case, virtex 6 is used where the area occupied by the frame is determined by the CLBs and the DSP slices [11, 12]. The RP region (dynamic region) is dedicated to SISO, SIMO, MISO and MIMO modules. Multiple configurations are created for the Partial Reconfiguration of the different permutations of SISO, SIMO, MISO, MIMO (RMs) and they are implemented, and thus configuration files are generated. Once area group ranges have been defined, implementation process for each configuration and partial bit streams are generated. The set of active RMs along with static logic is considered as a complete design for the particular application [13, 14]. Multiple configurations will exist for SISO, SIMO, MISO and MIMO case. RMs for these cases is implemented by separate partial BIT files. Each configuration has its own independent configuration run. The resulting output files are .ngd, .ngm, .ncd, and .pcf format files, and report files.

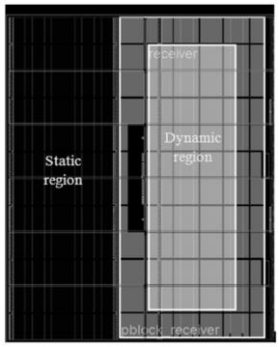

Fig.12. Floorplan PR Architecture of PHICH receiver on FPGA

7. RESULTS AND DISCUSSION

PHICH Transmitter and Receiver architectures are realized using Partial Reconfiguration with Diversities as reconfiguration modules. To demonstrate the feasibility of the proposed architecture, Virtex-6 L×240T FPGA (xc6vlx240tff1156) is used for the realization. The results of multiple configurations in terms of resource utilization are discussed in this section. A Reconfigurable Region (RR) is an area on the device allocated to logic during design time. It includes different types of basic primitives such as configurable logic blocks (CLBs), Block RAMs, and DSP Slices. Synthesis tools are used to build netlists for base design and RMs, for different configuration. Different RMs associated with a Reconfigurable Partition (RP) use various resources. The Area Group Range of the RP must contain a superset of resources used by all its RMs.

The simulation waveforms of PHICH transmitter is shown in Fig.13. The PHICH transmitter with LTE specifications of Frequency ‘freq’: 1.4 MHz, Physical Layer Cell ID ‘cellid’: 1, PHICH ‘Ng’ factor: 1. ‘phich’ shows the transmitted PHICH values after mapping to the first column of the LTE grid.

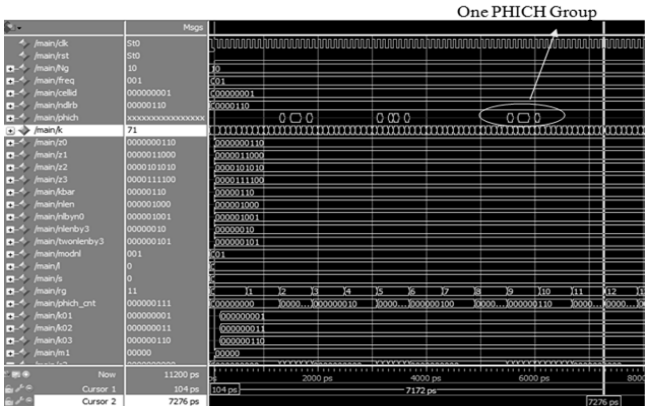

Fig.13. Simulation wave for PHICH transmitter

Implementation results of direct and PR method of PHICH transmitter are summarized in Table.3. It is observed that PR implementation requires less resources compared to the direct implementation. Partial bitstream size increases the flexibility to configure the specific diversity of PHICH transmitter. Partial bitstream size for layer mapping module and precoding module is 151KB, 323 KB. Base design configuration bitstream size is 9017 KB. Reconfiguration values are calculated for 200MHz system speed of Virtex 6 FPGA, and the measured values are given in Table.4. It satisfies the LTE time constraints. One useful symbol length without cyclic prefix of single column in LTE grid is 66.7µs. The values in the reconfiguration table satisfy the LTE grid Time constraint. The PR architecture can also reduce the reconfiguration time. Since the size of the bit stream is directly proportional to the number of resources being configured, partial reconfiguration utilizes a smaller bit stream than a full bit stream for the FPGA. The FPGA editor for the different Reconfiguration Modules of the PHICH transmitter is shown in Fig.14.

Table.3. Performance of partial reconfiguration method

Method	Diversity	Resources (in %)				Max clk delay (ns)	Speed MHz
		LUT	Registers	Slice	DSP		
DIRECT	Single configuration	5	3	7	1	5.7340	230.730
PR	SISO	3	1	6	1	4.9720	185.632
	SIMO	3	1	6	1	4.9720	185.632
	MISO2 × 1	4	1	5	1	5.0579	197.707
	MIMO2 × 2	4	1	5	1	5.0579	197.707

Table.4. Reconfiguration and processing time of PHICH transmitter on xc6vlx240tff1156-1 device

From RM	To RM	Reconfiguration time(ns)	Processing time (ns)	Total time taken(ns)
SISO	SIMO	20	4.9720	24.9720
	MISO	20	5.0579	25.0579
	MIMO	50	5.0579	55.0579
SIMO	SISO	35	4.9720	39.9720
	MISO	50	5.0579	55.0579
	MIMO	60	5.0579	65.0579
MISO	SISO	35	4.9720	39.9720
	SIMO	35	4.9720	39.9720
	MIMO	60	5.0579	65.0579
MIMO	SISO	35	4.9720	39.9720
	SIMO	35	4.9720	39.9720
	MISO	50	5.0579	55.0579

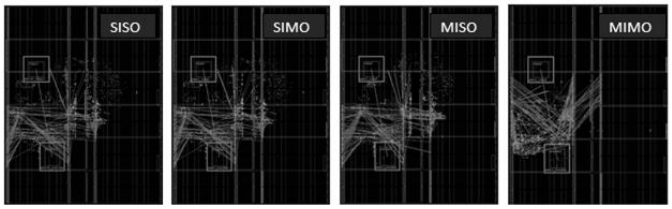

Fig.14. Implemented device for PHICH transmitter on xc6vlx240tff1156 device

The PHICH receiver modelsim waveform is shown in Fig.15. Ack1-8 in the waveform shows the 8 user group PHICH and 'ack' signal represents the output. 'sum' is the decision variable shows the correct reception of ACK/NACK. Sign bit of variable 'sum' decides the output, where sign bit '1' as NACK, '0' as ACK.

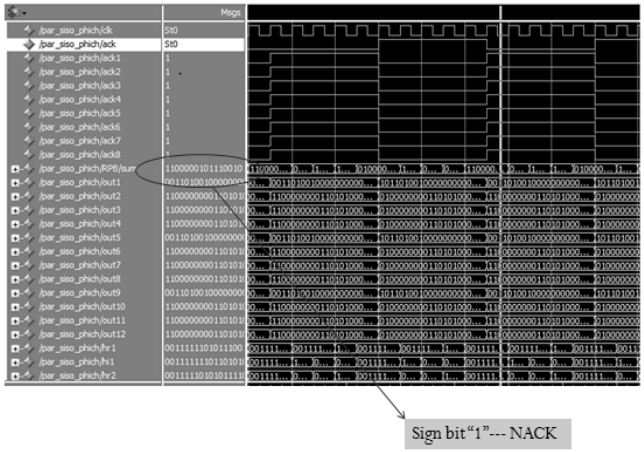

Fig.15. Simulation Wave for PHICH Receiver

Implementation in device xc6vlx240tff1156-1 also helps to determine the resource utilization which indicates the amount of resources exploited by the entire PHICH receiver architecture. Table.5 gives the implemented results of PHICH receiver in terms of maximum delay, speed, number of frames and size of Full and Partial bitstreams.

Table.5. Implementation results of PHICH receiver

Method	RM	Max Delay/ clk(ns)	Speed (MHz)	No of frames	Bitstream size(kb)
Direct	-	16.507	60.580	Whole FPGA	9017
PR	SISO	13.324	75.052	108	3235 (partial bit stream)
	SIMO	13.860	72.150		
	MISO	14.245	70.200		
	MIMO	15.555	64.288		

Using the synthesis result, the estimated resource reduction including both RP compared to the direct method in terms of LUT and DSP48 shown in the Table 6. The proposed architecture could achieve reduction of resources in terms of DSP48Es, LUTs, registers and slices compared to direct implementation.

Table.6. Resource reduction table for direct and PR method

Resource	Available	Direct Method	PR
LUT	150720	13267	6223
DSP48	768	424	238

The FPGA editor for the different Reconfiguration Modules of the PHICH Receiver is shown in Fig.16. The placing and routing of MIMO has been increased compared to the SISO, because need of more resources in MIMO. These two reconfigurable modules placed in the 1st Region (RP1) of the floorplan.

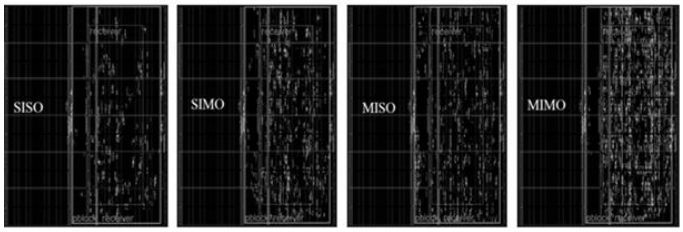

Fig.16. FPGA Editor of Receiver for SISO, SIMO, MISO and MIMO configuration

Table.7. Reconfiguration Time of PHICH receiver on xc6vlx240tff1156-1 device

From RM	To RM	Reconfiguration time(ns)	Processing time (ns)	Total time taken (ns)
SISO	SIMO	160	13.860	173.860
	MISO	125	14.245	139.245
	MIMO	310	15.555	325.555
SIMO	SISO	115	13.324	128.324
	MISO	205	14.245	219.245
	MIMO	145	15.555	160.555
MISO (2 × 1)	SISO	125	13.324	138.324
	SIMO	205	13.860	218.860
	MIMO	235	15.555	250.555
MIMO (2 × 2)	SISO	310	13.324	323.324
	SIMO	145	13.860	158.860
	MISO	290	14.245	304.245

As reconfiguration times are highly dependent on the size and organization of the RPs, an additional benefit is that the reconfiguration time is shorter because of reduction of size of partial bitstream. So the proposed Architecture could achieve the reduction in device size and configuration time for the essential operation. Table.7 summarizes the reconfiguration time and the processing time involved during the swapping of one RM to another.

8. CONCLUSION

In this paper, Partial Reconfiguration Technique is proposed for the realization of the Single Input Single Output (SISO), Single Input Multiple Output (SIMO-1 × 2), Multiple Input Single Output (MISO-2 × 1), and Multiple Input Multiple Output (MIMO-2 × 2) diversities of PHICH Physical Downlink Control Channel for LTE-A in FPGA. The realization of the transmitter and receiver using PR could achieve the resource reduction in terms of number of LUTs, DSPs, Registers and Slices used with respect to MIMO, MISO, SIMO, SISO configuration. The concept of hardware reusability is achieved by using Partial Reconfiguration method and leading to the reduction of hardware size in the FPGA Device. In future, the result can be further improved to accommodate all the six physical downlink channels of LTE-A implemented in the single FPGA hardware using PR technique.

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