HARDWARE IMPLEMENTATION OF PIPELINE BASED ROUTER DESIGN FOR ON-CHIP NETWORK

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Abstract

As the feature size is continuously decreasing and integration density is increasing, interconnections have become a dominating factor in determining the overall quality of a chip. Due to the limited scalability of system bus, it cannot meet the requirement of current System-on-Chip (SoC) implementations where only a limited number of functional units can be supported. Long global wires also cause many design problems, such as routing congestion, noise coupling, and difficult timing closure. Network-on-Chip (NoC) architectures have been proposed to be an alternative to solve the above problems by using a packet-based communication network. In this paper, the Circuit-Switched (CS) Router was designed and analysed the various parameters such as power, timing and area. The CS router has taken more number of cycles to transfer the data from source to destination. So the pipelining concept was implemented by adding registers in the CS router architecture. The proposed architecture increases the speed of operation and reduces the critical path of the circuit. The router has been implemented using Verilog HDL. The parameters area, power and timing were calculated in 130 nm CMOS technology using Synopsys tool with nominal operating voltage of 1V and packet size is 39 bits. Finally power, area and time of these two routers have been analysed and compared.

Keywords:
SoC, NoC, Circuit Switched Router, Worm-Hole Router, Latency

1. INTRODUCTION

Network-On-Chip (NoC) is an effective and scalable alternative to bus based and point-to-point schemes for meeting communication requirements in a system with large number of processing cores. NoCs offer low latency high bandwidth communication when compared to the bus based schemes. The NoCs concepts include distributing the communication structure and using multiple routes for data transfer. This allows creating flexible, programmable, and even reconfigurable networks [1], [2].

In general, a packet-based NoC consists of routers, the network interface between the routers and the processing unit, and the interconnection network. A 4×4 mesh-based NoC interconnection network is shown in Fig.1. The processing core (PC) can be a general purpose processor, a DSP, an embedded memory etc. Each PC is attached to a router which connects it to its neighbouring PCs [3]. The NoC-based SoCs impose new and critical design challenges. Firstly, which topology is suitable for the applications of the target NoCs. Secondly, the design of network interfaces to access the on-chip network and routers to provide the physical interconnection mechanisms to transport data between processing cores. Thirdly, the selection of communication protocols (including routing, switching, buffer management, flow control, etc.), which are suitable for on-chip

interconnection networks. Finally, technology scales and switching speed of the NoC [4], [5].
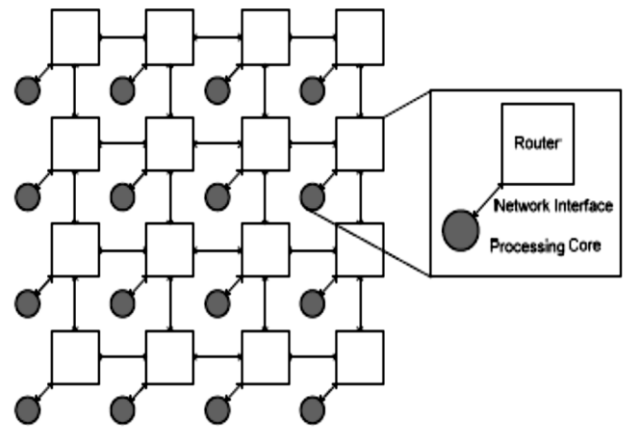

Fig.1. Mesh based NoCs architecture

2. RELATED WORKS

Every design and innovative researches in VLSI circuits are trade-off between speed, area and power. Similar with that, different on chip router methodologies carried out to reduce area, power and increase speed. In order to provide efficient router for NoC, novel methods were introduced at Network Interface kernel part of the router which contains buffer, control unit, routing unit and some queuing or scheduling unit. Some of the earlier works are studied in this paper and listed below.

According to the resources of NoC, Kavaldjiev et. al analyzed two different virtual router architectures. In which, they had proposed new scheme to reduce router area size and increase the speed. The proposed idea in their paper is Virtual Channels are directly connected to Switch Fabric (SF) rather than multiplexing with SF next to buffer stage [6]. Bei Yin developed a wormhole router for NoC which support multicast routing to provide performance predictability [7]. Nousias et. al analyzed a new mechanism that reduces the memory space used in a conventional implementation of virtual channels. The mechanism had developed based on adaptive rate control where the required buffer size is reduced [8]. Lee et. al proposed efficient clock boosting mechanism to enhance the performance of adaptive router by increasing the accepted load and reducing the average latency [9].

Performance in terms buffer usage, latency and throughput of wormhole router had improved by applying different flit admission and ejection model [10]

2.1 SWITCHING MECHANISM

There are different types of routers are available in Multiprocessor system to use the shared memory. This section describes the three different switching mechanisms for NoCs.

2.2 CIRCUIT SWITCHING

In circuit switching, a physical path is reserved from source to destination before the transmission. A header of the message is injected to the network and when it reaches the destination, the complete path has been set up and an acknowledgment is sent back to source so that message contents may be transmitted at the full bandwidth of the hardware path. Circuit switching is advantageous when messages are infrequent and long, i.e. when the transmission time long compared to the path setup time. On the other hand, the physical path is reserved for the duration of the message and may block other messages [11].

2.3 WORM HOLE SWITCHING

Wormhole switching is a special case of cut-through switching. Instead of storing a packet completely in a node and then transmitting it to the next node, wormhole routing operates by advancing the head of a packet directly from incoming to outgoing channels of the routing chip. A packet is divided into a number of flits (flow control digits) for transmission. The size of a flit depends on system parameters, in particular, the channel width. The header flit (or flits) governs the route. As soon as a node examines the header flit(s) of a message, it selects the next channel on the route and begins forwarding flits down that channel.

In wormhole switching, contiguous flits in a packet are always contained in the same or adjacent nodes of the network. This can cause difficulties, as possibility of deadlock arises. Deadlock in the interconnection network occurs when no message can advance towards its destination because the queues of the message system are full. No communication can occur over the deadlocked channels until exceptional action is taken to break the deadlock [12], [13].

2.4 VIRTUAL CUT THROUGH SWITCHING

The technique of virtual channels allows deadlock-free routing to be performed in any tightly connected interconnection network. In order to reduce the effect of message blocking, physical channels may be split into virtual channels and these will be used to increase the total throughput of the physical channel. Virtual channels are logical entities associated with a physical link used to distinguish multiple data streams traversing the same physical channel. They are multiplexed over a physical channel in a demand-driven manner, with bandwidth allocated to each virtual channel as needed [14].

3. CONVENTIONAL CIRCUIT SWITCH ROUTER

The CS router provides a simple data-path, being composed only of a crossbar with registered outputs. I/O port is 39-bits wide, it consists of consists of 32 data bits(0-31), 3 destination bits(32-34), 3 source bits(35-37), and 1 control bit(38). The crossbar has 5 paths from each input. In this router the data will be sent to control block present in the router, then the control block generates the crossbar select signal by using the source address. The select signal selects one path among the available path in the crossbar block. Fig.2 shows the architecture of circuit-switched router.

The data format will be shown below. Packet Format for CS Router:

Control Bit(1)	Source bits(3)	Destination bits(3)	Pay load (32)

The advantage of the CS router is very simple method and need not to split the data packet. But the drawback is buffer size which is equal to the packet size, so it requires large size buffer.
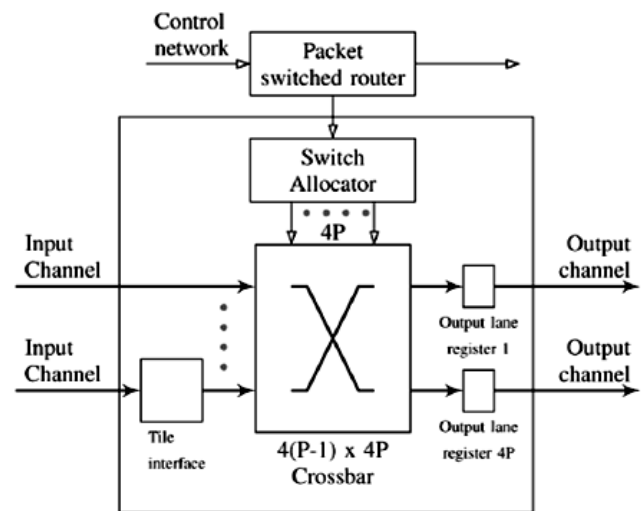

Fig.2. Architecture of conventional CS Router

The complete architecture of Router has been coded in Xilinx environment by using Verilog Hardware Description Language. The Verilog code has been improved as synthesizable coding to invoke with the Synopsys design compiler. The time, power and area have been calculated using design vision in Synopsys tool [15], [16].

4. PROPOSED ROUTER LOGIC

Conventional CS router, increment in the critical path decreases the operating speed of the circuit because it requires more clock cycles to transfer a data from source to destination ports. To overcome this drawback, pipeline concept has been introduced in conventional CS router architecture. In our study we introduced 5 – stage pipeline is described below,

Five pipeline stages are,

S1: Input Fetch

S2: Allocates the path from source to destination

S3: Switch Allocator stage

S4: Crossbar switch stage

S5: Output stage

Table.1 shows the pipelining stages in the CS router. X-axis shows the number of clock cycles and Y-axis shows the stages in the router.

Table.1. 5 Stage pipeline

				S5	...	S5	S5	S5	S5	S5
			S4	S4	...	S4	S4	S4	S4	
		S3	S3	S3	...	S3	S3	S3		
	S2	S2	S2	S2	...	S2	S2			
S1	S1	S1	S1	S1	...	S1				
1	2	3	4	5	...	9	10	11	12	13

The registers were added to store the data in the three stages such as S1, S2, S3, S4 and S5 (i.e. Registers are added in the input channels, Path allocation stage, Switch Allocator, Cross bar and output stage). The proposed router takes 3 cycles to transfer the 1st data, but after 3 cycles the data will be received to the destination for each cycle. Table.1 shows the pipeline stages of the proposed architecture. The speed of operation has been increased and reduces the critical path. But the area, power and latency has been increased slightly due to the additional registers.

5. RESULTS AND DISCUSSION

The test bench has written to verify the functionality of the router architecture using Modelsim tool. Verilog HDL code of WHWP router was synthesized and implemented in XILINX and Virtex II Pro (selected device: 2v40cs144-6) FPGA Board respectively. RTL schematic view of proposed router was achieved by synthesizing Veilog Code using Xilinx. In order to analyse area, power consumption and performance, these two router architectures were synthesized in a Synopsys Design Compiler using 130nm technology. We set up the synthesis environment using an operating voltage of 1V (typical voltage).

5.1 CONVENTIONAL CS ROUTER

The CS router without pipelining is verified for various input combinations. Below Fig.3 shows the waveform for CS router without pipelining. Here the CS router has taken two cycles to transfer the data from source to the destination.
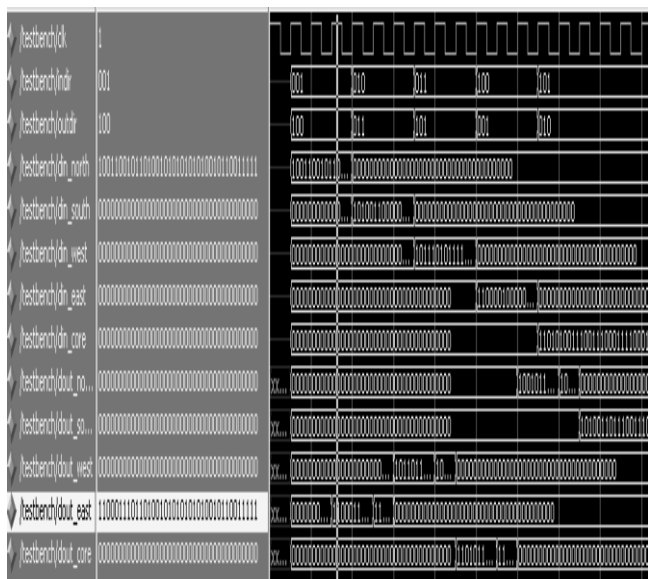

Fig.3. Simulation Result of conventional CS Router

5.2 PROPOSED ROUTER

The CS router with pipelining is verified for various input combinations. Below Fig.4 shows the waveform for CS router with pipelining. Here the CS router has taken three cycles to transfer the data from source to the destination for the 1st input, after that data transfers continuously. Fig.5 shows the RTL schematic view of proposed router for Virtex II Pro FPGA.
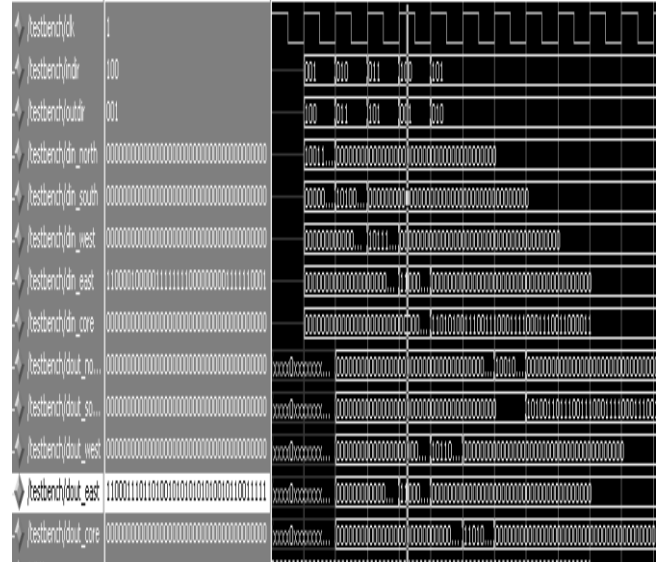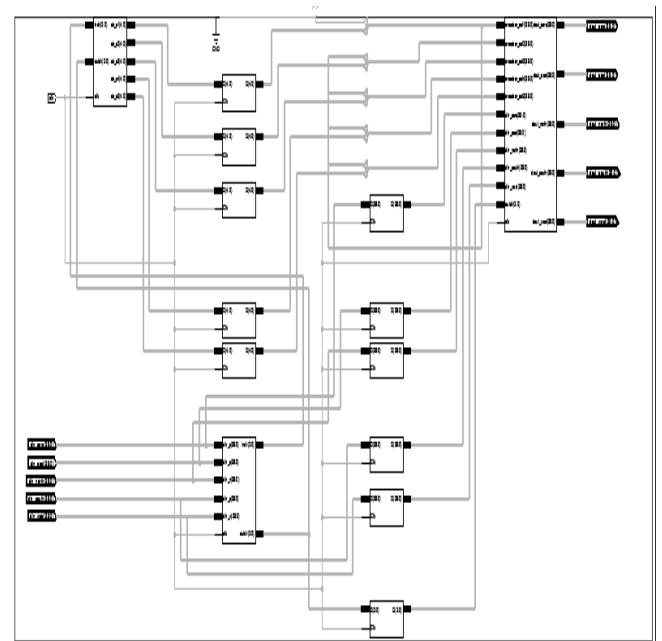

Fig.4. Simulation Result of Proposed Router

Fig.5. RTL Schematic view of proposed router

5.3 COMPARISON OF CONVENTIONAL CS ROUTER AND PROPOSED ROUTER

Table.2 shows the comparison between the CS router with and without pipelining. The Combinational area, Non Combinational area, Slack time, Dynamic power and leakage power had calculated using Synopsys Tool with 130nm

technology with nominal operating voltage of 1V. Library file used to calculate the area, power and slack time in Synopsys is fsc0h_d_sc_bc. The CS router with pipelining has occupied larger area and power than the CS router without pipelining. Fig.5 shows the comparison chart of conventional CS Router and proposed router.

Table.2. Comparison result of CS and CS with pipeline router

Parameters	CS Router without Pipeline	CS Router with Pipeline
Dynamic Power	4.112 mW	6.8256 mW
Leakage Power	2.7402 μW	4.2768μW
Slack Time	3.12ns	2.29ns
Combinational Area	4190μm2	4040 μm2
Non Combinational Area	7989μm2	15549μm2
Total Cell Area	12179 μm2	19589μm2

By applying pipeline technique, slack time is reduced from 3.12ns (data required time = 3.81, data arrival time = -0.69) to 2.29ns (data required time = 3.93, data arrival time = -1.64). Fig.6 compares the power consumption of WH and WHWP with packet size of 39 bits. The cell internal power is increased by 16% while net switching power is reduced by 16% with pipeline technique.
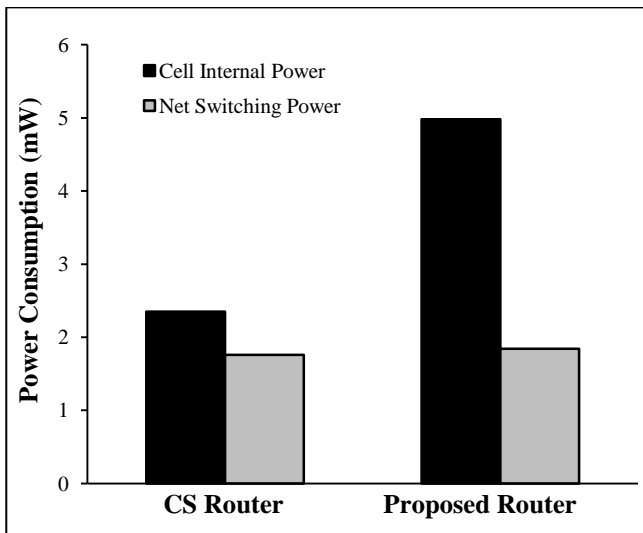

Fig.6. Power consumption of CS and Proposed router

6. CONCLUSION

In this paper, we introduced pipeline technique for NoC routers to minimize the required clock cycle for data transmission from source to destinations. Three different pipeline stages namely input fetch, path allocation and crossbar were implemented in CS router. All the functionalities of proposed router verified and synthesized using Modelsim and

Xilinx. In addition to this delay, area and power parameters also had calculated using Synopsys with UMC 130nm technology.
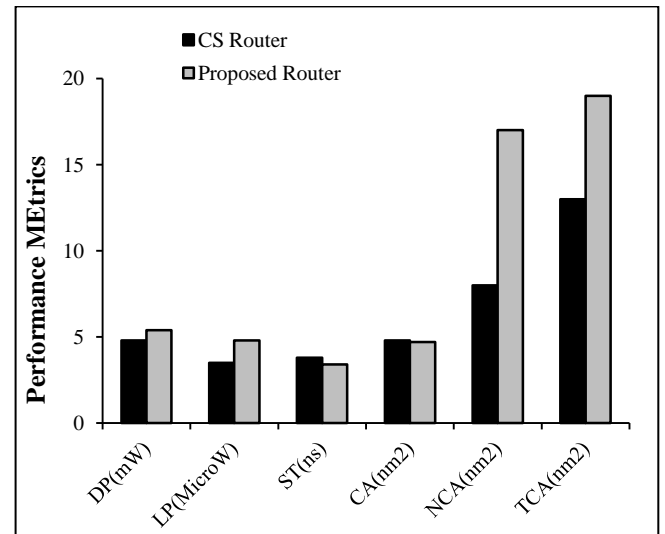

Fig.7. Comparison between CS Router with and without Pipelining

Finally, this proposed router compared with conventional CS router. Comparison results clearly stated that the proposed router design reduced critical path and transmitted a data packet from source to destination with less clock period. In future, we intend to design a NoC router with less power and area.

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